DATA ACQUISITION USING AT89c51 AND PCL-207

SUBMITTED BY:-

DILLIP KU. DAS (10507017)

SANDEEP SHEETAL (10507016)

UNDER GUIDANCE OF:-

Prof. U.C.PATI

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG.

NATIONAL INSTITUTE OF TECHNOLOGY

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ABSTRACT

A typical data acquisition system consists of individual sensors with necessary signal conditioning, data conversion, data processing, multiplexing, data handling and associated transmission, storage and display system.

In order to optimize the characteristics of a system in terms of performance, handling capacity and cost, the relevant subsystem can be combined together. Analog data is generally acquired and converted into the digital form for the purpose of processing, transmission and display.

Rapid advances in Personal Computer (PC) hardware and software technologies have resulted in easy and efficient adoption of PCs in various precise measurement and complex control applications. A PC based measurement or control application requires conversion of real world analog signal into digital format and transfer of digitized data into the PC. A data acquisition system that performs conversion of analog signal to digital data and the digital data to analog signal is interfaced to a pc to implement the functions of a measurement and control instrumentation applications.

In this project we have used the electromagnetic sensor to acquire the data of a magnetic disk angular velocity, which we have got in mili volts range. This has been further converted approximately into the range of 5 volt by using an instrumentation amplifier of suitable gain (~20).We then converted the analog voltage into digital by using ADC 0808 and the processing part is done by using ATMEL89c51.In the second case we have used the data acquisition card PCL-207 to interface the amplified output to PC.

CONTENTS

CHAPTER 1

Introduction

1. INTRODUCTION

1.1 PC based Instrumentation System

The instrumentation systems have evolved over a period of time. Instrumentation systems are in standalone or modular types. Traditionally, measurement and control are done using standalone instruments. The measurement and control are automated by exchanging data between the instruments and computers. There are several ways of exchange of measurement and control data between computer and instruments. The GPIB, RS-232, USB and IEEE 1394 are the standard interfaces provided in high performance standalone instruments for exchange of data. The general form of PC based measurement system is shown below.

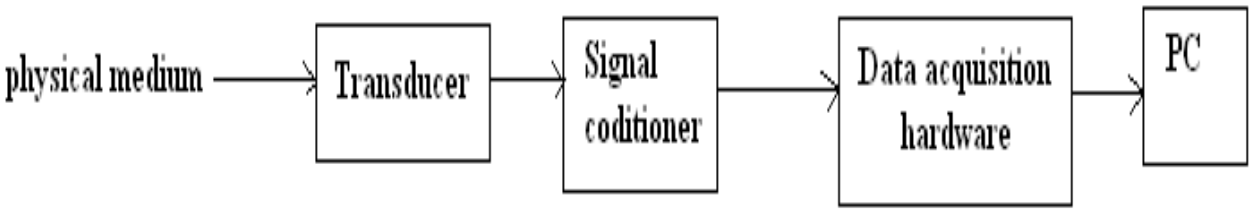


Figure1 (Block Diagram of DAQ System)

A PC-based measurement system is achieved on a PC platform with the aid of a DAQ (Data Acquisition) system. Design of a PC-based measuring system involves:

(i) Design of a data acquisition hardware, and

(ii) Design of appropriate application software.

1.2 Data Acquisition Systems

Data acquisition refers to getting real world signals into computer. A PC being a digital system cannot directly accept the analog signal from the sensor. The data acquisition system (DAQ) performs the conversion of analog to digital and subsequently to transfer the digital data to PC. In general a DAQ system performs following four important functions:

(i) Analog to digital conversion
(ii) Digital to analog conversion
(iii) Digital input/output
(iv) Timing I/O.

For a measurement application, the DAQ system converts the analog signal form signal conditioning circuit to a digital data and transfers it to the computer. For a control application it converts digital data from the computer to analog signals for controlling external devices.

1.2.1 PC Interfaces

The DAQ hardware is available in different forms. The most common type is plug in type which is inserted into one of the empty expansion bus slots on the motherboard. The hardware uses the PC expansion bus for communication with the PC. The DAQ devices which are compatible with PC serial port (RS232 compatible) and USB port are also more common. The DAQ system support one of these interfaces for communication with the PC.

1.2.2 Software

The driving force behind the PC based data acquisition and control is the software. The software in general includes data acquisition, data processing and display routines. The data acquisition routine in software generates the required signals on the require control signals on the interface bus. It receives converted data from the DAQ system through the interface bus and stores the data in an array in the memory. Data processing routine in the software extracts the relevant information regarding the measurement from the acquired data. It can perform certain functions of signal conditioning by means of data processing. The PC executes software routines for (i) acquiring the data from DAQ system (ii) analyzing the acquired data for retrieving relevant information (iii) displaying the information in required format.

Programming a data acquisition and control system can be accomplished via either of three ways: hardware programming, driver level programming and package level programming.

CHAPTER 2

Sensing elements

2. SENSING ELEMENT

2.1 Digital tachometers

Digital tachometers (digital tachometric generators*)* are usually non-contact instruments that sense the passage of equally spaced marks on the surface of a rotating disc or shaft. Measurement resolution is governed by the number of marks around the circumference. Various types of sensor are used, such as optical, inductive and magnetic ones. As each mark is sensed, a pulse is generated and input to an electronic pulse counter. Usually, velocity is calculated in terms of the pulse count in unit time, which of course only yields information about the mean velocity. If the velocity is changing, instantaneous velocity can be calculated at each instant of time that an output pulse occurs, using the scheme shown in Figure .In this circuit, the pulses from the transducer gate the train of pulses from a 1MHz clock into a counter. Control logic resets the counter and updates the digital output value after receipt of each pulse from the transducer. The measurement accuracy of this system is highest when the speed of rotation is low.

2.1.1 Optical sensing

Digital tachometers with optical sensors are often known as optical tachometers. Optical pulses can be generated by one of the two alternatives photoelectric techniques illustrated in Figure, the pulses are produced as the windows in a slotted disc pass in sequence between a light source and a detector. The alternative form has both light source and detector mounted on the same side of a

reflective disc which has black sectors painted onto it at regular angular intervals. Light sources are normally either lasers or LEDs, with photodiodes and phototransistors being used as detectors. Optical tachometers yield better accuracy than other forms of digital tachometer but are not as reliable because dust and dirt can block light paths.

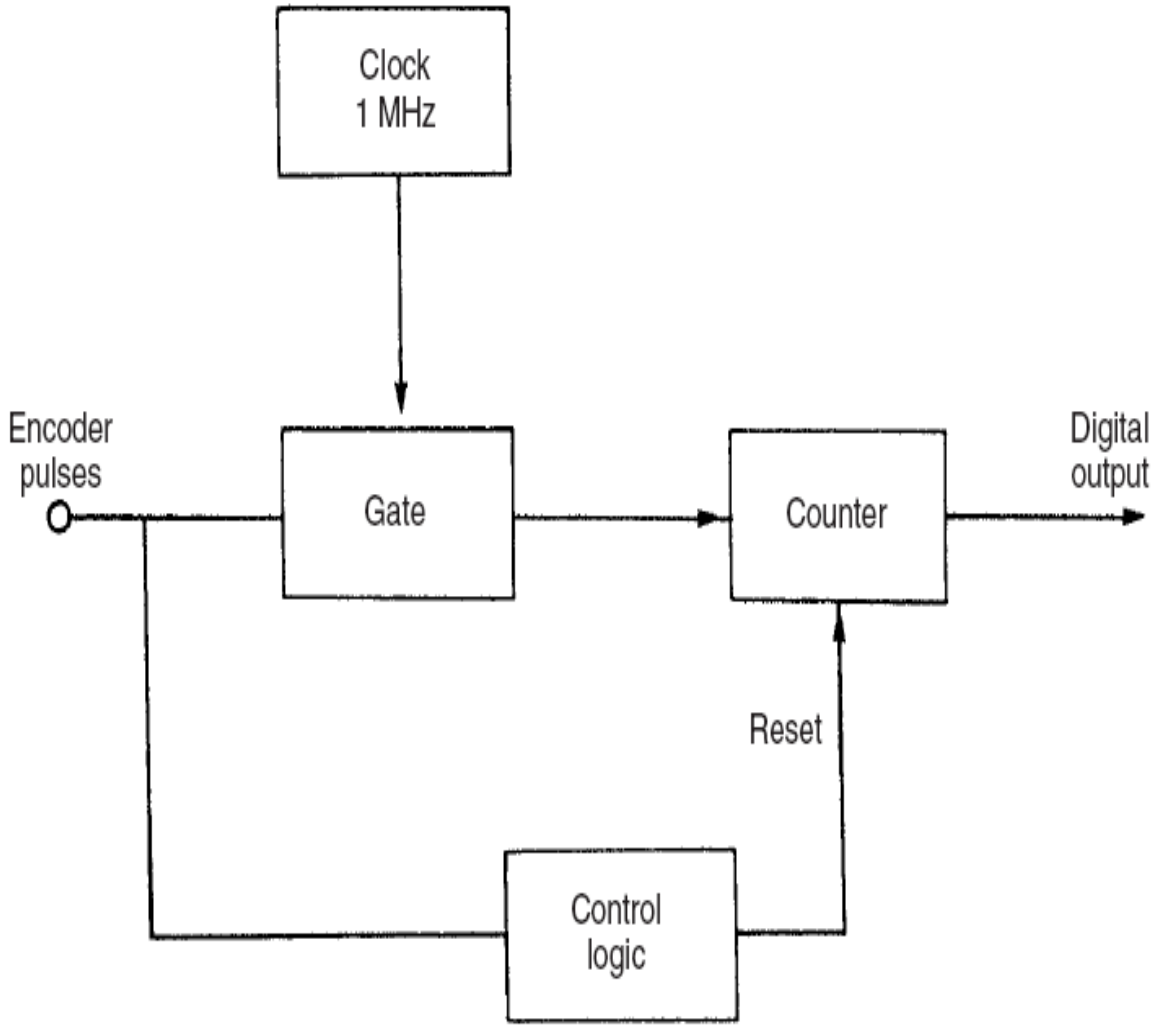


Figure 2 (Optical Sensor's Block Diagram)

2.1.2 Inductive sensing

Variable reluctance velocity transducers, also known as induction tachometers, are a form of digital tachometer that uses inductive sensing. They are widely used in automotive industry within anti-skid devices, anti-lock braking systems (ABS) and traction control. A more

sophisticated version shown in Figure. It has a rotating disc that is constructed from a bonded-fiber material into which soft iron poles are inserted at regular intervals around its periphery. The sensor consists of a permanent magnet with a shaped pole piece, which carries a wound coil. The distance between the pick-up and the outer perimeter of the disc is around 0.5 mm. As the disc rotates, the soft iron inserts on the disc move in turn past the pick-up unit. As each iron insert moves towards the pole piece, the reluctance of the magnetic circuit increases and hence the flux in the pole piece also increases. Similarly, the flux in the pole piece decreases as each iron inserts moves away from the sensor. The changing magnetic flux inside the pick-up coil causes a voltage to be induced in the coil whose magnitude is proportional to the rate of change of flux. This voltage is positive while the flux is increasing and negative while it is decreasing. Thus, the output is a sequence of positive and negative pulses whose frequency is proportional to the rotational velocity of the disc. The maximum angular velocity that the instrument can measure is limited to about 10000 rpm because of the finite width of the induced pulses. As the velocity increases, the distance between the pulses is reduced, and at a certain velocity, the pulses start to overlap. At this point, the pulse counter ceases to be able to distinguish the separate pulses. The optical tachometer has significant advantages in this respect, since the pulse width is much narrower, allowing measurement of higher velocities.

A simpler and cheaper form of variable reluctance transducer also exists that uses a ferromagnetic gear wheel in place of a fiber disc. The motion of the tip of each gear tooth towards and away from the pick-up unit causes a similar variation in the flux pattern to that produced by the iron inserts in the fiber disc. The pulses produced by these means are less sharp, however, and consequently the maximum angular velocity measurable is lower.

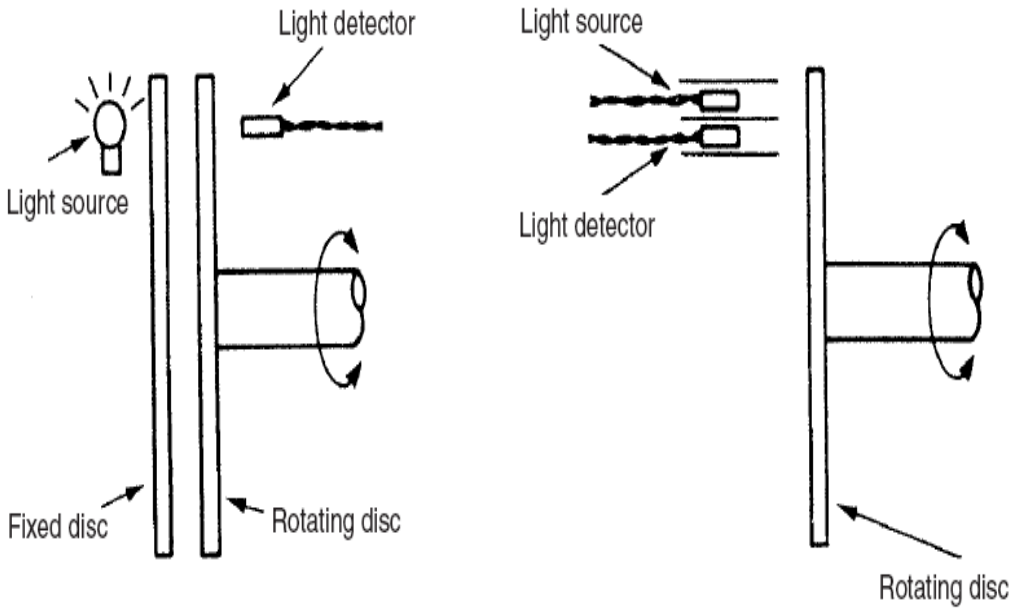


Figure 3(Optical Sensor)

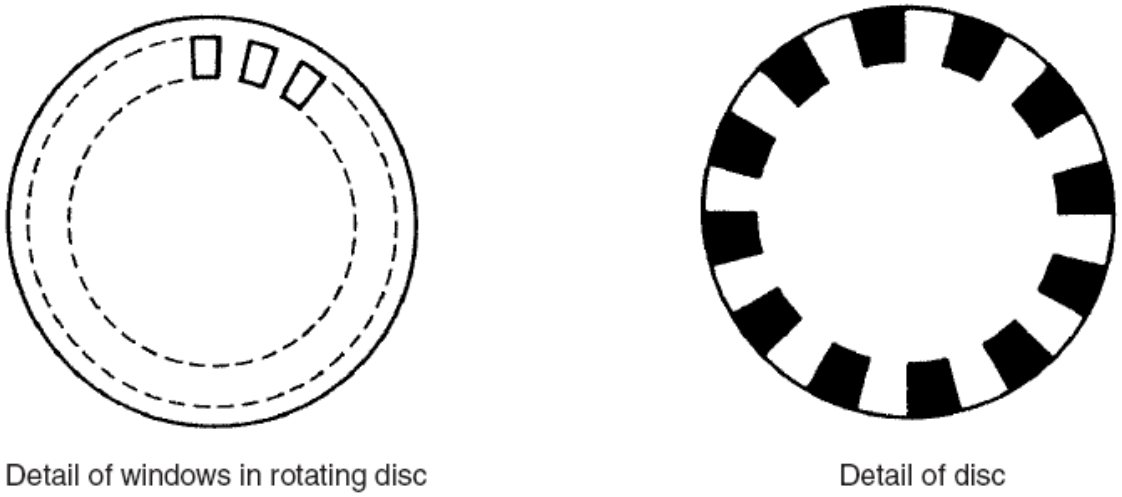


Figure 4(Electromagnetic sensor)

Output of the tachometer (magnetic pickup) is given by

$$E = bm w_r \sin(m w_r t)$$

b- amplitude of flux variation

m- number of teeth in the rotating wheel

w_r -angular velocity of the rotating wheel

Thus sinusoidal signal amplitude $E = bm w_r$ and frequency $f = m w_r / 2\pi$ are proportional to angular velocity of wheel.

However this output voltage comes in the range of mili volt . But the requirement of Data acquisition card is that input should be in the range of +/- 5 volt. So it need to be amplified prior to inputting it into Data acquisition card.

CHAPTER 3

Amplifier

3. AMPLIFIER

3.1 The instrumentation amplifier

An op-amp with no feedback is already a differential amplifier, amplifying the voltage difference between the two inputs. However, its gain cannot be controlled, and it is generally too high to be of any practical use. So far, our application of negative feedback to op-amps has resulting in the practical loss of one of the inputs, the resulting amplifier is only good for amplifying a single voltage signal input. With a little ingenuity, however, we can construct an op-amp circuit maintaining both voltages inputs, yet with a controlled gain set by external resistors. If all the resistor values are equal, this amplifier will have a differential voltage gain of 1.

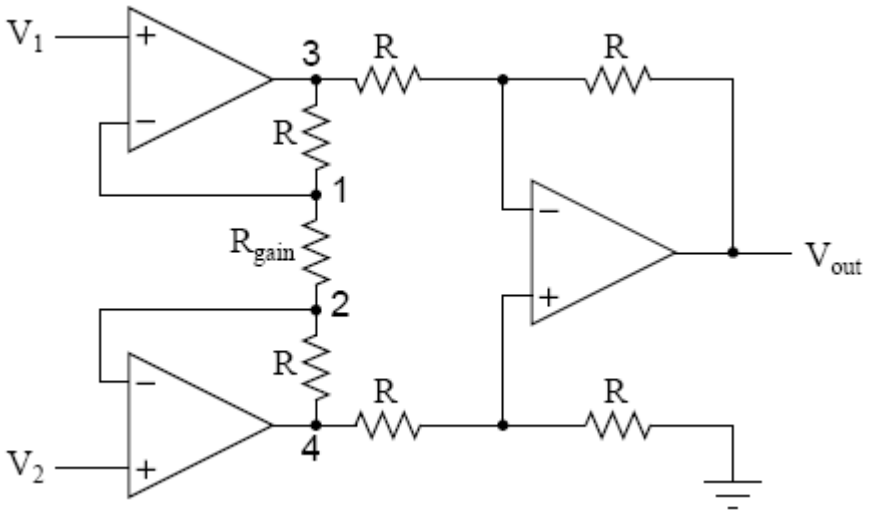


Figure 5

The analysis of this circuit is essentially the same as that of an inverting amplifier, except that the noninverting input (+) of the op-amp is at a voltage equal to a fraction of V2, rather than being connected directly to ground. As would stand to reason, V2 functions as the noninverting input

and V1 functions as the inverting input of the operational amplifier circuit. It is beneficial to be able to adjust the gain of the amplifier circuit without having to change more than one resistor value, as is necessary with the previous design of differential amplifier. The so-called instrumentation builds on the last version of differential amplifier to give us that capability.

This intimidating circuit is constructed from a buffered differential amplifier stage with three new resistors linking the two buffer circuits together. Consider all resistors to be of equal value except for Rgain. The negative feedback of the upper-left op-amp causes the voltage at point 1 (top of Rgain) to be equal to V1. Likewise, the voltage at point 2 (bottom of Rgain) is held to a value equal to V2. This establishes a voltage drop across Rgain equal to the voltage difference between V1 and V2. That voltage drop causes a current through Rgain, and since the feedback loops of the two input op-amps draw no current, that same amount of current through Rgain must be going through the two .R. resistors above and below it. This produces a voltage drop between points 3 and 4 equal to:

$$V_{3-4} = (V_2 - V_1)(1 + 2R/R_{gain})$$

The regular differential amplifier on the right-hand side of the circuit then takes this voltage drop between points 3 and 4 and it and amplifies it by a gain of 1 (assuming again that all .R resistors are of equal value). Though this looks like a cumbersome way to build a differential amplifier, it has the distinct advantages of possessing extremely high input impedances on the V1 and V2 inputs (because they connect straight into the noninverting inputs of their respective op-amps), and adjustable gain that can be set by a single resistor. Manipulating the above formula a bit, we have a general expression for overall voltage gain in the instrumentation amplifier:

$$A_V = (1 + 2R/R_{gain})$$

Though it may not be obvious by looking at the schematic, we can change the differential gain of the instrumentation amplifier simply by changing the value of one resistor: Rgain. Yes, we could still change the overall gain by changing the values of some of the other resistors, but this would necessitate balanced resistor value changes for the circuit to remain symmetrical. The lowest gain possible with the above circuit is obtained with Rgain completely open (infinite resistance), and that gain value is 1.

We have used PSPICE software for simulation of the operational amplifier to achieve a gain which is suitable for our required purpose of amplification i.e. the gain required.

3.2 PSPICE:

PSPICE is a full-featured simulator for serious analog designers. Sophisticated, internal models allow you to simulate everything from high-frequency systems to low-power IC designs. Draw on the expansive library of models to create off-the-shelf parts, or create models for new devices. Fully explore the relationships in your design with “what if” scenarios before committing to final implementation.

We have used the ORCAD 10.0 for circuit simulation.

SIMULATED CIRCUIT

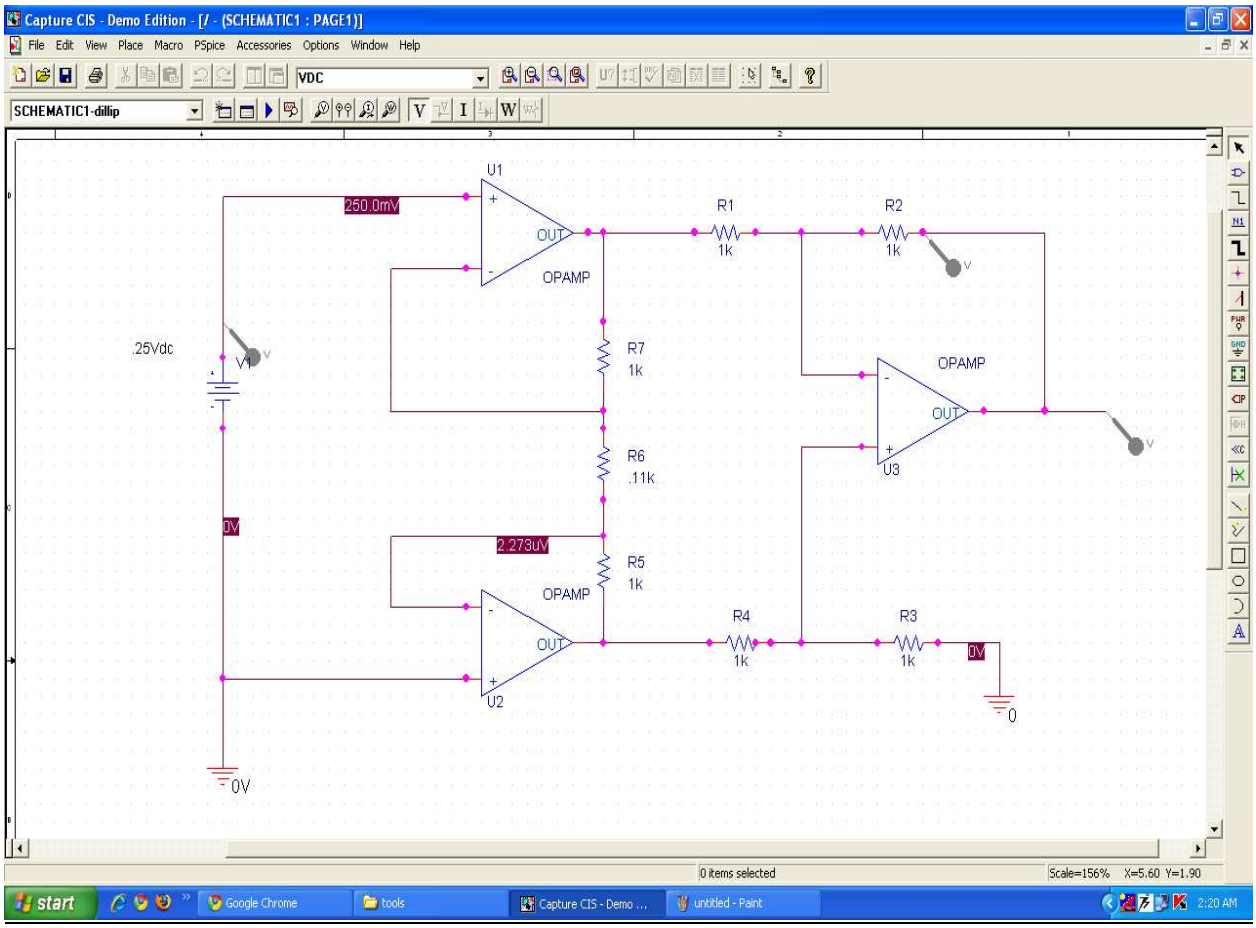


Figure 6

OUTPUT:

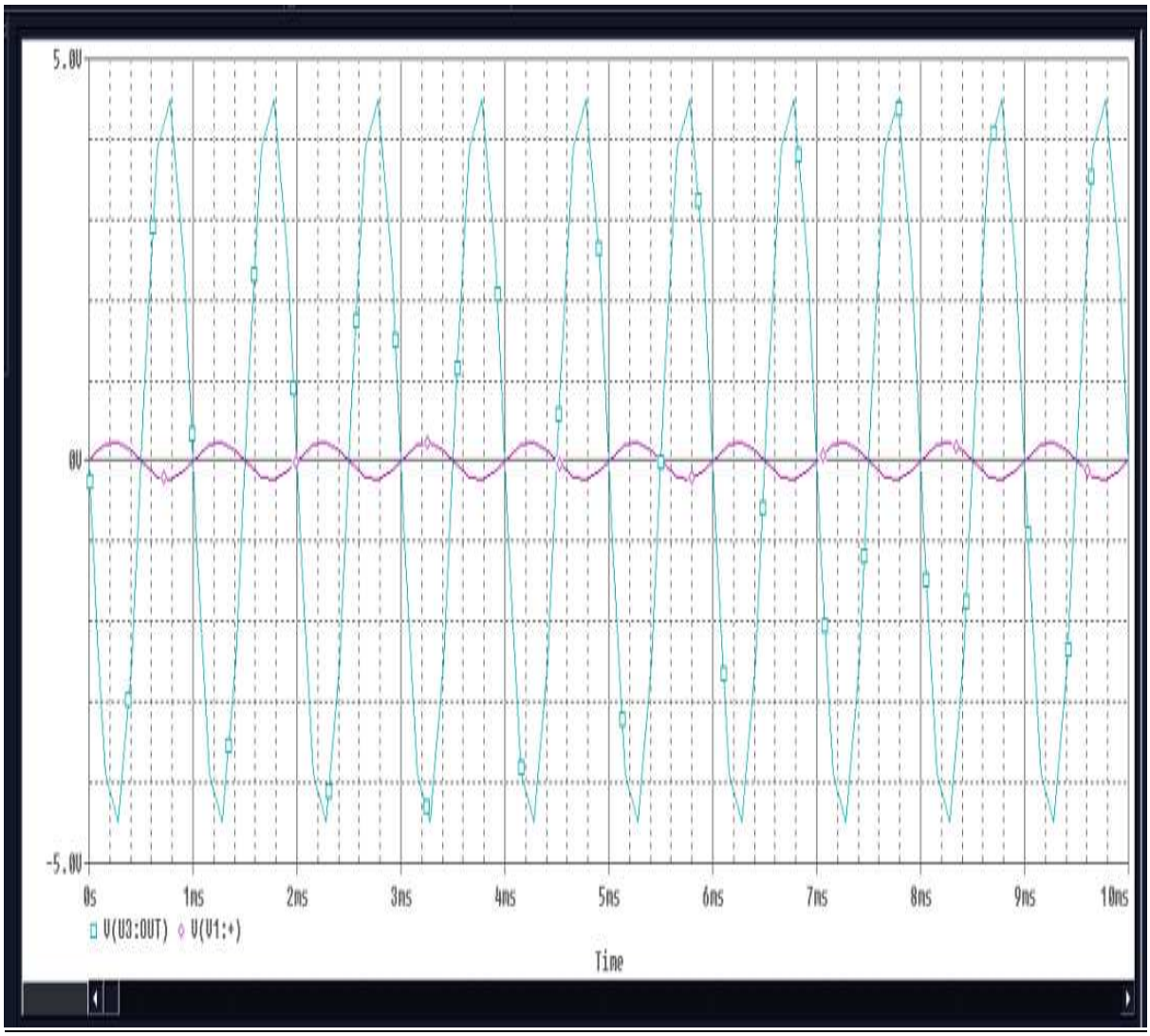


Figure 7

OBSERVAION TABLE

RPM (Photo reflective) Pick up	O/P voltage (Magnetic pick up) (in mv.)	Amplified O/P (in mv.)
250	55	825
330	72	986
350	76	1139
400	84	1257
530	110	1643
624	124	1858
705	137	2051
751	146	2185
845	159	2188
910	167	2471
960	175	2537
1052	187	2692
1106	194	2754
1140	199	2801
1215	206	2850
1270	212	2880
1325	219	2912
1378	224	2931
1440	230	2983
1495	235	2993
1530	238	2998
1600	244	3074
1675	254	3149
1755	256	3150

CHAPTER 4

Data acquisition using AT89c51

4. ACQUISTION SYSTEM USING AT89c51

AT89c51 the following important features:

This is an 8-bit microcontroller.

4kB masked ROM.

128 bytes internal data memory.

32 I/O lines

Internal UART (Universal Asynchronous Receiver Transmitter)

5 Interrupts including 2 external interrupts

Supports additional 60kB external program memory & 64kB external data memory

4.1 DESCRIPTION ABOUT 8051

1) ARCHITECTURE:-

1.1) Microprocessors and Microcontrollers:--

A digital computer typically consists of three major components: the Central Processing Unit (CPU), program and data memory, and an Input/output (I/O) system. The CPU controls the flow of information among the components of the computer. It also processes the data by performing digital operations. Most of the processing is done in the Arithmetic-Logic Unit (ALU) within the CPU. When the CPU of a computer is built on a single printed circuit board, the computer is called a minicomputer. A microprocessor is a CPU that is compacted into a single-chip semiconductor device. Microprocessors are general-purpose devices, suitable for many applications.

A computer built around a microprocessor is called a microcomputer.

The choice of I/O and memory devices of a microcomputer depends on the specific application. For example, most personal computers contain a keyboard and monitor as standard input and output devices. A microcontroller is an entire computer manufactured on a single chip.

PIN LAYOUT DIAGRAM OF 8051

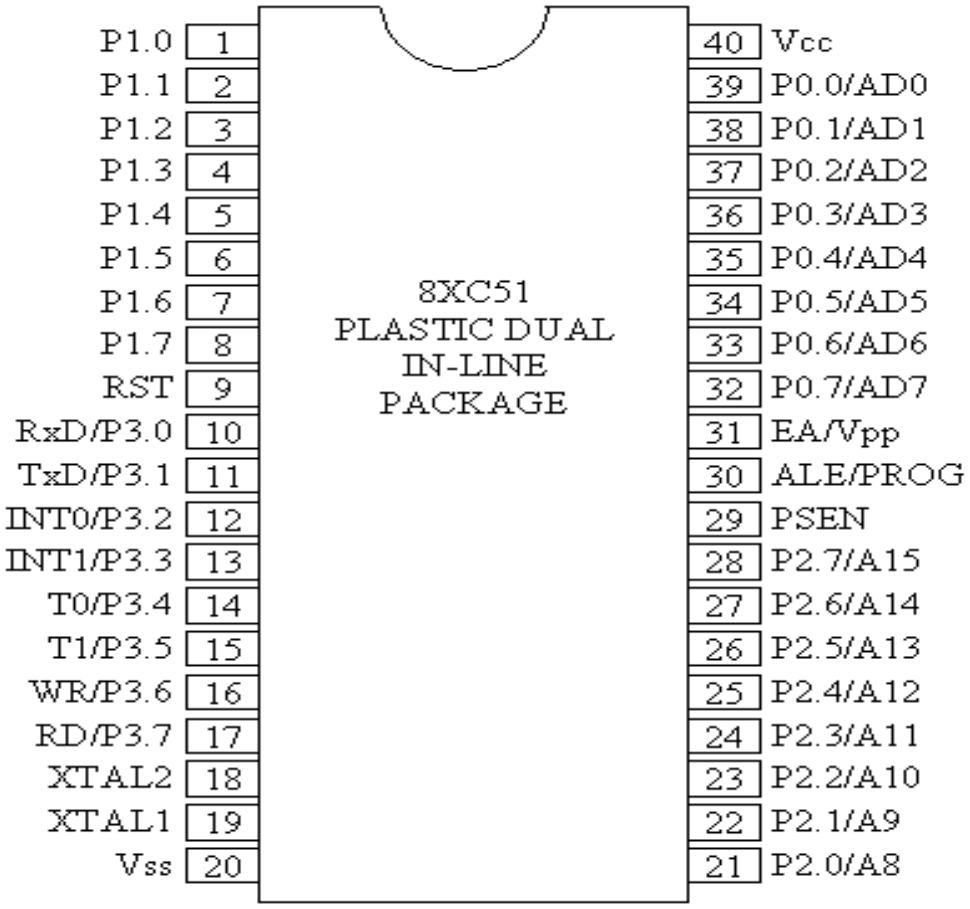


Figure 8(Pin Diagram of 8051)

Microcontrollers are usually dedicated devices embedded within an application. For example, microcontrollers are used as engine controllers in automobiles and as exposure and focus controllers in cameras. In order to serve these applications, they have a high concentration of on-chip facilities such as serial ports, parallel input/output ports, timers, counters; interrupt control, analog-to-digital converters, random access memory, read only memory, etc. The I/O, memory, and on-chip peripherals of a microcontroller are selected depending on the specifics of the target

application. Since microcontrollers are powerful digital processors, the degree of control and programmability they provide significantly enhances the effectiveness of the application.

The 8051 is the first microcontroller of the MCS-51 family introduced by Intel Corporation at the end of the 1970s. The 8051 family with its many enhanced members enjoys the largest market share, estimated to be about 40%, among the various microcontroller architectures. The architecture of the 8051 family of the microcontrollers is presented in this chapter. First, the original 8051 microcontroller is discussed, followed by the enhanced features of the 8032, and the 80C515.

1.2. The 8051 Microcontroller Family Architecture

The architecture of the 8051 family of microcontrollers is referred to as the MCS-51 architecture, or sometimes simply as MCS-51. The microcontrollers have an 8-bit data bus. They are capable of addressing 64K of program memory and a separate 64K of data memory. The 8051 has 4K of code memory implemented as on-chip *Read Only Memory* (ROM). The 8051 has 128 bytes of internal *Random Access* Memory (RAM). The 8051 has two timer/counters, a serial port, 4 general purpose parallel input/output ports, and interrupt control logic with five sources of interrupts.

Besides internal RAM, the 8051 has various *Special Function Registers* (SFR), which are the control and data registers for on-chip facilities. The SFRs also include the accumulator, the B register, and the *Program Status Word* (PSW), which contains the

CPU flags. Programming the various internal hardware facilities of the 8051 is achieved by placing the appropriate control words into the corresponding SFRs. The 8031 is similar to the 8051, except it lacks the on-chip ROM. As stated, the 8051 can address 64K of external data memory and 64K of external program memory. These may be separate blocks of memory, so that up to 128K of memory can be attached to the microcontroller. Separate blocks of code and data memory are referred to as the Harvard architecture. The 8051 has two separate read signals, RD# (P3.7) and PSEN#. The first is activated when a byte is to be read from external data memory, the other, from external program memory. Both of these signals are so-called active low signals. That is, they are cleared to logic level 0 when activated. All external code is fetched from external program memory. In addition, bytes from external program memory may be read

by special read instructions such as the MOVC instruction. There are separate instructions to read from external data memory, such as the MOVX instruction. That is, the instructions determine which block of memory is addressed, and the corresponding control signal, either RD# or PSEN# is activated during the memory read cycle. A single block of memory may be mapped to act as both data and program memory. This is referred to as the Von Neumann1 architecture. In order to read from the same block using either the RD# signal or the PSEN# signal, the two signals are combined with a logic AND operation.

This way, the output of the AND gate is low when either input is low. The advantage of the Harvard architecture is not simply doubling the memory capacity of the microcontroller. Separating program and data increases the reliability of the microcontroller, since there are no instructions to write to the program memory. A ROM device is ideally suited to serve as program memory. The Harvard architecture is somewhat awkward in evaluation systems, where code needs to be loaded into program memory. By adopting the Von Neumann architecture, code may be written to memory as data bytes, and then executed as program instructions.

During the past decade, many manufacturers introduced enhanced members of the 8051 microcontroller. The enhancements include more memory, more ports, analog to-digital converters, more timers with compare, reload and capture facilities, more interrupt sources, higher precision multiply and divide units, idle and power down mode support, watchdog timers, and network communication subsystems. All microcontroller of the family use the same set of machine instructions, the MCS-51.

4.2 ADC 0808CCN

In lot of embedded systems micro controllers needs to take analog input. Most of the sensors and transducers such as temperature, humidity, pressure, are analog. For interfacing these sensors to micro controllers we require to convert the analog output of these sensors to digital so that the controller can read it. Some micro controllers have built in Analog to Digital Converter (ADC) so there is no need of external ADC. For controllers that don't have internal ADC external ADC is used.

One of the most commonly used ADC is ADC0808. ADC 0808 is a Successive approximation type with 8 channels i.e. it can directly access 8 single ended analog signals

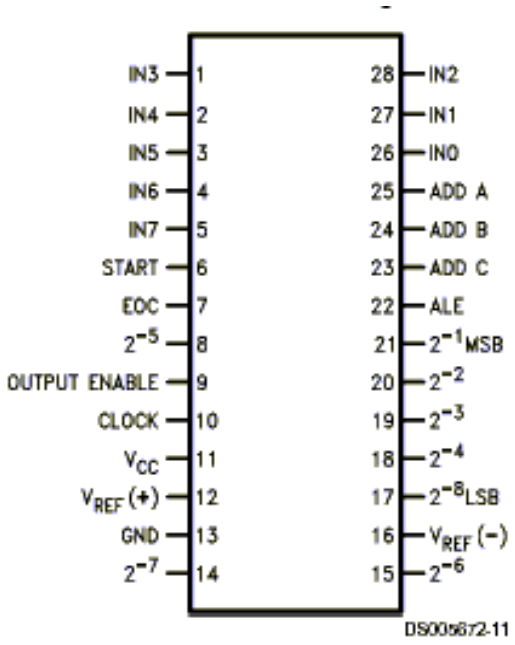


Figure 9(Pin Diagram of ADC0808)

I/O Pins

Analog Channel	ADDRESS LINES		
	C	B	A
IN0	0	0	0
IN1	0	0	1
IN2	0	1	0
IN3	0	1	1
IN4	1	0	0
IN5	1	0	1
IN6	1	1	0
IN7	1	1	1

- ***ADDRESS LINE A, B, C***

The device contains 8-channels. A particular channel is selected by using the address decoder line. The TABLE 1 shows the input states for address lines to select any channel.

- ***Address Latch Enable ALE***

The address is latched on the Low – High transition of ALE.

- ***START***

The ADC's Successive Approximation Register (SAR) is reset on the positive edge i.e. Low-High of the Start Conversion pulse. Whereas the conversion is begun on the falling edge i.e. High – Low of the pulse.

- ***Output Enable***

Whenever data has to be read from the ADC, Output Enable pin has to be pulled high thus enabling the TRI-STATE outputs, allowing data to be read from the data pins D0-D7.

- ***End of Conversion (EOC)***

This Pin becomes High when the conversion has ended, so the controller comes to know that the data can now be read from the data pins.

- ***Clock***

External clock pulses are to be given to the ADC; this can be given either from LM 555 in Astable mode or the controller can also be used to give the pulses.

Vref/2 (Volts)	Vin (Volts)	Step size (mV)
Open (2.5)	0 to 5	5/256 = 19.53
2.56	0 to 5.12	5.12/256 =20
1.28	0 to 2.56	2.56/256 = 10
0.5	0 to 1	1/256=3.90

Data Out

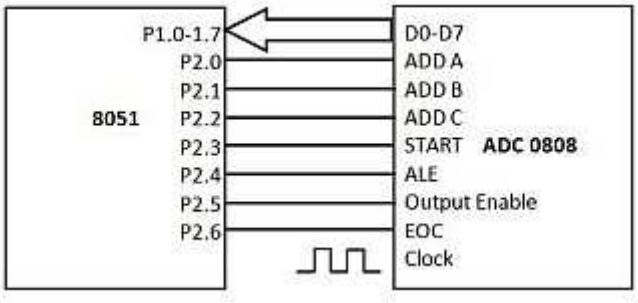
Dout = Vin / Step Size

For input vtg. of 2.56 volts (Vref=1.28 volts) and step size of 10mv Dout =2560/10 =256 or FF that is full scale output.

Resolution

8 bits for ADC0808

Algorithm



1. Start.
2. Select the channel.
3. A Low – High transition on ALE to latch in the address.
4. A Low – High transition on Start to reset the ADC's SAR.
5. A High – Low transition on ALE.
6. A High – Low transition on start to start the conversion.
7. Wait for End of cycle (EOC) pin to become high.
8. Make Output Enable pin High.
9. Take Data from the ADC's output
10. Make Output Enable pin Low.
11. Stop

The total numbers of lines required are:

- data lines: 8
- ALE: 1
- START: 1
- EOC:1
- Output Enable:1

I.e. total 12 lines. You can directly connect the OE pin to $V_{cc.}$ Moreover instead of polling for EOC just put some delay so instead of 12 lines you will require 10 lines.

You can also provide the clock through the controller thus eliminating the need of external circuit for clock.

Timing Diagram

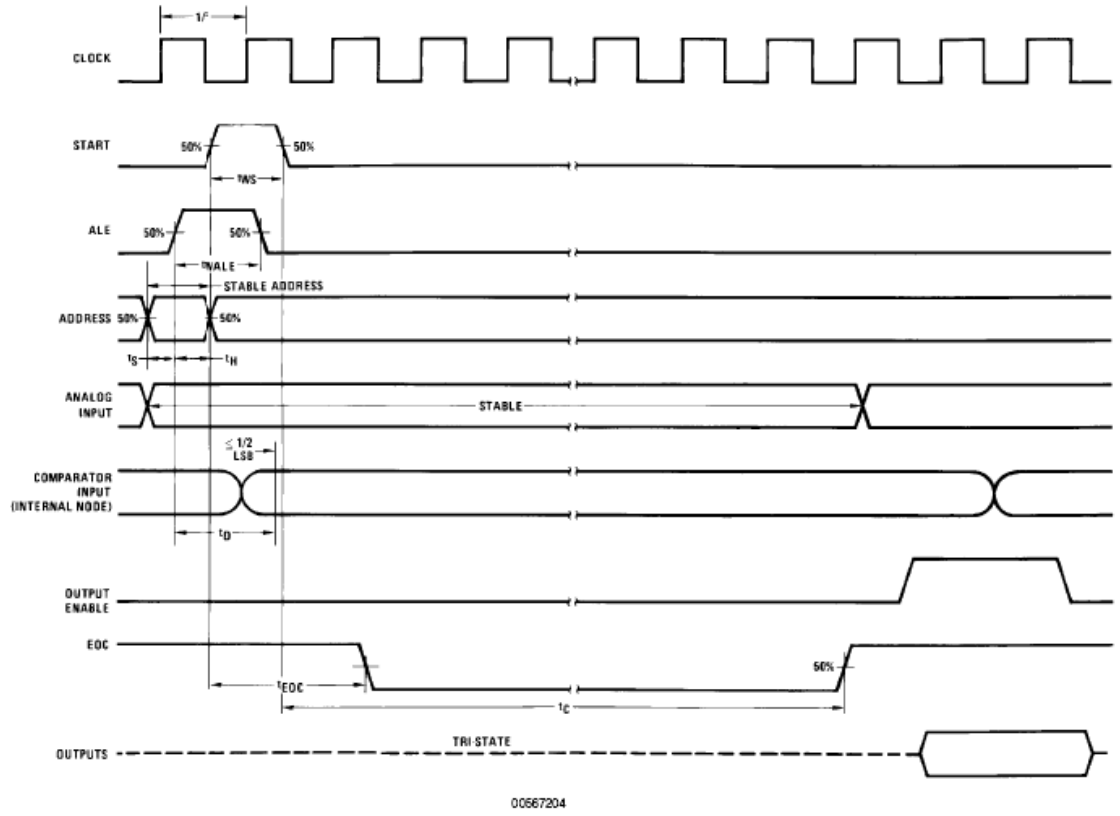


Figure 10

ADC OUTPUT :

SL NO	**VOLTAGE(V1=V*20) IN VOLTS.**	**Digital OUTPUT(8BITRESO) FROM ADC0808(DECIMAL)**
1	3.074	157
2	2.912	149
3	2.850	146
4	2.800	143
5	2.692	138
6	2.188	112
7	2.051	105
8	1.257	65
9	0.825	42

Where V = analog output of Electromagnetic Sensor

4.3 555 TIMER

The 555 monolithic timing circuits is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA.

PIN DETAILS OF 555 TIMER:

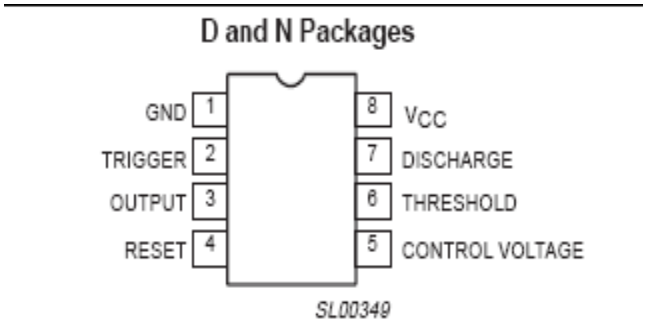


Figure 11

- **Pin 1 (Ground)**: The ground (or common) pin is the most-negative supply potential of the device, which is normally connected to circuit common (ground) when operated from positive supply voltages.

- **Pin 2 (Trigger):** This pin is the input to the lower comparator and is used to set the latch, which in turn causes the output to go high. This is the beginning of the timing sequence in

monostable operation. Triggering is accomplished by taking the pin from above to below a voltage level of 1/3 V+ (or, in general, one-half the voltage appearing at pin 5). The action of the trigger input is level-sensitive, allowing slow rate-of-change waveforms, as well as pulses, to be used as trigger sources. The trigger pulse must be of shorter duration than the time interval determined by the external R and C. If this pin is held low longer than that, the output will remain high until the trigger input is driven high again. One precaution that should be observed with the trigger input signal is that it must not remain lower than 1/3 V+ for a period of time longer than the timing cycle. If this is allowed to happen, the timer will re-trigger itself upon termination of the first output pulse. Thus, when the timer is driven in the monostable mode with input pulses longer than the desired output pulse width, the input trigger should effectively be shortened by differentiation. The minimum-allowable pulse width for triggering is somewhat dependent upon pulse level, but in general if it is greater than the 1uS (micro-Second), triggering will be reliable. A second precaution with respect to the trigger input concerns storage time in the lower comparator. This portion of the circuit can exhibit normal turn-off delays of several microseconds after triggering; that is, the latch can still have a trigger input for this period of time after the trigger pulse. In practice, this means the minimum monostable output pulse width should be in the order of 10uS to prevent possible double triggering due to this effect. The voltage range that can safely be applied to the trigger pin is between V+ and ground. A dc current, termed the trigger current, must also flow from this terminal into the external circuit. This current is typically 500nA (nano-amp) and will define the upper limit of resistance allowable from pin 2 to ground. For an astable configuration operating at V+ = 5 volts, this resistance is 3 Mega-ohm; it can be greater for higher V+ levels.

Pin 3 (Output): The output of the 555 comes from a high-current totem-pole stage made up of transistors Q20 - Q24. Transistors Q21 and Q22 provide drive for source-type loads, and their Darlington connection provides a high-state output voltage about 1.7 volts less than the V+ supply level used. Transistor Q24 provides current-sinking capability for low-state loads referred to V+ (such as typical TTL inputs). Transistor Q24 has a low saturation voltage, which allows it to interface directly, with good noise margin, when driving current-sinking logic. Exact output saturation levels vary markedly with supply voltage, however, for both high and low states. At a

V+ of 5 volts, for instance, the low state Vce(sat) is typically 0.25 volts at 5 mA. Operating at 15 volts, however, it can sink 200mA if an output-low voltage level of 2 volts is allowable (power dissipation should be considered in such a case, of course). High-state level is typically 3.3 volts at V+ = 5 volts; 13.3 volts at V+ = 15 volts. Both the rise and fall times of the output waveform are quite fast, typical switching times being 100nS. The state of the output pin will always reflect the inverse of the logic state of the latch, and this fact may be seen by examining Fig. 3. Since the latch itself is not directly accessible, this relationship may be best explained in terms of latch-input trigger conditions. To trigger the output to a high condition, the trigger input is momentarily taken from a higher to a lower level. [see "Pin 2 - Trigger"]. This causes the latch to be set and the output to go high. Actuation of the lower comparator is the only manner in which the output can be placed in the high state. The output can be returned to a low state by causing the threshold to go from a lower to a higher level [see "Pin 6 - Threshold"], which resets the latch. The output can also be made to go low by taking the reset to a low state near ground [see "Pin 4 - Reset"]. The output voltage available at this pin is approximately equal to the Vcc applied to pin 8 minus 1.7V.

Pin 4 (Reset): This pin is also used to reset the latch and return the output to a low state. The reset voltage threshold level is 0.7 volt, and a sink current of 0.1mA from this pin is required to reset the device. These levels are relatively independent of operating V+ level; thus the reset input is TTL compatible for any supply voltage. The reset input is an overriding function; that is, it will force the output to a low state regardless of the state of either of the other inputs. It may thus be used to terminate an output pulse prematurely, to gate oscillations from "on" to "off", etc. Delay time from reset to output is typically on the order of 0.5 μS, and the minimum reset pulse width is 0.5 μS. Neither of these figures is guaranteed, however, and may vary from one manufacturer to another. In short, the reset pin is used to reset the flip-flop that controls the state of output pin 3. The pin is activated when a voltage level anywhere between 0 and 0.4 volt is applied to the pin. The reset pin will force the output to go low no matter what state the other inputs to the flip-flop are in. When not used, it is recommended that the reset input be tied to V+ to avoid any possibility of false resetting.

Pin 5 (Control Voltage) :This pin allows direct access to the 2/3 V+ voltage-divider point, the reference level for the upper comparator. It also allows indirect access to the lower comparator, as there is a 2:1 divider (R8 - R9) from this point to the lower-comparator reference input, Q13. Use of this terminal is the option of the user, but it does allow extreme flexibility by permitting modification of the timing period, resetting of the comparator, etc. When the 555 timer is used in a voltage-controlled mode, its voltage-controlled operation ranges from about 1 volt less than V+ down to within 2 volts of ground (although this is not guaranteed). Voltages can be safely applied outside these limits, but they should be confined within the limits of V+ and ground for reliability. By applying a voltage to this pin, it is possible to vary the timing of the device independently of the RC network. The control voltage may be varied from 45 to 90% of the Vcc in the monostable mode, making it possible to control the width of the output pulse independently of RC. When it is used in the astable mode, the control voltage can be varied from 1.7V to the full Vcc. Varying the voltage in the astable mode will produce a frequency modulated (FM) output. In the event the control-voltage pin is not used, it is recommended that it be bypassed, to ground, with a capacitor of about 0.01uF (10nF) for immunity to noise, since it is a comparator input. This fact is not obvious in many 555 circuits since I have seen many circuits with 'no-pin-5' connected to anything, but this is the proper procedure. The small ceramic cap may eliminate false triggering.

- **Pin 6 (Threshold):** Pin 6 is one input to the upper comparator (the other being pin 5) and is used to reset the latch, which causes the output to go low. Resetting via this terminal is accomplished by taking the terminal from below to above a voltage level of 2/3 V+ (the normal voltage on pin 5). The action of the threshold pin is level sensitive, allowing slow rate-of-change waveforms. The voltage range that can safely be applied to the threshold pin is between V+ and ground. A dc current, termed the threshold current, must also flow into this terminal from the external circuit. This current is typically 0.1μA, and will define the upper limit of total resistance allowable from pin 6 to V+. For either timing configuration operating at V+ = 5 volts, this resistance is 16 Mega-ohm. For 15 volt operation, the maximum value of resistance is 20 MegaOhms.

- **Pin 7 (Discharge):** This pin is connected to the open collector of a npn transistor (Q14), the emitter of which goes to ground, so that when the transistor is turned "on", pin 7 is effectively shorted to ground. Usually the timing capacitor is connected between pin 7 and ground and is discharged when the transistor turns "on". The conduction state of this transistor is identical in timing to that of the output stage. It is "on" (low resistance to ground) when the output is low and "off" (high resistance to ground) when the output is high. In both the monostable and astable time modes, this transistor switch is used to clamp the appropriate nodes of the timing network to ground. Saturation voltage is typically below 100mV (milli-Volt) for currents of 5mA or less, and off-state leakage is about 20nA (these parameters are not specified by all manufacturers, however). Maximum collector current is internally limited by design, thereby removing restrictions on capacitor size due to peak pulse-current discharge. In certain applications, this open collector output can be used as an auxiliary output terminal, with current-sinking capability similar to the output (pin 3).

- **Pin 8 (V +):** The V+ pin (also referred to as Vcc) is the positive supply voltage terminal of the 555 timer IC. Supply-voltage operating range for the 555 is +4.5 volts (minimum) to +16 volts (maximum), and it is specified for operation between +5 volts and +15 volts. The device will operate essentially the same over this range of voltages without change in timing period. Actually, the most significant operational difference is the output drive capability, which increases for both current and voltage range as the supply voltage is increased. Sensitivity of time interval to supply voltage change is low, typically 0.1% per volt. There are special and military devices available that operate at voltages as high as 18 volts.

Operating Modes: The 555 timer has two basic operational modes: one shot and astable.

One-shot multivibrators are used for turning some circuit or external component on or off for a specific length of time. It is also used to generate delays. When multiple one-shots are cascaded, a variety of sequential timing pulses can be generated. Those pulses will allow you to time and sequence a number of related operations. The other basic operational mode of the 555 is as and astable multivibrator. An astable multivibrator is simply and oscillator. The astable multivibrator

generates a continuous stream of rectangular off-on pulses that switch between two voltage levels. The frequency of the pulses and their duty cycle are dependent upon the RC network values.

One-Shot Operation: Fig. 4 shows the basic circuit of the 555 connected as a monostable multivibrator. An external RC network is connected between the supply voltage and ground. The junction of the resistor and capacitor is connected to the threshold input which is the input to the upper comparator. The internal discharge transistor is also connected to the junction of the resistor and the capacitor. An input trigger pulse is applied to the trigger input, which is the input to the lower comparator.With that circuit configuration; the control flip-flop is initially reset. Therefore, the output voltage is near zero volts. The signal from the control flip-flop causes T1 to conduct and act as a short circuit across the external capacitor. For that reason, the capacitor cannot charge. During that time, the input to the upper comparator is near zero volts causing the comparator output to keep the control flip-flop reset.

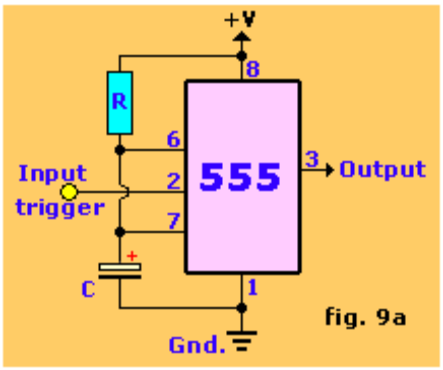


Figure 12

Notice how the monostable continues to output its pulse regardless of the inputs swing back up. That is because the output is only triggered by the input pulse, the output actually depends on the capacitor charge.

Monostable Mode: The 555 in fig. 9a is shown here in it's utmost basic mode of operation; as a triggered monostable. One immediate observation is the extreme simplicity of this circuit. Only two components to make up a timer, a capacitor and a resistor. And for noise immunity maybe a capacitor on pin 5. Due to the internal latching mechanism of the 555, the timers will always time-out once triggered, regardless of any subsequent noise (such as bounce) on the input trigger

(pin 2). This is a great asset in interfacing the 555 with noisy sources. Just in case you don't know what 'bounce' is: bounce is a type of fast, short term noise caused by a switch, relay, etc. and then picked up by the input pin. The trigger input is initially high (about 1/3 of +V). When a negative-going trigger pulse is applied to the trigger input (see fig. 9a), the threshold on the lower comparator is exceeded. The lower comparator, therefore, sets the flip-flop. That causes T1 to cut off, acting as an open circuit. The setting of the flip-flop also causes a positive-going output level which is the beginning of the output timing pulse. The capacitor now begins to charge through the external resistor. As soon as the charge on the capacitor equal 2/3 of the supply voltage, the upper comparator triggers and resets the control flip-flop. That terminates the output pulse which switches back to zero. At this time, T1 again conducts thereby discharging the capacitor. If a negative-going pulse is applied to the reset input while the output pulse is high, it will be terminated immediately as that pulse will reset the flip-flop. Whenever a trigger pulse is applied to the input, the 555 will generate its single-duration output pulse. Depending upon the values of external resistance and capacitance used, the output timing pulse may be adjusted from approximately one millisecond to as high as on hundred seconds. For time intervals less than approximately 1-millisecond, it is recommended that standard logic one-shots designed for narrow pulses be used instead of a 555 timer. IC timers are normally used where long output pulses are required. In this application, the duration of the output pulse in seconds is approximately equal to:

$T = 1.1 \times R \times C$ (in seconds).

The output pulse width is defined by the above formula and with relatively few restrictions, timing components R(t) and C(t) can have a wide range of values. There is actually no theoretical upper limit on T (output pulse width), only practical ones. The lower limit is 10uS. You may consider the range of T to be 10uS to infinity, bounded only by R and C limits. Special R(t) and C(t) techniques allow for timing periods of days, weeks, and even months if so desired. However, a reasonable lower limit for R(t) is in the order of about 10Kilo ohm, mainly from the standpoint of power economy. (Although R(t) can be lower that 10K without harm, there is no need for this from the standpoint of achieving a short pulse width.) A practical minimum for C(t) is about 95pF; below this the stray effects of capacitance become noticeable, limiting accuracy and predictability. Since it is obvious that the product of these two minimums yields a T that is

less the 10uS, there is much flexibility in the selection of R(t) and C(t). Usually C(t) is selected first to minimize size (and expense); then R(t) is chosen. The upper limit for R(t) is in the order of about 15 Mega ohm but should be less than this if all the accuracy of which the 555 is capable is to be achieved. The absolute upper limit of R(t) is determined by the threshold current plus the discharge leakage when the operating voltage is +5 volt. For example, with a threshold plus leakage current of 120nA, this gives a maximum value of 14M for R(t) (very optimistic value). Also, if the C(t) leakage current is such that the sum of the threshold current and the leakage current is in excess of 120 nA the circuit will never time-out because the upper threshold voltage will not be reached. Therefore, it is good practice to select a value for R(t) so that, with a voltage drop of 1/3 V+ across it, the value should be 100 times more, if practical.

So, it should be obvious that the real limit to be placed on C (t) is its leakage, not it's capacitance value, since larger-value capacitors have higher leakages as a fact of life. Low-leakage types, like tantalum or NPO, are available and preferred for long timing periods. Sometimes input trigger source conditions can exist that will necessitate some type of signal conditioning to ensure compatibility with the triggering requirements of the 555. This can be achieved by adding another capacitor, one or two resistors and a small signal diode to the input to form a pulse differentiator to shorten the input trigger pulse to a width less than 10uS (in general, less than T). Their values and criterion are not critical; the main one is that the width of the resulting differentiated pulse (after C) should be less than the desired output pulse for the period of time it is below the 1/3 V+ trigger level.

There are several different types of 555 timers. The LM555 from National is the most common one these days, in my opinion. The Exar XR-L555 timer is a micro power version of the standard 555 offering a direct, pin-for-pin (also called plug-compatible) substitute device with an advantage of a lower power operation. It is capable of operation of a wider range of positive supply voltage from as low as 2.7volt minimum up to 18 volts maximum. At a supply voltage of +5V, the L555 will typically dissipate of about 900 microwatts, making it ideally suitable for battery operated circuits. The internal schematic of the L555 is very much similar to the standard 555 but with additional features like 'current spiking' filtering, lower output drive capability, higher nodal impedances, and better noise reduction system.

Maxim's ICM7555, and Sanyo's LC7555 models are a low-power, general purpose CMOS design version of the standard 555, also with a direct pin-for-pin compatibility with the regular 555. It's advantages are very low timing/bias currents, low power-dissipation operation and an even wider voltage supply range of as low as 2.0 volts to 18 volts. At 5 volts the 7555 will dissipate about 400 microwatts, making it also very suitable for battery operation. The internal schematic of the 7555 (not shown) is however totally different from the normal 555 version because of the different design process with cmos technology. It has much higher input impedances than the standard bipolar transistors used. The cmos version removes essentially any timing component restraints related to timer bias currents, allowing resistances as high as practical to be used.

This very versatile version should be considered where a wide range of timing is desired, as well as low power operation and low current synching appears to be important in the particular design.

Some of the less desirable properties of the regular 555 are high supply current, high trigger current, double output transitions, and inability to run with very low supply voltages. These problems have been remedied in a collection of CMOS successors.

A caution about the regular 555 timer chips; the 555, along with some other timer ic's, generates a big (about 150mA) supply current glitch during each output transition. Be sure to use a hefty bypass capacitor over the power connections near the timer chip. And even so, the 555 may have a tendency to generate double output transitions.

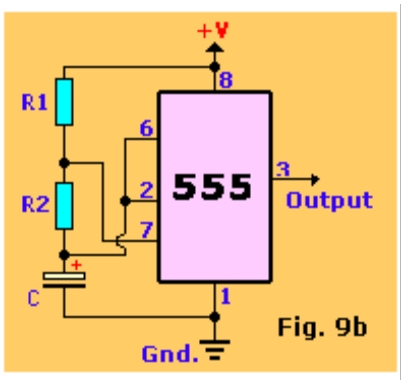


Figure 13

***Astable operation**:* Figure 9b shows the 555 connected as an astable multivibrator. Both the trigger and threshold inputs (pins 2 and 6) to the two comparators are connected together and to the external capacitor. The capacitor charges toward the supply voltage through the two resistors, R1 and R2. The discharge pin (7) connected to the internal transistor is connected to the junction of those two resistors.

When power is first applied to the circuit, the capacitor will be uncharged; therefore, both the trigger and threshold inputs will be near zero volts (see Fig. 10). The lower comparator sets the control flip-flop causing the output to switch high. That also turns off transistor T1. That allows the capacitor to begin charging through R1 and R2. As soon as the charge on the capacitor reaches 2/3 of the supply voltage, the upper comparator will trigger causing the flip-flop to reset. That causes the output to switch low. Transistor T1 also conducts. The effect of T1 conducting causes resistor R2 to be connected across the external capacitor. Resistor R2 is effectively connected to ground through internal transistor T1. The result of that is that the capacitor now begins to discharge through R2.

The only difference between the single 555, dual 556, and quad 558 (both 14-pin types), is the common power rail. For the rest everything remains the same as the single version, 8-pin 555.

As soon as the voltage across the capacitor reaches 1/3 of the supply voltage, the lower comparator is triggered. That again causes the control flip-flop to set and the output to go high. Transistor T1 cuts off and again the capacitor begins to charge. That cycle continues to repeat with the capacitor alternately charging and discharging, as the comparators cause the flip-flop to be repeatedly set and reset. The resulting output is a continuous stream of rectangular pulses.

The frequency of operation of the astable circuit is dependent upon the values of R1, R2, and C. The frequency can be calculated with the formula:

$f = 1/(.693 \times C \times (R1 + 2 \times R2))$

The Frequency f is in Hz, R1 and R2 are in ohms, and C is in farads. The time duration between pulses is known as the 'period', and usually designated with a 't'. The pulse is on for t1 seconds, then off for t2 seconds. The total period (t) is t1 + t2 (see fig. 10). That time interval is related to the frequency by the familiar relationship:

$f = 1/t$ or $t = 1/f$

The time intervals for the on and off portions of the output depend upon the values of R1 and R2. The ratio of the time duration when the output pulse is high to the total period is known as the duty-cycle. The duty-cycle can be calculated with the formula:

$D = t1/t = (R1 + R2) / (R1 + 2R2)$

You can calculate t1 and t2 times with the formulas below:

$t1 = .693(R1+R2)C$

$t2 = .693 \times R2 \times C$

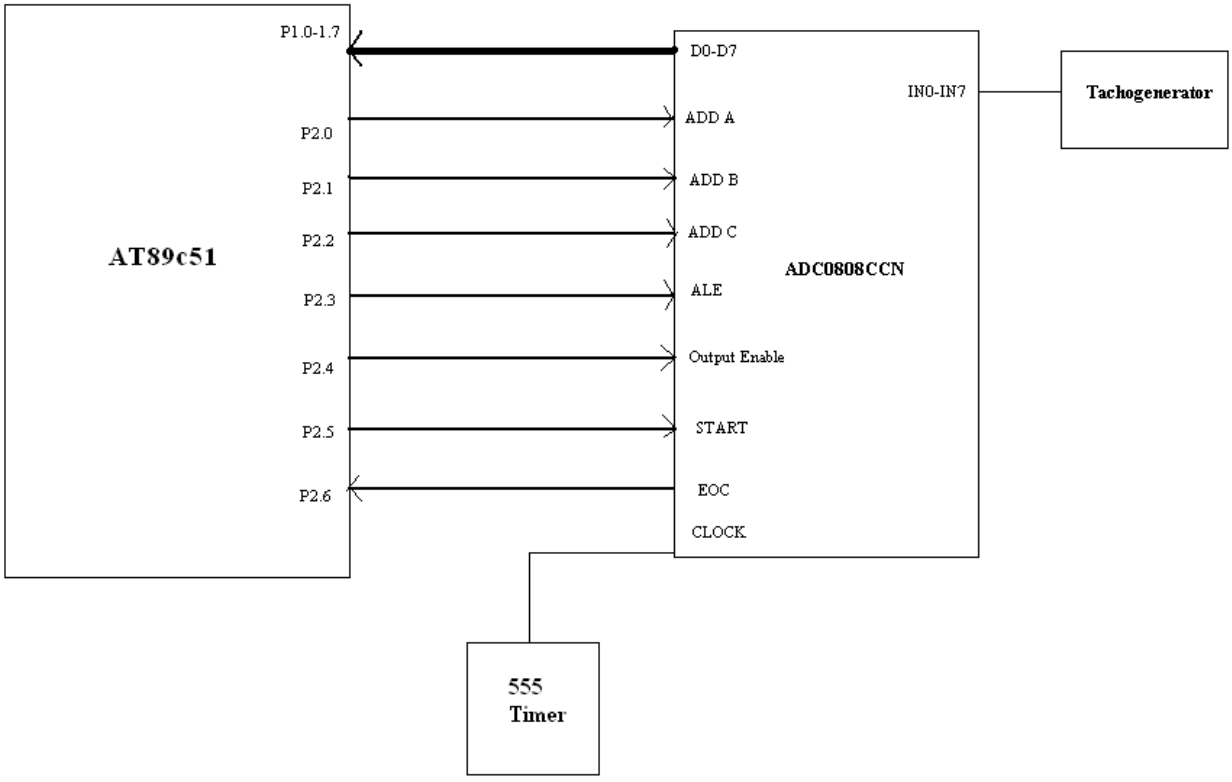
The 555, when connected as shown in Fig. 9b, can produce duty-cycles in the range of approximately 55 to 95%. A duty-cycle of 80% means that the output pulse is on or high for 80% of the total period. The duty-cycle can be adjusted by varying the values of R1 and R2.

CHAPTER 5

Adc interfacing with 8051 and 555 timer

5.
ADC INTERFACING WITH 8051 MICROCONTROLLER AND 555 TIMER

INTERFACING OF ADC AND 8051 MICROCONTROLLER USING 555 TIMER:



General Circuit Diagram of Final Working Model Diagram

Figure 14

WORKING:

1. As the output obtained from Electromagnetic sensor is in the range of mV range so an amplifier of gain 20 is used to convert the analog voltage obtained from sensor into 5V

range.

2. Now the Voltage obtained is applied to input terminal of ADC.
3. The working of ADC is tested .
4. Port of 8051 microcontroller was programmed in Assembly language (as shown in the program):

```
PROGRAM:
        ADC_A     P2.0
        ADC_B     P2.1
        ADC_C     P2.2
        ALE       P2.3
        OE        P2.4
        EOC       P2.6
        ORG 0000H
        MOV P1,#0FFH
        MOV P,#00H
        CLR  ALE
        CLR  START
        CLR  OE
        SETB  EOC
INIT: CLR ADC_A
        CLR ADC_B
        CLR ADC_C
        CALL DELAY_SMALL
        SETB  ALE
        CALL  DELAY_SMALL
        SETB START
        CALL DELAY_SMALL
        CLR ALE
        CLR  START
        CALL  DELAY_LONG
```

```
WAIT : JNB  EOC,WAIT
       SETB  OE
       CALL  DELAY_SMALL
       MOV A, P1
       MOV P0,A
       SJMP INIT
DELAY_SMALL: MOV R0,#10
             NOP
             NOP
             DJNZ R0,DELAY SMALL
             RET
DELAY_LONG: MOV R1,#40H
            NOP
            NOP
            DJNZ R1,DELAY_LONG
            RET
```

5. The above program is a test program for single analog input

6. The above program was running successfully and as we are not controlling any output of ADC so the output of Port 0 of microcontroller was the same that of ADC output channels

7. The above program was tested for 5 Volt and 0 Volt analog inputs.

Table for data acquired from electromagnetic sensor and the corresponding digital output:

Sr. No.	Angular Speed (RPM)	Voltage O/P of electromagnetic sensor(V)	Amplifier O/P V1	Digital output
1	1600	0.244	3.074	157
2	1325	0.219	2.912	149
3	1215	0.206	2.850	146
4	1140	0.199	2.800	143
5	1052	0.187	2.692	138
6	845	0.159	2.188	122
7	705	0.137	2.051	105
8	400	0.084	1.257	65
9	250	0.055	0.825	42

CHAPTER 6

Data acquisition card pcl-207

6. Data Acquisition Using PCL-207

PCL 207

The PCL-207 low cost AD/DA card is an easy to use, cost effective multifunction data acquisition card for IBM PC/XT/AT and compatible computers. The specifications of this half sized card and software support makes it ideal for a wide range of applications in industrial and laboratory environments. These applications include data acquisition, process control, automatic testing and factory automation.

6.1 SCOPE OF PCL-207 CARD

The PCL-207 is a low cost high performance analog interface card for IBM/PC/XT/AT and compatible computers. It uses the hardware based successive approximation method, providing 25 thousand samples per second acquisition rate. The true 12 bit conversion gives an overall accuracy of 0.015% reading +/-1 bit. The output channel provides fast settling time with accuracy. A high quality MUX in the input stage provides 8 single ended analog inputs. Standard input and output voltage ranges are user selectable, independent of each other.

6.2 APPLICATION AREAS

Features of the PCL-207 card makes it suitable for various applications . Some applications are discussed below.

1. Industrial Measurements/Automation

   The PCL-207 has great scope in this field. This card can be used to develop a continuous monitoring system for industrial automation.

2. Process control

   A continuous process can be made to receive feedback from a monitored system and any variation can be detected by the ADC. This will inform the ibm pc. Further action can be taken on the DAC channel depending on the software design. This makes the PCL-207 card highly versatile in the field of process control.

   The PCL-207 can also be widely used in laboratory measurements, Signal analysis etc.

The PCL-207 provides powerful and easy to use software driver routines which can be accessed by the basic call statement. The PCL card is provided with application software package.

6.3 SPECIFICATIONS

The data acquisition card has the following specification:

1. Analog Input (A/D converter)

   Channels : 8 single ended

   Resolution : 12 bits

   Input Range : Bipolar +/- 5v

   Overvoltage : continuous +/- 30v max.

   Conversion type : Successive approximation

   Converter : AD574 or equivalent

   Conversion speed: 25 microsecond max.

   Accuracy : 0.015% of reading +/- 1 bit

   Linearity : +/- 1bit

   Trigger mode : Software trigger

   Data transfer : Program control

2. Analog Output (D/A converter)

Channels	:	1 channel
Resolution	:	12 bits
Output range	:	0 to +5 v or 0 to +10v
Reference voltage:		Internal -5v and -10v(+/-0.05v)
Conversion type :		12 bit monolithic multityping
Analog devices	:	AD7541 AKN or equivalent
Linearity	:	+/- ½ bit
Output drive	:	+/- 5 ma max
Settling time	:	30 micro seconds

3. General Specifications

Power consumption: +5V: typ 100 ma, max 500ma
+12V:typ 40 ma, max100 ma
-12V:typ 20 ma, max 50ma

I/O connector : 20 pin post headers for analog I/O ports

6.4 Hardware Details

Base Address Selection:

Some of the PC peripheral devices and interface cards are controlled through input/output ports. These ports are addressed using the I/O port address space.

An 8 way DIP switch is present on board out of which SW1-SW6 is used for base address selection and SW7 and SW8 are used for software trigger selection.

The PCL-207 requires 16 consecutive address location in the I/O space.

Valid addresses are from hex 000 to hex 3F0. The factory setting is hex 220.If the user wants to change the default value to another value then before installing the card in the computer he must change the switch setting to any one of the following addresses.

I/O Address	**Switch selection**					
Range(Hex)	**1**	**2**	**3**	**4**	**5**	**6**
	A9	**A8**	**A7**	**A6**	**A5**	**A4**
000-00F	0	0	0	0	0	0
100-10F	0	1	0	0	0	0
200-20F	1	0	0	0	0	0
210-21F	1	0	0	0	0	1
220-22F	1	0	0	0	1	0
300-30F	1	1	0	0	0	0
3F0-3FF	1	1	1	1	1	1

NOTE: ON-0 , OFF-1

A4-A9 corresponds to PC bus address lines.

CONNECTOR PIN ASSIGNMENT

PCL-207 I provided with a single 20 pin FRC connector CN1, accessible through the rear of the PC. The pin assignment of this connector is as given below.

SIGNAL NAME	PIN NO.	PIN NO.	SIGNAL NAME
A/D 0	1	2	A.GND
A/D 1	3	4	A.GND
A/D 2	5	6	A.GND
A/D 3	7	8	A.GND
A/D 4	9	10	A.GND
A/D 5	11	12	A.GND
A/D 6	13	14	A.GND
A/D 7	15	16	A.GND
D/A	17	18	A.GND
A.GND	19	20	A.GND

JUMPER SELECTION

Only one jumper JP1 is provided on the PCL-207 card. It is used to select the D/A reference voltage. Two reference voltage are present on the board.

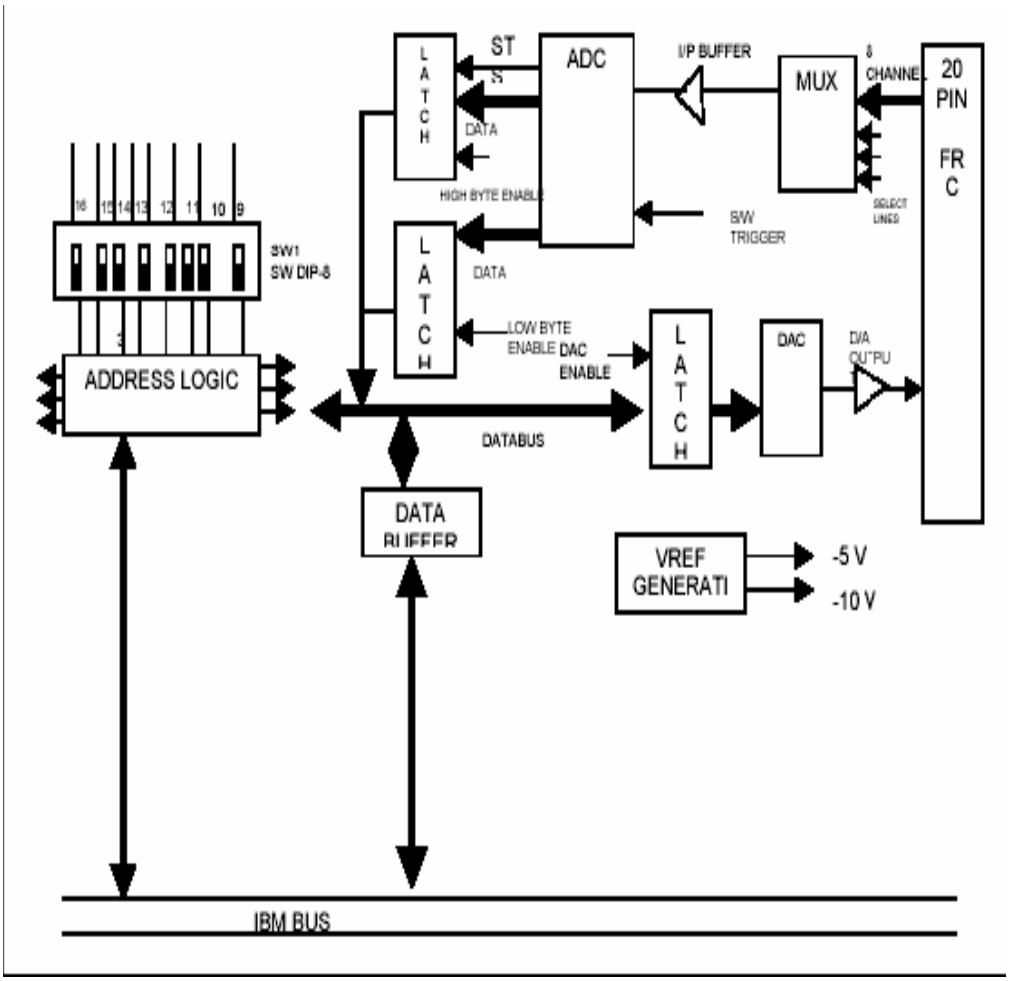


Figure 14

6.5 BLOCK DIAGRAM DESCRIPTION

The base address is selected by the DIP switch. When the software routine addresses the DIP switch address, the card is enabled. The reference voltage generator produces the desired reference voltage which are jumper selectable.

In the D/A operation the digital input from the PC is fed to a latch through the data buffer. The latched digital value is fed to the DAC logic for D/A conversion. The analog output is fed to a buffer and finally to the 20 pin FRC connector.

In the A/D operation any one of the 8 channels present on the 20 pin FRC can be selected by the MUX. For impedance matching the input signal is buffered and then fed to the ADC. The ADC can be software triggered by outputting the required through the specific address register. The converted data can be read through two latches, one containing the higher byte and the other lower byte. The data is fed to the IBM PC bus through the data buffer.

REGISTER STRUCTURE AND FORMAT:

The PCL-207 requires 16 consecutive addresses in the input output space. In order to program the PCL-207 a good understanding of the 16 registers addressable from the selected I/O port base address is necessary. A summary of the functions of each address and the data format of each register is given below.

I/O PORT ADDRESS MAP

The following table shows the location of each register and driver relative to the base address.

LOCATION	READ	WRITE
Base+0	N/U	N/U
+1	N/U	N/U
+2	N/U	N/U
+3	N/U	N/U
+4	A/D low byte	D/A low byte
+5	A/D high byte	D/A high byte
+6	N/U	N/U
+7	N/U	N/U
+8	N/U	N/U
+9	N/U	N/U
+10	N/U	MUX scan channel
+11	N/U	Software A/D trigger
+12	N/U	Software A/D trigger
+13	N/U	N/U

+14	N/U	N/U
+15	N/U	N/U

NOTE: N/U-Not Used

BASE+11 and BASE+12 can be selected through SW7 and SW8 of the DIP switch. Their combinations are as given below:

SW7	**SW8**	**LOCATION**
ON	OFF	BASE+11
OFF	ON	BASE+12

A/D DATA REGISTERS:

The PCL-207 performs 12 bit A/D conversions, an 8 bit register is not big enough to accommodate all 12 bits of data. Therefore A/D data is stored in two registers located at address BASE+4 and BASE+5.

DATA FORMAT:

1. **A/D LOW BYTE**

BASE+4	D7	D6	D5	D4	D3	D2	D1	D0
	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

2. **A/D HIGH BYTE**

BASE+5	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	DRDY	AD11	AD10	AD9	AD8

MUX SCAN REGISTR:

The MUX scan register is a write only register using address BASE+10. The low nibble provides the scan channel number. The MUX switches to a new channel when written to this register.

DATA FORMAT:

BASE+10	D7	D6	D5	D4	D3	D2	D1	D0
Scan channel	x	x	x	x	x	CL2	CL1	CL0
Channel 0	x	x	x	x	x	0	0	0
Channel 1	x	x	x	x	x	0	0	1
Channel 2	x	x	x	x	x	0	1	0
Channel 3	x	x	x	x	x	0	1	1
Channel 4	x	x	x	x	x	1	0	0
Channel 5	x	x	x	x	x	1	0	1
Channel 6	x	x	x	x	x	1	1	0
Channel 7	x	x	x	x	x	1	1	1

The PCL-207 A/D conversion is triggered by software. The software trigger is controlled by the application program issued software command.

6.6 CALIBERATION

In data acquisition and control, it is important to constantly calibrate the measurement device to maintain its accuracy. It is necessary to have a digital voltmeter, digital calibrator or a stable and noise free DC voltage source to perform the calibration.

PCL-207 VR ASSIGNMENT:

There are 3 variables (VR) on the PCL-207 to assist in making accurate adjustment on the A/D and D/A channels. The function of each VR is listed below:

VR1: D/A gain adjustment

VR2: A/D offset adjustment

VR3: A/D gain adjustment

A/D Calibration

The demo program DEMO02.BAS can be run to read the A/D data when standard voltages are applied to the input channel.

1. Apply a short to the input channel and adjust VR2 (offset) to obtain zero data.
2. Apply +4.9963V to the input channel and adjust VR3 (gain) so that the data lies between 2046 and 2047.

   Other voltages can be applied to the input to check the linearity.

D/A Calibration

The demo program DEMO04.BAS is run in order to make D/A calibration. The users should choose the D/A range to be calibrated by setting the jumper JP. Set the D/A data to 4095 to get full scale output. Measure the output voltage with a precision voltmeter. Adjust VR1 (D/A gain) to get the correct full scale voltage.

CHAPTER 7

Conclusion and reference

CONCLUSION

Here in our project we have designed an 8 single ended input channel data acquisition system using ATMEL89c51 microcontroller and ADC0808CCN analog to digital converter, using 555 timer. The designed model was programmed in assembly level language for single analog input and was tested under proper condition.

Also we have used PCL-207 as an interface to realize PC based data acquisition in partial fulfillment. Owing to shifting of most instrumentation system towards PC compatibility it offer more advantage compared to 89c51 based data acquisition system. Also it is more flexible as program can be changed according to requirement repeatedly.

Future work:

We have used both model for acquiring and processing analog input but with slight modification it can be used in control application. For e.g. on the basis of data acquired from tachogenerator voltage driving can be varied to maintain the speed at desired value.

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