Performance Study of Nano-Scale Transistor with Conventional Transistor

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF

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By

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ROURKELA

CERTIFICATE

This is to certify that the thesis entitled, "Performance Study of Nano-Scale Transistor with Conventional Transistor" submitted by Subash Hansdah and Pankaj Kumar Bharti in partial fulfillments for the requirements for the award of Bachelor of Technology Degree in Electrical Engineering at National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by them under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been duplicated from any other University / Institute for the award of any Degree or Diploma.

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Last but not the least, our sincere thanks to all of our friends who have patiently extended all sorts of help in this project.

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:ABSTRACT:

According to Moore's Law, the no of transistors in an IC chip doubles every 18 months. This leads in increase in power density. Hence in modern power circuits, the main factor of the circuit efficiency is power efficiency. Due to scaling, leakage power accounts for an increasingly large portion of the total power consumption in deep submicron technologies.

In this article, we proposed a methodology to find the problems occurring while scaling it into small size with some factor. We have simulated the inverter circuit using CMOS in MATLAB, P-Spice (ICs used BSH107, BSH207) and nano-CMOS using T-Spice where we can vary the physical dimensions of the MOSFET. The outputs were observed and the time delay was calculated. The above results showed that, as we go on reducing the size, the performance enhances. Due to some limitations, the CMOS were facing some of the problems like Drain-induced barrier lowering (DIBL), Velocity Saturation, Punch through, Oxide Breakdown, Channel length modulation.

Hence due to the above factors, FinFET technology has proposed as an alternative to deep sub-micron bulk CMOS. FinFET is likely to meet the performance requirements in the sub-20nm gate length regime. FinFET will replace the traditional MOSFET due to its better performance in sub 20nm regime and also it has excellent control over the problems faced by the Traditional CMOS.

CHAPTER-I

INTRODUCTION

1.1 *History of Transistor*

During the period 1904-1947, the vacuum tube was the electronic device of interest and development. In 1904, the vacuum-tube diode was introduced by J.A. Fleming. Shortly thereafter, in 1906, Lee De Forest added a third element, called the control grid, to the vacuum diode, resulting in the first amplifier, the triode. On December 3, 1947, however, the electronics industry was to experience the advent of a completely new direction of interest and development. It was on the afternoon of this day that Walter H. Brattain and John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories. The advantages of these three terminal solid state devices over the tube were immediately obvious. It was smaller and light weight had no heater requirement or heater loss: had rugged construction and was more efficient since less power was observed by the device itself,: it was instantly available for use, requiring no warm-up period and lower operating voltage were possible.**[3]**

This was the History of Development of transistor, how it came to function in the electronics world.

1.2 *Transistor*

A transistor is a semiconductor device which is used to amplify and switch electronic signals. It is made of a solid piece of semiconductor material, with at least three terminals for connection to an external circuit. A voltage or current applied to one pair of the transistor's terminals changes the current flowing through another pair of terminals. Because the controlled (output) power can be much more than the controlling (input) power, the transistor provides amplification of a signal. Some transistors are packaged individually but many more are found embedded in integrated circuits.

The different types of transistors are BJT, JFET, IGFET (MOSFET) and IGBT. **[4]**

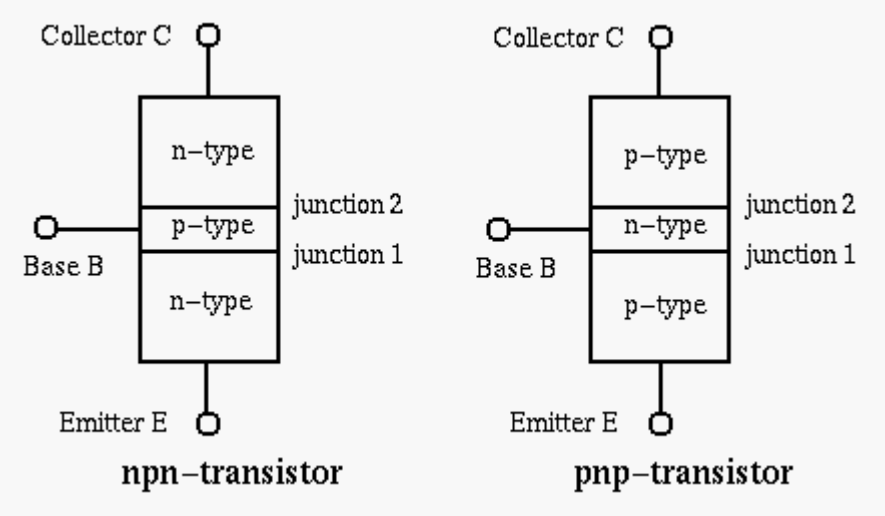


Fig. 1.2.1 (BJT)

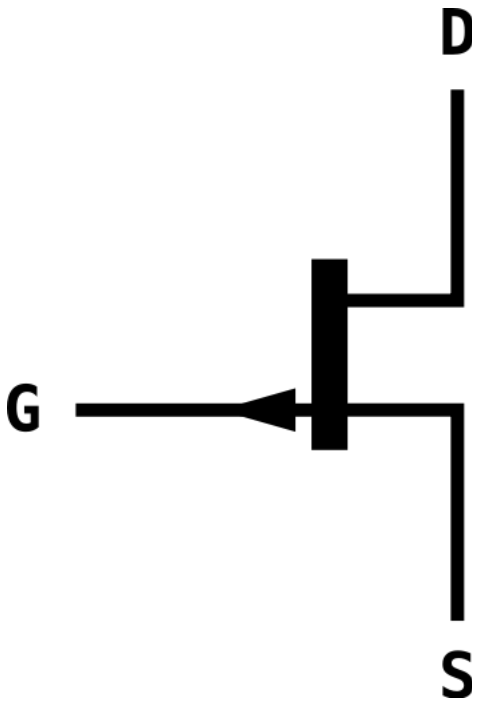


Fig. 1.2.2 (JFET)

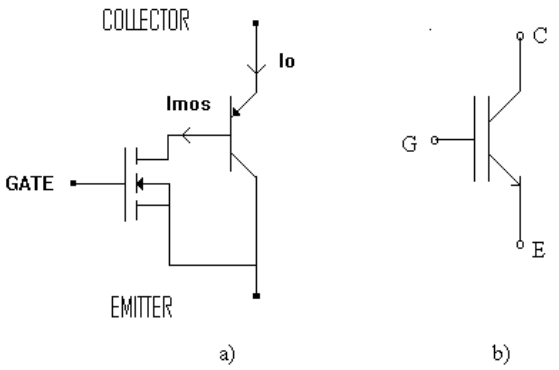


Fig. 1.2.3 (IGBT)

In our work, we will be mainly concentrating on MOSFET.

1.3 OBJECTIVE

The objective is to simulate the inverter circuit using CMOS through MATLAB, P-Spice and T-Spice and comparing with the nano CMOS. Comparison with traditional MOS with FinFET was also studied. The merits of small scale are also discussed.

1.4 FUTURE PROSPECTS

The future work is to replace the Bulk-CMOS with the nano-CMOS and make the system faster. This includes SD-RAM, Processor, logic circuits, and switches, and also where we can implement these applications. FinFET being one of the nano device is the better option among all the devices because of smaller size among all the above. FinFET can overcome all the problems caused by scaling the MOSFET into the nano regime.

Wider FinFET devices are built utilizing multiple parallel fins between the source and drain. Independent gating of the FinFET's double gates allows significant reduction in leakage current.

CHAPTER-II

MOSFET

2.1 INTRODUCTION

Metal-Oxide-Semiconductor Field Effect Transistor is a three terminal device used for a variety of applications as per the requirement in different fields of electronics. It is used for amplifying or switching electronic signals. The basic principle of the device was first proposed by Julius Edgar Lilienfield in 1925. In MOSFETs, a voltage on the oxide-insulated gate electrode can induce a conducting channel between the two other contacts called source and drain. The channel can be of n-type or p-type and is accordingly called an nMOSFET or a pMOSFET (also commonly nMOS, pMOS).

2.2 COMPOSITION

Usually the semiconductor of choice is silicon, but some chip manufacturers, most notably IBM, recently started using a chemical compound (bond, NOT a mixture) of silicon and germanium (SiGe) in MOSFET channels. Unfortunately, many semiconductors with better electrical properties than silicon, such as gallium arsenide, do not form good semiconductor-to-insulator interfaces, thus are not suitable for MOSFETs.

2.3 CONSTRUCTION

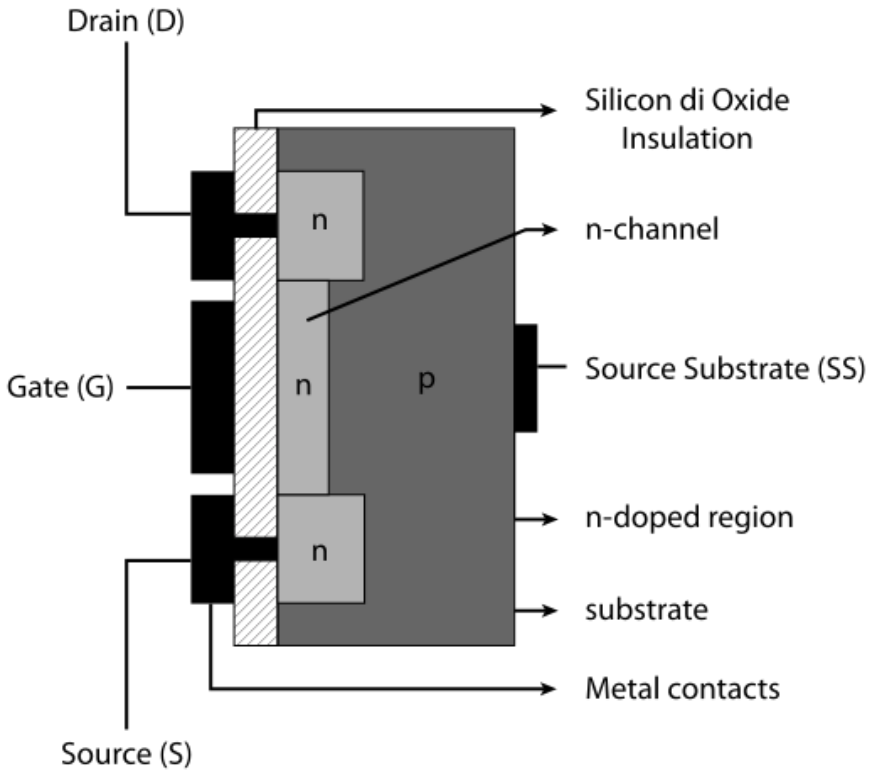


Fig. 2.3.1(Structure of MOSFET)

The basic construction of the n-channel enhancement-type MOSFET is provided in Fig. 2.3.1. A slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally external control of its potential level. The source and drain terminals are again connected through metallic contacts to n-doped regions. This is the primary difference between the constructions of depletion-type and enhancement-type MOSFETs -the absence of a channel as a constructed component of the device. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

2.4 OPERATION

A traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO_2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon (the latter is commonly used). As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor.

When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. If we consider a P-type semiconductor (with N_A the density of acceptors, p the density of holes; $p = N_A$ in neutral bulk), a positive voltage, V_{GB}, from gate to body (see figure. 2.4.1) creates a depletion layer by forcing the positively charged holes away from the gate-insulator/semiconductor interface, leaving exposed a carrier-free region of immobile, negatively charged acceptor ions. If V_{GB} is high enough, a high concentration of negative charge carriers forms in an inversion layer located in a thin layer next to the interface between the semiconductor and the insulator. Unlike the MOSFET, where the inversion layer electrons are supplied rapidly from the source/drain electrodes, in the MOS capacitor they are produced much more slowly by thermal generation through carrier generation and recombination centers in the depletion region. Conventionally, the gate voltage at which the volume density of electrons in the inversion layer is the same as the volume density of holes in the body is called the threshold voltage.

This structure with P-type body is the basis of the N-type MOSFET, which requires the addition of an N-type source and drain regions.

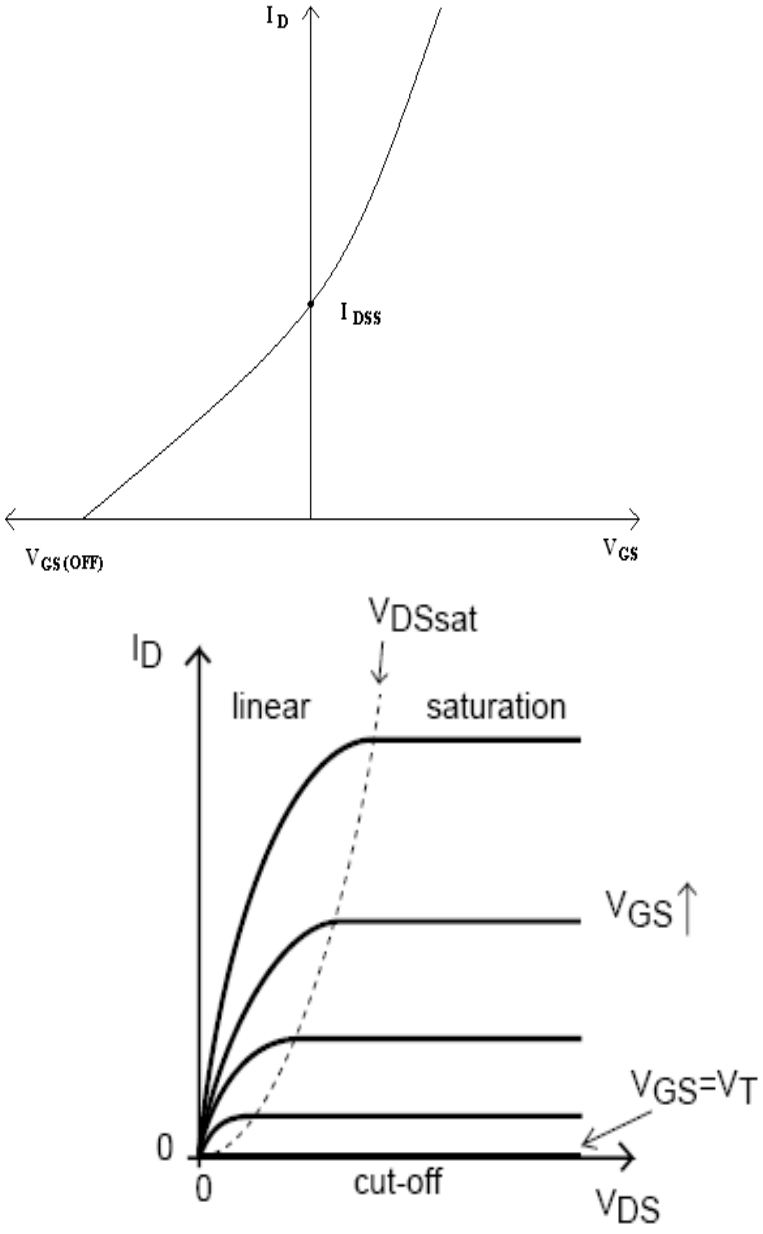


Fig. 2.4.1

(Operation of MOSFET)

CHAPTER-III

SCALING OF MOSFET

3.1 INTRODUCTION OF SCALING

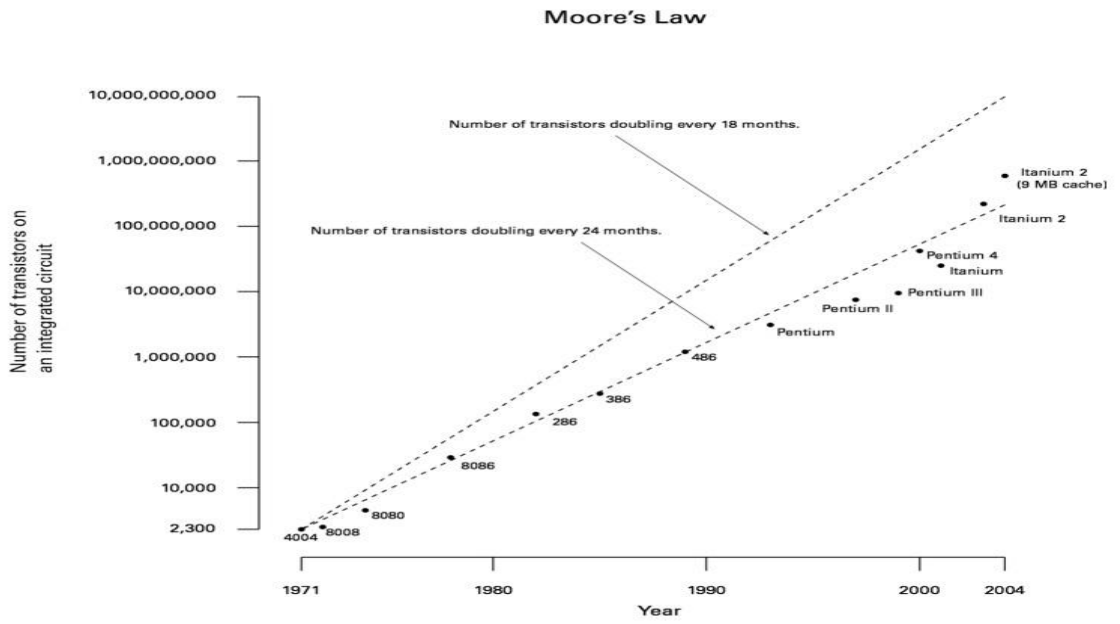


Fig 3.1.1 (Moore's Law)

In order to satisfy Moore's Law, modern transistors are made very small to fit in a single IC chip for fast operation. The reduction of the dimensions of a MOSFET has been dramatic during the last three decades.

The gate length was gradually reduced from 10 mm in 1970 to 0.15 mm minimum feature size in 2000, resulting in a 13% reduction per year. Proper scaling of MOSFET requires a reduction of other dimensions like, reduction of the gate length and width , gate/source and gate/drain alignment, the oxide thickness and the depletion layer widths. Scaling of the depletion layer widths also implies a scaling of the substrate doping density.

The common types of scaling are: constant field scaling and constant voltage scaling.

Constant field scaling yields the largest reduction in the power-delay product of a single transistor. However, it requires a reduction in the power supply voltage as one decreases the minimum feature size. Constant voltage scaling does not have this problem and is therefore the preferred scaling method as it provides voltage compatibility with older circuit technologies. The disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length is reduced. This leads to velocity saturation, mobility degradation, increased leakage currents and lower breakdown voltages.

3.2 SCALING TABLE

Parameter	Symbol	Constant Field Scaling	Constant Voltage Scaling	Constant Voltage Scaling with velocity saturation
Gate length	L	$1/\alpha$	$1/\alpha$	$1/\alpha$
Gate width	W	$1/\alpha$	$1/\alpha$	$1/\alpha$
Field	$\mathcal{E}$	1	α	α
Oxide thickness	t_{ox}	$1/\alpha$	$1/\alpha$	$1/\alpha$
Substrate doping	N_a	α^2	α^2	α^2
Gate capacitance	C_G	$1/\alpha$	$1/\alpha$	$1/\alpha$
Oxide capacitance	C_{ox}	α	α	α
Transit time	t_r	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha$
Transit frequency	f_T	α	α^2	α
Voltage	V	$1/\alpha$	1	1
Current	I	$1/\alpha$	α	1
Power	P	$1/\alpha^2$	α	1
Power-delay	$P \Delta t$	$1/\alpha^3$	$1/\alpha$	$1/\alpha$

3.3 SCALING LIMITATIONS IN MOSFET

3.3.1Channel length modulation

Channel length modulation in a MOSFET is caused by the increase of the depletion layer width at the drain as the drain voltage is increased. This leads to a shorter channel length and an increase in drain current. The channel-length-modulation effect is typically high in small devices with low-doped substrates. An extreme case of channel length modulation is a punch through where the channel length reduces to zero. We can reduce channel length modulation by proper scaling, i.e by increasing the doping density as the gate length is reduces.

3.3.2 Drain induced barrier lowering(DIBL)

Effect of the drain voltage on the output conductance and measured threshold voltage is called ‘drain induced barrier lowering’. This effect occurs in devices where only the gate length is reduced without proper scaling of the other dimensions. It is observed as a variation of the measured threshold voltage with reduced gate length. The threshold variation is caused by the increased current with increased drain voltage as the applied drain voltage controls the inversion layer charge at the drain, thereby competing with the gate voltage. This effect is due to the two-dimensional field distribution at the drain end and can be eliminated by properly scaling the drain and source depths while increasing the substrate doping density.

3.3.3 Velocity saturation

As devices are reduced in size, the electric field also increases and the carriers in the channel have an increased velocity. However at high field values there is no longer a linear relation between the electric field and the velocity as the velocity gradually saturates reaching the saturation velocity. This velocity saturation is caused by the increase in scattering rate of highly energetic electrons, primarily due to optical phonon emission. This effect increases the transit time of carriers through the channel. In sub-micron MOSFETs it is found that the average electron velocity is larger than in bulk material so that velocity saturation is not quite as much of a restriction as initially thought.

3.3.4 Oxide Breakdown

As the gate-oxide is scaled down, breakdown of the oxide and oxide reliability becomes more of a concern. Higher fields in the oxide increase the tunneling of carriers from the channel into the oxide. These carriers slowly degrade the quality of the oxide and lead to failure of the oxide over time. This effect is referred to as time dependent destructive breakdown (TDDB).

Oxides other than silicon dioxide have been considered as alternate oxides and are referred to as high-k dielectrics. These oxides have larger dielectric constant so that the same gate capacitance can be obtained with a thicker oxide. The challenge is to obtain the same stability, reliability and breakdown voltage as silicon dioxide. Oxides of interest include - Al2O3, ZrO and TiO.

CHAPTER-IV

EXPERIMENTATION

4.1 Simulation of CMOS Inverter Logic Circuit using MATLAB.

Simulation of inverter circuit was carried out using CMOS through MATLAB software. And output was observed. NOT gate and NAND gate was designed through MATLAB.

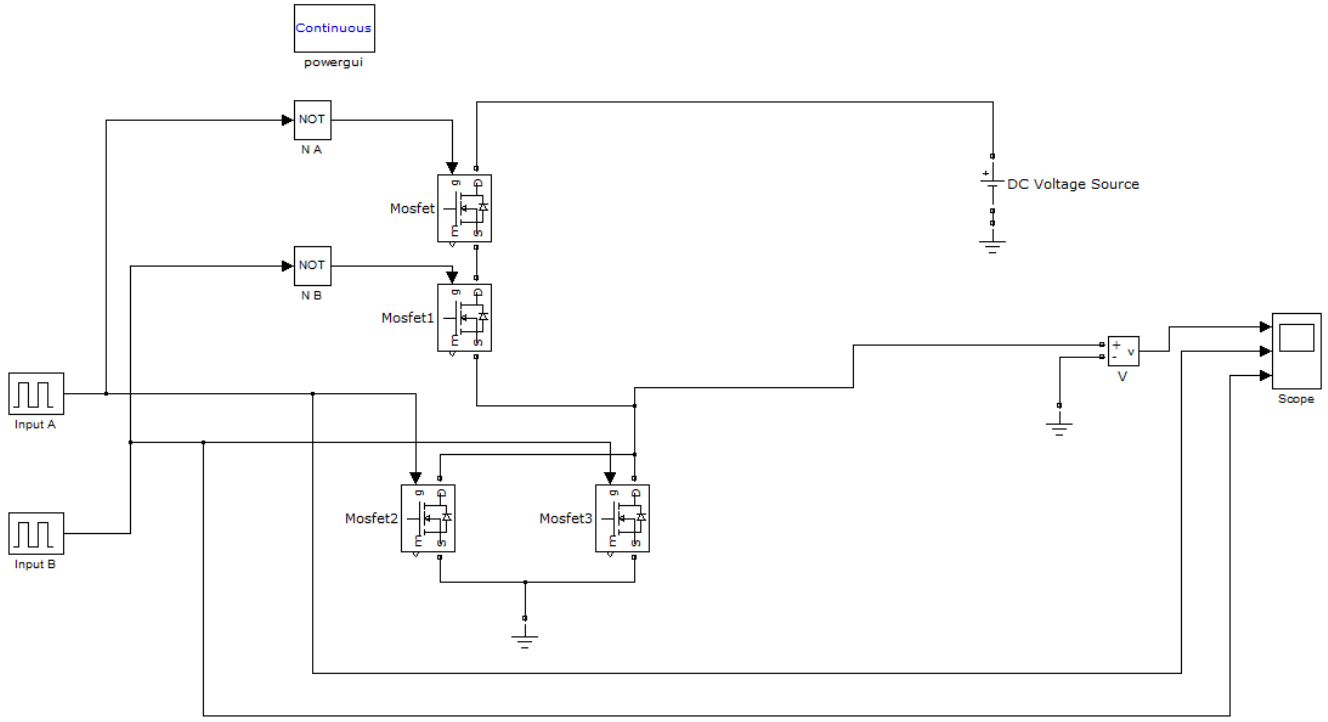


Fig. 4.1.1(NOR GATE)

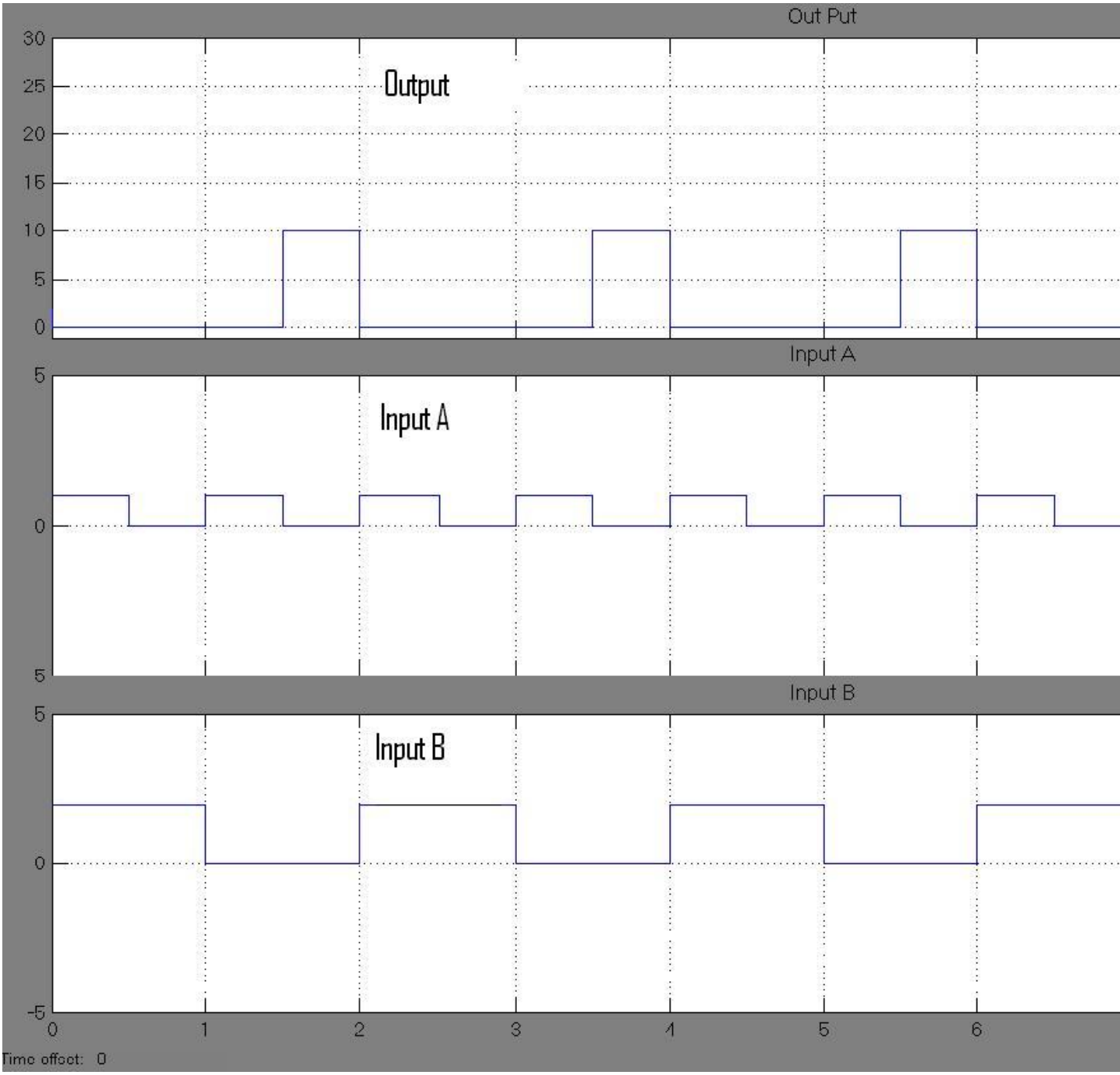
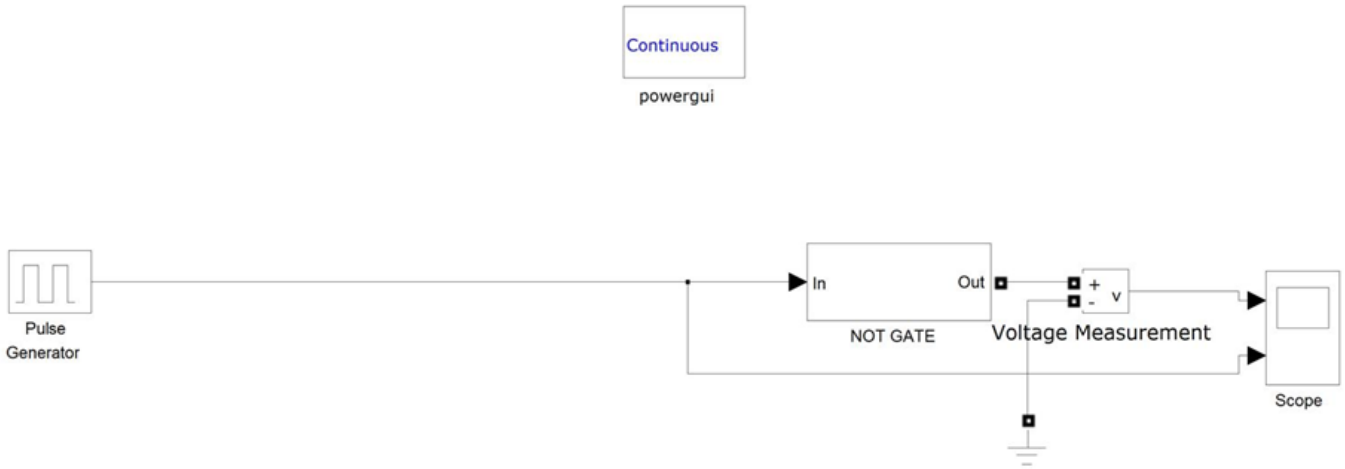
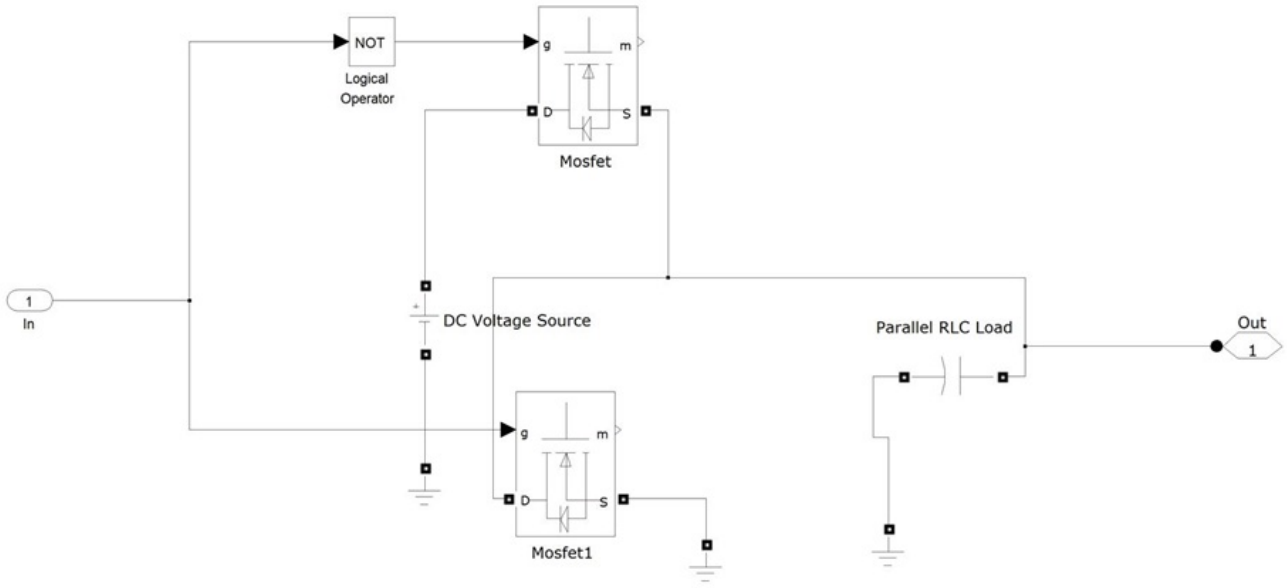


Fig 4.1.2(NOR OUTPUT)



NOT Gate

Fig 4.1.3 (NOT GATE)



NOT gate (sub system inside block)

Fig 4.1.4 (NOT GATE)

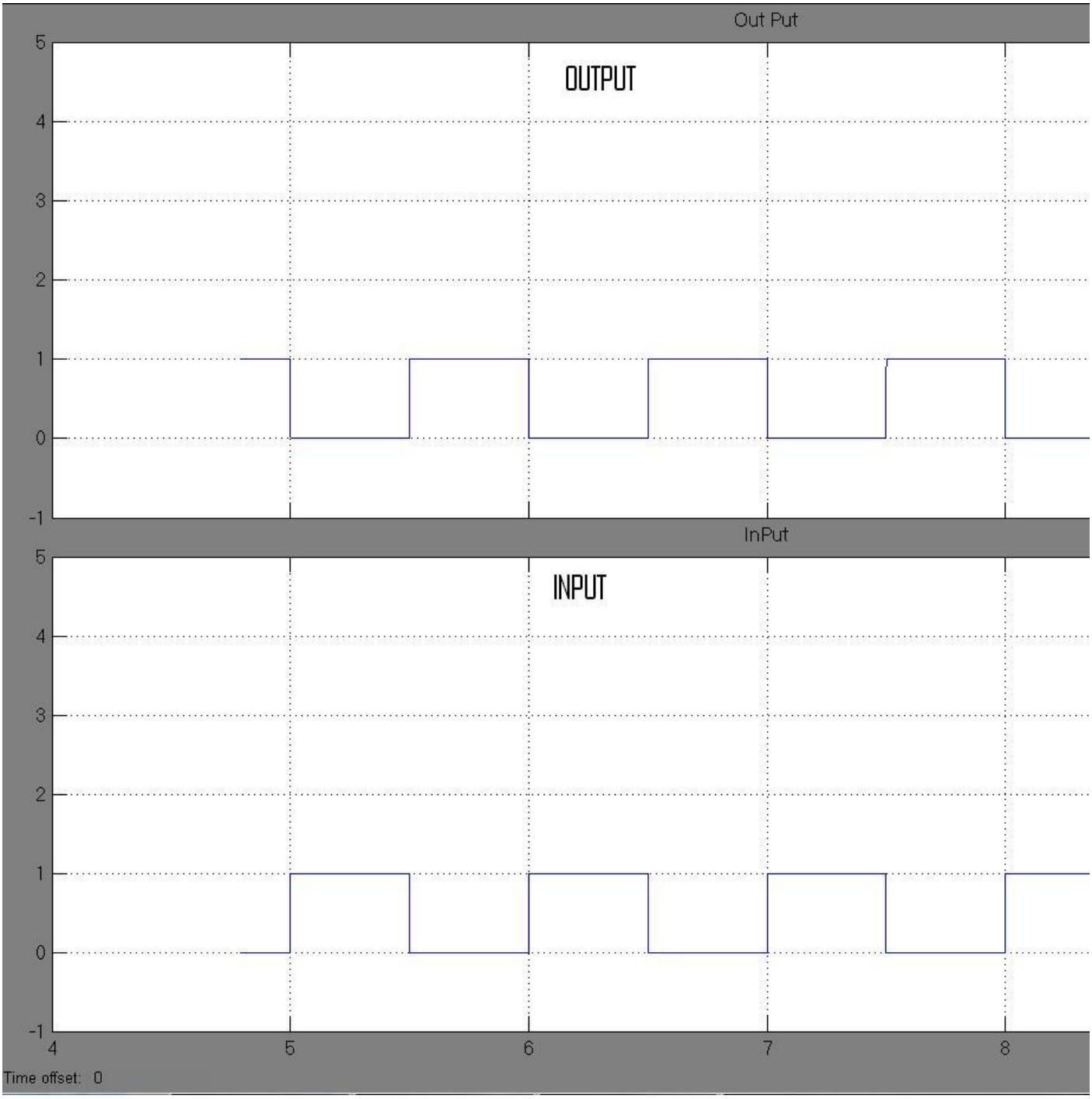


Fig 4.1.5 (NOT GATE OUTPUT)

4.2 Simulation of CMOS Inverter Logic Circuit using P-Spice.

The inverter circuit was also simulated using P-Spice and the MOSFET used were BSH107 (N-channel enhancement MOSFET) and BSH201 (P-channel enhancement MOSFET). In this simulation, we have observed the frequency of operation, time delay and also calculated the power dissipation of the MOSFET during the work.

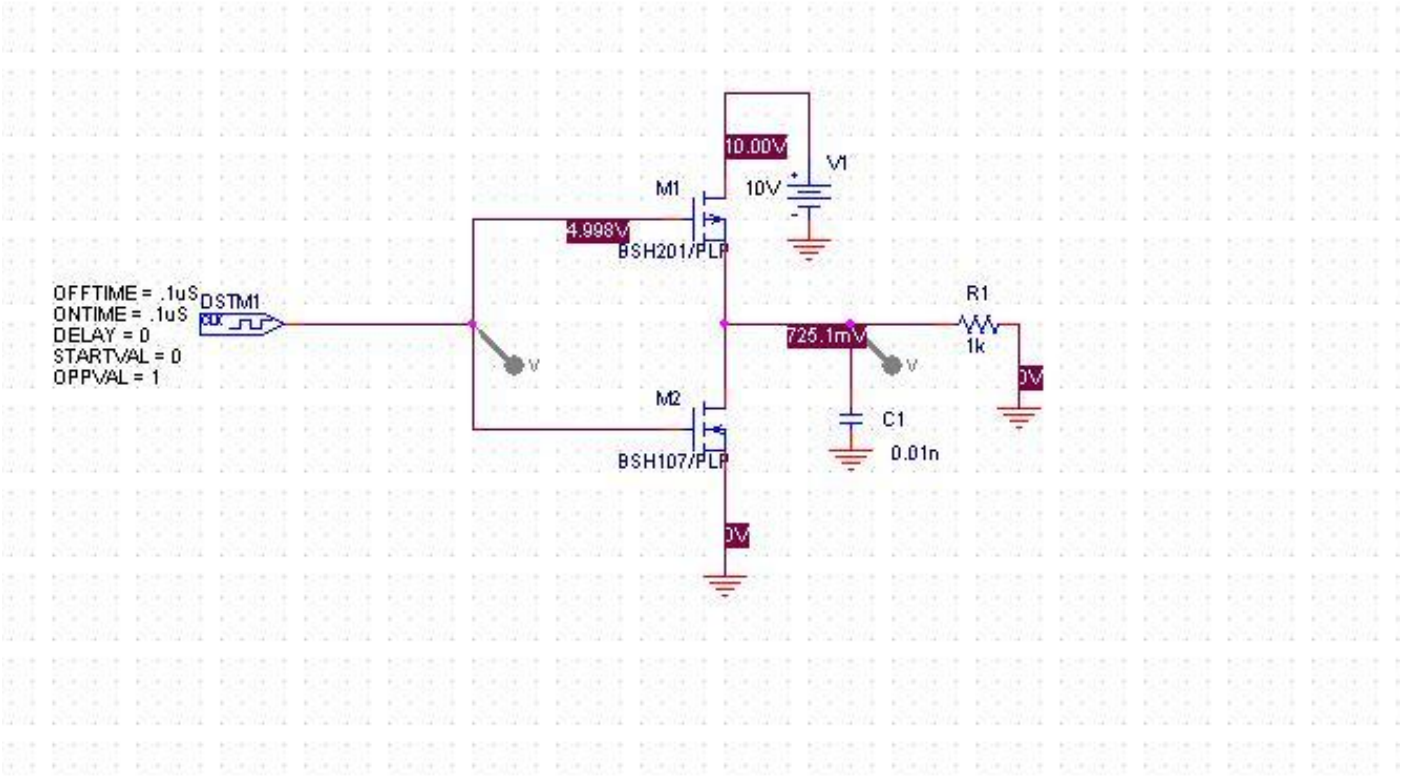


Fig 4.2.1(Figure of Inverter Circuit on P-Spice Platform)

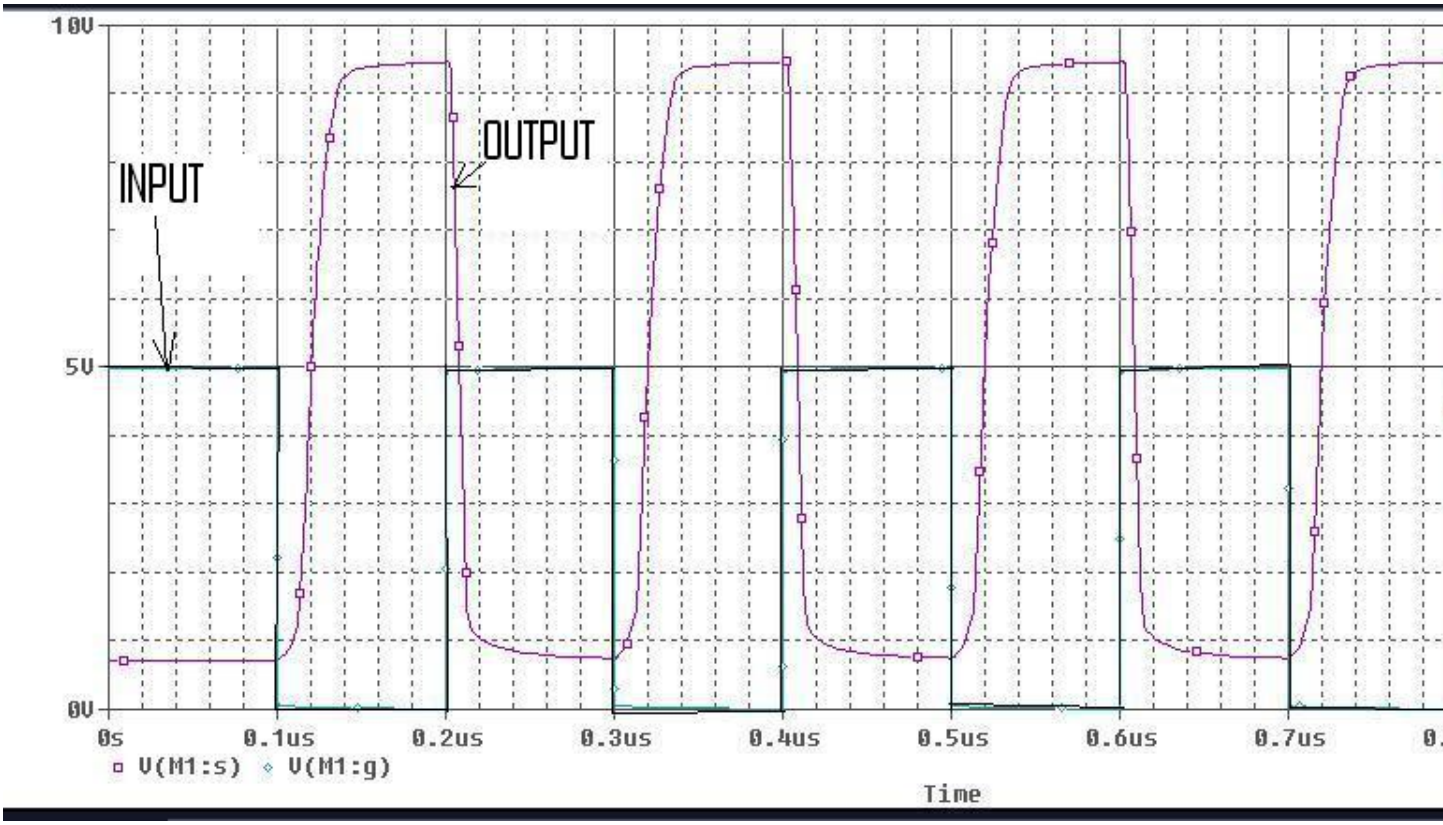


Fig 4.2.2 (Output of Inverter through P-Spice)

4.2.1. Calculation: -

A standard MOSFET has a Width of 25 µm and Length of 16 µm. Frequency from the graph,

$f = 1/(0.2\mu s)$

Hence, Time Delay= 0.02 µs, Frequency=5 MHz, V_{DD}=10 V, Internal capacitance = 15pF (Datasheet of BSH201 MOSFET)

Power = $(fCV_{DD})^2$

Applying the formula, we get Power Dissipation= 7.5mW

4.3 Simulation of Nano-CMOS Inverter Logic Circuit using T-Spice.

4.3.1 Program Code for Simulation of T-Spice.

.

```
option search="C:\Documents and Settings\Subash\My Documents\Tanner EDA\Tanner Tools v12.1 Demo\T-Spice\models"

.probe

.option probev

.option probei

.include "ml2_125.md"

m1n out in Gnd Gnd nmos L=5u W=10u

m1p out in Vdd Vdd pmos L=5u W=20u

c2 out Gnd 0.00000001F

vin in Gnd pwl (0ns 0V 100ns 0V 105ns 3V 200ns 3V 205ns 0V 300ns 0V 305ns 3V 400ns 3V 405ns 0V 500ns 0V 505ns 3V 600ns 3V)

vdd Vdd Gnd 3

.print tran v(in) v(out)

.tran 1n 600n

.end
```

4.4. Different Sets of values for MOS:

*4.4.1 Case – I (nmos L=40 n*m *W=60 n*m*),(pmos L=40 n*m *W=80* µm*)*

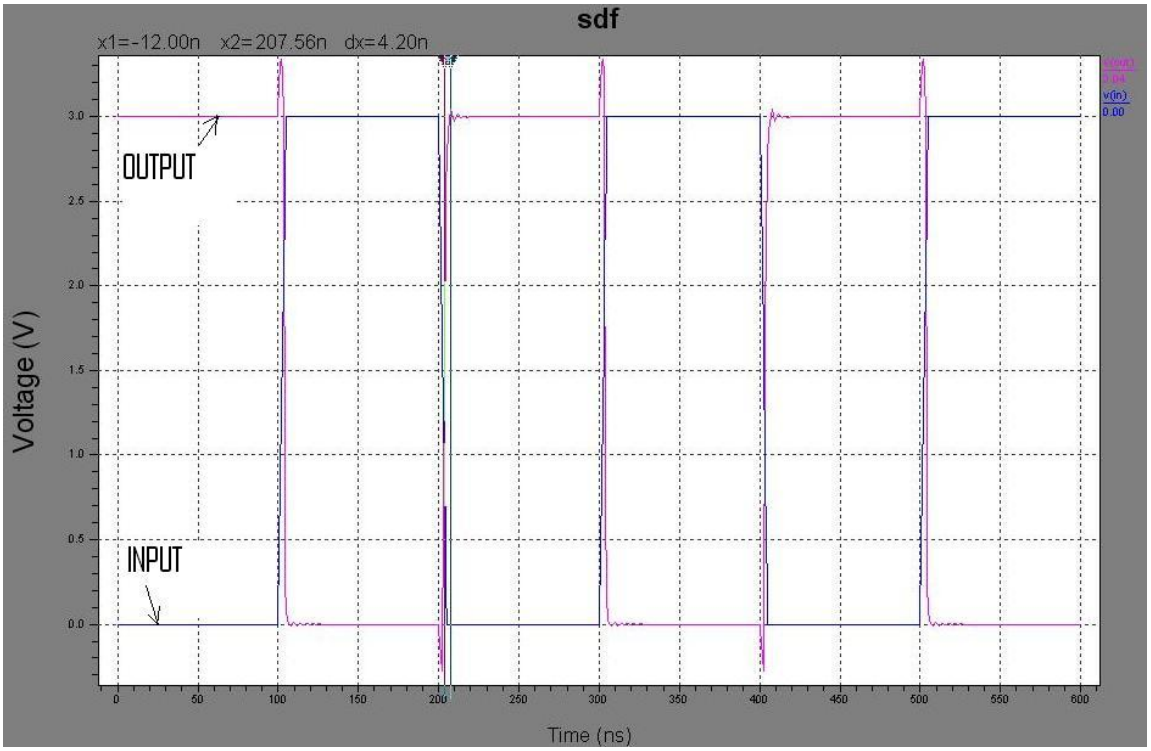


Fig. 4.4.1(Inverter output using T-Spice)

4.4.1.1 Calculation

T-Spice is simulation software, which provides freedom to vary the physical parameters of any device. Through which we can vary the physical parameters of MOSFET like Length, Width, Internal Capacitance, etc. We reduce the length and width of the MOSFET taking the eq. below into consideration.

$\left(\frac{W}{L}\right) > 1.5$

And accordingly change the internal capacitance changes according to equation

$C_{gs}=C_{gd}=0.5WLC_{ox}$, where W=Width of MOSFET, L=Length of MOSFET, t_{ox}=2nm

C_{ox}= Capacitance per unit gate area. $C_{ox}=\varepsilon_{ox}/t_{ox}$, $\varepsilon_{ox}=3.9$ $\varepsilon_o=3.45x10^{-11}$ F/m ($\varepsilon_o=8.854x10^{-12}$ F/m)

Frequency is calculated through the graph. The input frequency of clock is considered.

$f = 1/(100ns)$ = 10 MHz

Taking W=60 nm, L=40 nm, Frequency= 10 MHz, V_{DD}=10 V,

We got C=18.84 x 10^{-18} F

$P=Cf[(V_{DD})]^2$

And calculating power $P = fC(V_{DD})^2$ **[6]**

Hence Power Dissipation= 18.84 x 10^{-9} W.

Propagation delay can also be measured through the graph=4.2 ns.

4.4.2 Case – II (nmos L=5 µm *W=10* µm*), (pmos L=5* µm *W=20* µm*)*

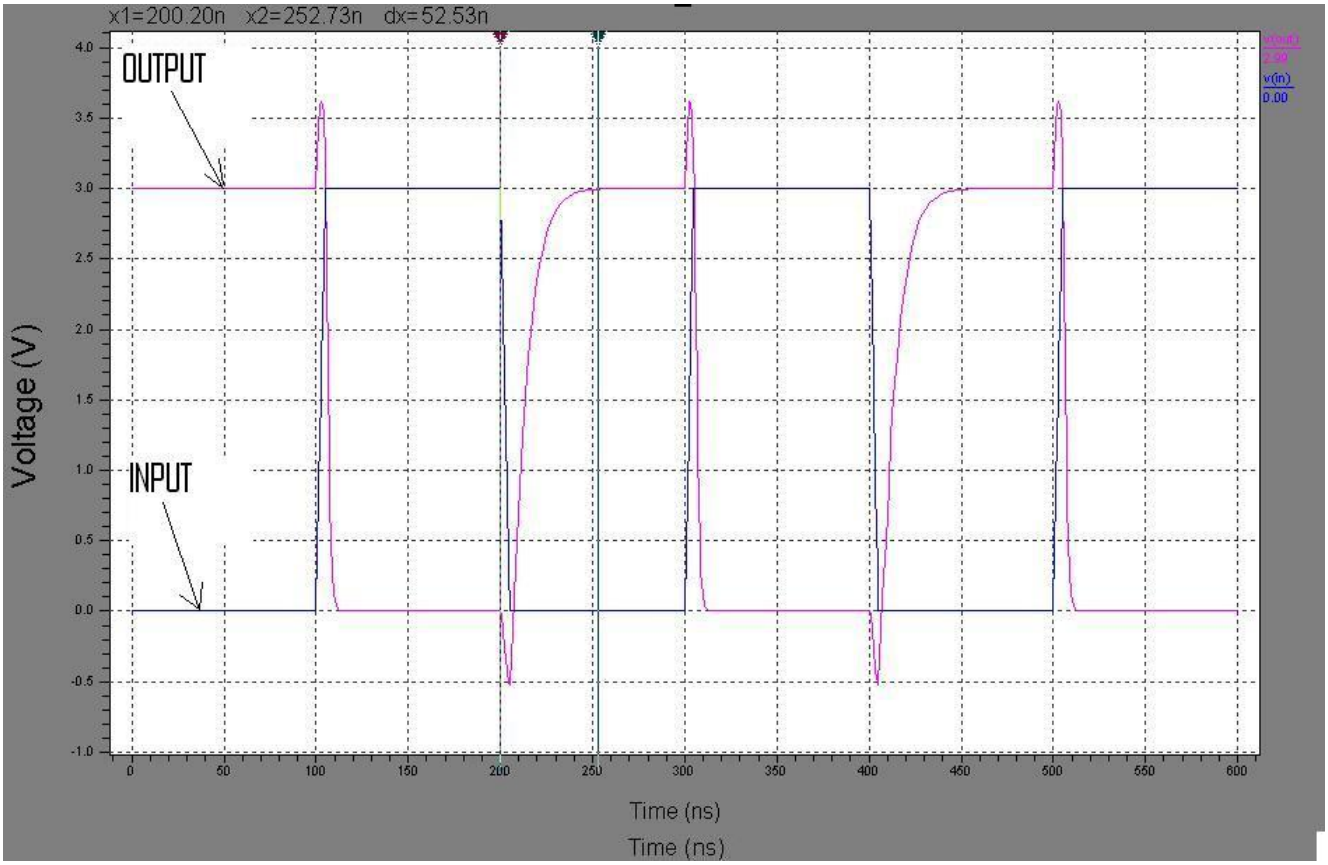


Fig. 4.4.2 (Output of CMOS with L=5 µm W=10 µm)

4.4.2.1 Calculation

Here we get, propagation delay= 52.53 ns.

$C_{gs}=C_{gd}=0.5WLC_{ox}$, where W=Width of MOSFET, L=Length of MOSFET, t_{ox}=2nm

C_{ox}= Capacitance per unit gate area. $C_{ox}=\varepsilon_{ox}/t_{ox}$, $\varepsilon_{ox}=3.9$ $\varepsilon_o=3.45x10^{-11}$ F/m ($\varepsilon_o=8.854x10^{-12}$ F/m)

Frequency is calculated through the graph. The input frequency of clock is considered.

$f = 1/(200ns)$ = 5 MHz

Taking W=10 µm, L=5 µm, Frequency= 5 MHz, V_{DD}=10 V,

We got C=39.25 x 10^{-14} F

$P=Cf[(V_{DD})]^2$

And calculating power $P = fC(V_{DD})^2$ **[6]**

Hence Power Dissipation= 0.196 mW.

Propagation delay can also be measured through the graph=52.53 ns.

4.4.3 Case-III (nmos L=0.5 µm, W=1 µm), (pmos L=0.5 µm, W=2 µm)

In this case, we get propagation delay= 35.72 ns,

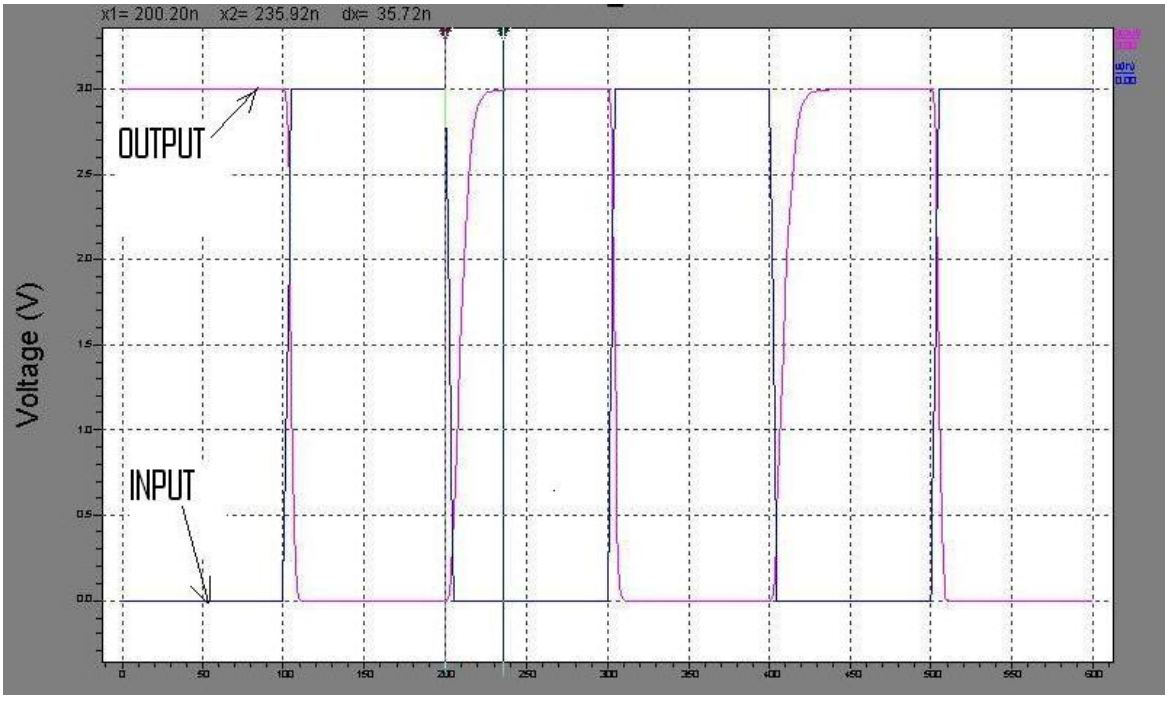


Fig. 4.4.3 (Output of Nano-CMOS with L=0.5 µm W=1 µm)

4.4.3.1 Calculation

Here we get, propagation delay= 35.72 ns.

$C_{gs}=C_{gd}=0.5WLC_{ox}$, where W=Width of MOSFET, L=Length of MOSFET, t_{ox}=2nm

C_{ox}= Capacitance per unit gate area. $C_{ox}=\varepsilon_{ox}/t_{ox}$, $\varepsilon_{ox}=3.9$ $\varepsilon_o=3.45x10^{-11}$ F/m ($\varepsilon_o=8.854x10^{-12}$ F/m)

Frequency is calculated through the graph. The input frequency of clock is considered.

$f = 1/(200ns)$ = 5 MHz

Taking W=1 µm, L=0.5 µm, Frequency= 5 MHz, V_{DD}=10 V,

We got C=39.25 x 10^{-16} F

$P=Cf[(V_{DD})]^2$

And calculating power $P = fC(V_{DD})^2$ **[6]**

Hence Power Dissipation= 3.9 µW.

Propagation delay can also be measured through the graph=35.72 ns.

4.4.4 Case-IV (nmos L=0.1 µm, W=0.2 µm), (pmos L=0.1 µm, W=0.4 µm)

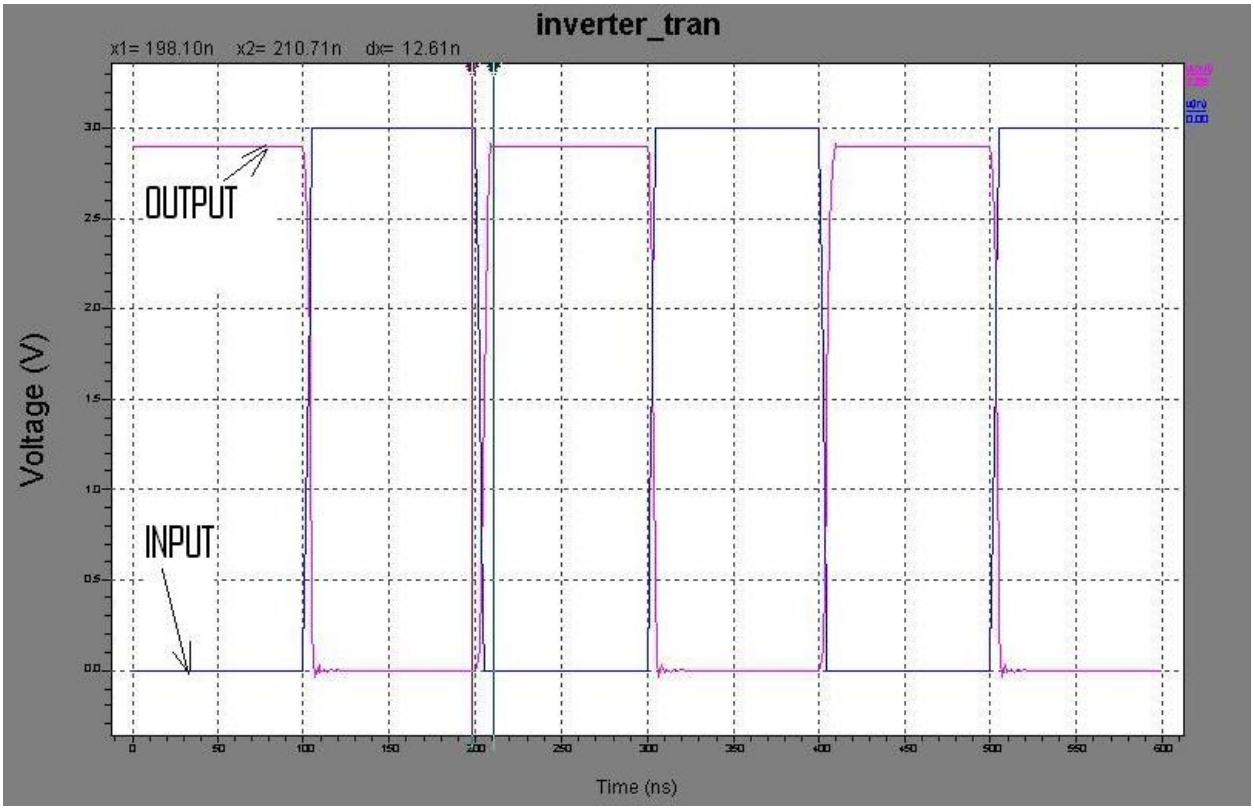


Fig.4.4.4. (Output of Nano-CMOS with L=0.1 µm W=0.2µm)

4.4.4.1 Calculation

Here we get, propagation delay= 12.61 ns.

$C_{gs}=C_{gd}=0.5WLC_{ox}$, where W=Width of MOSFET, L=Length of MOSFET, t_{ox}=2nm

C_{ox}= Capacitance per unit gate area. $C_{ox}=\varepsilon_{ox}/t_{ox}$, $\varepsilon_{ox}=3.9$ $\varepsilon_o=3.45\text{x}10^{-11}$ F/m ($\varepsilon_o=8.854\text{x}10^{-12}$ F/m)

Frequency is calculated through the graph. The input frequency of clock is considered.

$f = 1/(100ns)$ = 10 MHz

Taking W=0.2 µm, L=0.1 µm, Frequency= 5 MHz, V_{DD}=10 V,

We got C=1.57 x 10^{-16} F

$P=Cf[(V_{DD})]^2$

And calculating power $P = fC(V_{DD})^2$ **[6]**

Hence Power Dissipation= 0.157 µW.

Propagation delay can also be measured through the graph=12.61 ns.

4.5 Result.

L=5 µm W=10µm, Propagation Delay= 52.53 ns, Power Dissipated= 0.196 m W

L=0.5 µm W=0.1µm, Propagation Delay= 35.72 ns, Power Dissipated= 3.9 µW

L=0.1 µm W=0.2µm, Propagation Delay= 12.61ns, Power Dissipated= 0.157 µW

L=40 nm W=60 nm, Propagation Delay= 4.2 ns, Power Dissipated= 0.0188 µW.

From the above cases, we got that the propagation delay in first case is very less and also in respect of power consumption. Hence, we can opt for small size MOSFET in the range of nano scale. Further decrement of size is going on and also research is going on to make the device overall good in all respects.

CHAPTER-V

FINFET

5.1 INTRODUCTION

From the above analysis, we came to conclude that, the smaller the size, better is the overall performance of the MOSFET. And also the MOSFET will work better if it had been further small. But as per discussed in the section 3.3, we can't further reduce the size of MOSFET. Hence, the limitations restrict the use of MOSFET to reduce further and according to Moore' Law, we need further smaller MOSFETs.

5.2 FinFET

The FinFET has been developed to overcome the problems faced by MOSFET. It is basically a multi gate Field Effect Transistor which has been scaled further of MOSFET. It has all properties similar to a transistor, but has some advantages on CMOS. As you can see the above figures, multiple drains and multiple sources, we can also use each pair of source and drain can be considered as a single transistor hence increasing the no of transistors in one FinFET.

MOSFET has some technical problems like i) short channel effects and ii) Corner Effect Corner Effects has following problems: -

a) An enhancement of the leakage current at the edges of the active area adjacent to shallow trench isolation

b) Leakage enhancement is especially strong, if the gate electrode wraps around the corner of the active area

c) Corner effect leads to a not complete switching-off of the STI MOS transistors and worsens the transistor performance.

So to overcome the difficulty faced by traditional MOSFET, FinFET came into role and to make the transistors more efficient. Wider FinFET devices are built utilizing multiple parallel fins between the source and drain. Independent gating of the FinFET's double gates allows significant reduction in leakage current.

5.3 FinFET Structures

The figures of the FinFET are as follows: -

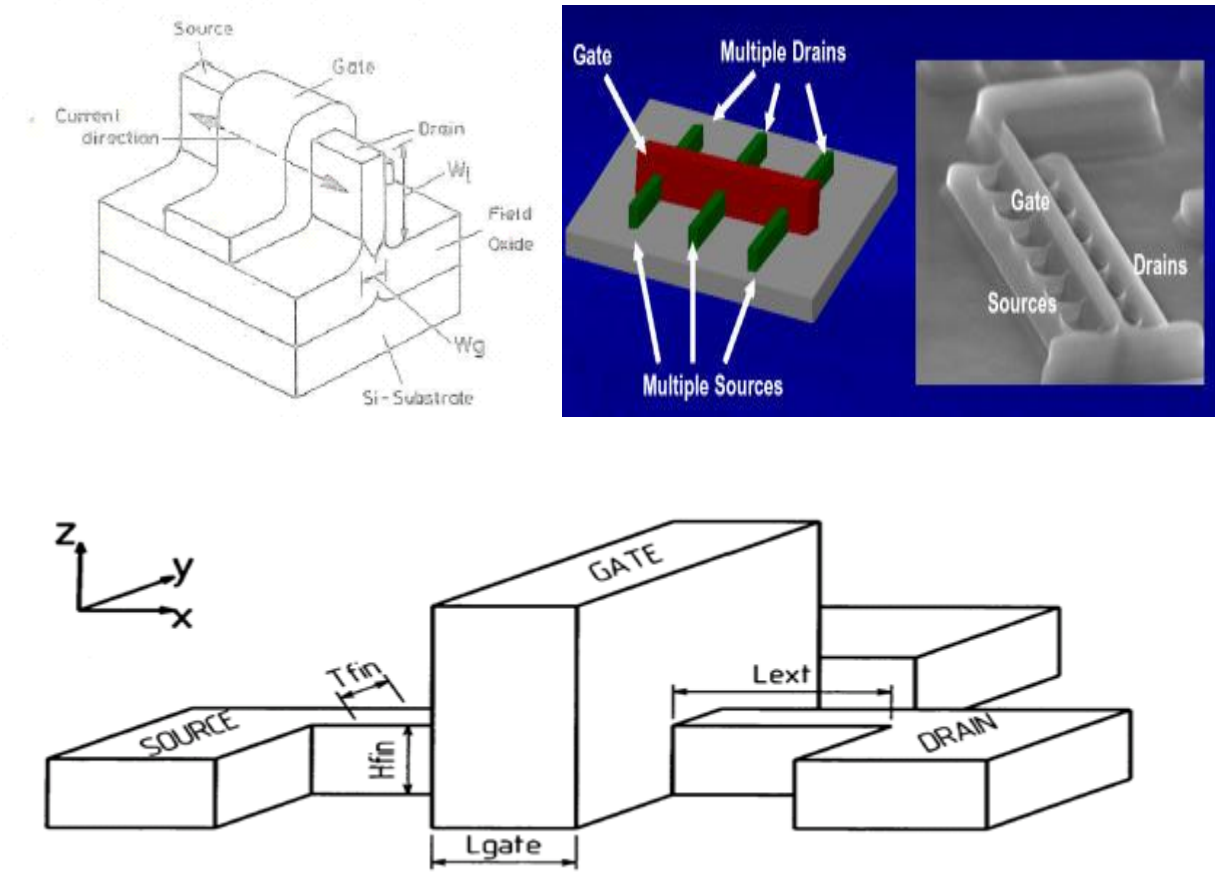


Fig. 5.3.1(Schematic 3D figures of FinFET)

CHAPTER-VI

RESULTS AND DISCUSSION

6.1 Simulation Results

We hereby conclude that, the simulations of CMOS logic inverter using MATLAB, P-Spice and T-Spice were done and results were shown in the previous sections.

6.2 Comparison of Results

We also measured the time delay of MOSFET, in different outputs performed in different soft wares. The time delay of the standard MOS using P-Spice were calculated and the time delay of MOS whose parameters were changed and calculated.

6.2.1 Nano CMOS simulated from T-Spice:

Frequency at which it is operated= 10 MHz,

V_{DD}= 10 V

Capacitance= 8.28 pF

Power Dissipated= 0. 828 µW.

6.2.2 CMOS simulated from P-Spice:

Frequency at which it is operated= 5 MHz,

V_{DD}= 10 V.

Capacitance=15 pF.

Power Dissipated= 7.5mW.

6.3 Comparision

Parameter	**CMOS**	**Nano-CMOS**
Frequency	5 MHz	10 MHz
V_{DD}	10 V	10 V
Capacitance	15 pF	8.28 pF
Power Dissipated	7.5 mW	0. 828 µW
Length	16 µm	40 nm
Width	25 µm	60 nm
Time delay	0.02 µs	0.4 ns

Hence, it shows that it would be more efficient to use nano-CMOS and we can further improve performance through FinFET which promises to replace traditional MOS and it will make more efficient, faster and reliable.

CHAPTER-VII

CONCLUSION

7.1. CONCLUSION

Each nano-transistor is consuming very less power in comparison to the bulk ones. And hence in the IC chip consisting of more no of MOSFET will consume less power and give more efficiency.

Downsizing of MOSFET results in

1) Reduce capacitance.

2) Reduce switch time of MOSFET.

3) Reduce power consumption.

4) Increase no of transistors.

5) Increase functionality.

6) Parallel Processing.

7) Increase Circuit Operation Speed.

Thus downscaling of Si devices is very essential and it very much enhances the performance of the device in terms of power consumption, speed, etc.

And as per Moore's Law, the no of transistors to be fabricated in an IC chip increases exponentially. Thus, device can operate faster with more no of transistors.

FinFET due to its fast operation, low power consumption, smaller size so that more no of transistors can be accommodate in a single IC chip. Being very fast operating device, low power consuming, and very tiny, the device is best option for our future applications. The no of transistor fabricated in single IC will be very large in no., if we use FinFET.

CHAPTER-VIII

FUTURE WORK

8.1 Applications

Some of the nano-CMOS are DG-MOSFET, FinFET, DG-FinFET, ultra-small MOSFETs, SiGe HBTs. These can be used for different applications in the world of electronics, such as SD-RAM and Processors, etc. and also in mobile technology.

It is also used in Low Power Applications of CMOS circuits.

Hence, the Nano-Technology based MOSFET replace the bulk CMOS and will make the computer-era faster and more reliable. It will bring revolution in the world of communication and electronics, as everything is digitalized and depends on transistors. Even a small digital clock needs timer circuits for its operation and also a computer processor, RAM etc.; they too need transistor for operation.

FinFET advantages over bulk MOS are, it is very small in size, low power consuming, fast operating, and it also has same fabrication process as a MOSFET. FinFET being very small in size, more no can be fabricated in a single IC chip. And works are going on to make the transistor in nano range so as to check some of the problems caused by small scaling such as Power Density, temperature etc.

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