Design of MP3 Player Application with Nios II Embedded Evaluation Kit, Cyclone III Edition

A Project Report

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CERTIFICATE

This is to certify that the thesis entitled, "**Design of MP3 Player application with Nios II Embedded Evaluation Kit, Cyclone III Edition**" submitted by **Ms. Sowmya Ratna Patibandla, 10609024** and **Mr. Jagdeep, 10609005** in partial fulfillments for the requirements for the award of Bachelor of Technology Degree in Electronics & Communication Engineering at National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by them under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

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ABSTRACT

A **MPEG-1 Audio Layer 3**, commonly referred as **MP3**, is a patented digital audio encoding format using a form of lossy data compression . A **field-programmable gate array** (**FPGA**) is an integrated circuit designed to be configured by the customer or designer. We are aiming at implementing a MP3 Player application with the FPGA based Nios II Embedded Evaluation Kit, Cyclone III Edition. Implementation of MP3 Player can be done by first instantiating a Nios II system in the board. Nios II system can be build around the altera's Nios II processor using the SOPC builder tool of the quartus II CAD tool. The SOPC builder tool generates the VHDL code of the defined system. Thus we get two files .SOF & .ELF from them we get flash files. Upload of these files on SD Card of kit initiates the application.This upload can be done in two ways ,

1.In system SD Card update,

2.Remote system update.

Thus the application is uploaded and mp3 files can be played on the kit. Specified controls like skip, pause, play, volume ,balance are also has to be implemented

Chapter1

Introduction

INTRODUCTION

Today there are lot many embedded based kits available. Applications based on FPGA implementations are highly working projects. Nios II Embedded Evaluation Kit, Cyclone III Edition is one of best embedded evaluation kit for research work. Many applications can be implemented on this kit, one of those is MP3 Player. In today's life MP3 Player has vast role for entertainment, & there lies wonderful technology behind it. In this work, we study abut the board and have to implement MP3 Player application on Nios II Embedded Evaluation Kit.

1.1 FPGA:

A **field-programmable gate array** (**FPGA**) is an integrated circuit designed to be configured by the customer or designer after manufacturing, hence called field-programmable. The FPGA configuration is generally specified using a hardware description language(HDL). FPGAs can be used to implement any logical function. The ability to update the functionality after shipping, partial re-configuration of the portion of the design and the low non-recurring engineering costs r offer advantages for many applications.

FPGAs contain programmable logic components called logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be wired. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

Many hardware designs can be implemented using this FPGA, Various development boards are designed for this implementation. One of such kits is Nios II Embedded Evaluation Kit, Cyclone III Edition. It has specific characteristics of having many applications which can be accessed easily. The details of the kit are discussed in the next chapter. The application that is designed and discussed over here is MP3 Player.

1.2 MP3 Player:

MPEG-1 Audio Layer 3, commonly referred as **MP3**, is a patented digital audio encoding format using a form of lossy data compression. But it is a common audio format for consumer audio storage, and a de facto standard of digital audio compression for the transfer and playback of music on digital audio players.

MP3 is an audio-specific format that was designed by the Moving Picture Experts Group as part of its MPEG-1 standard. The group is of several teams of engineers at Fraunhofer IIS, AT&T-Bell Labs, Thomson-Brandt, CCETT, and many other. It was approved as an ISO/IEC standard in 1991.

The use of a lossy compression algorithm in MP3 is designed to reduce the amount of data required for representation of the audio recording and sounds like a faithful reproduction of the original uncompressed audio for most listeners. An MP3 file, created using the setting of 128 kbit/s results in a file that is around 11 times smaller than the CD file created from the original audio source. It can also be constructed at lower or higher bit rates, with lower or higher resulting quality.

The compression works by reducing accuracy of certain parts of sound that are deemed beyond the auditory resolution ability of most people. This method is commonly referred to as perceptual coding.[5] It uses psychoacoustic models to discard or reduce precision of components less audible to human hearing, and then records the remaining information in an efficient manner.

This technique is often presented as relatively conceptually similar to the principles used by JPEG, an image compression format. However, the specific algorithms are different: JPEG uses a built-in vision model (very widely tuned, as is required for images), while MP3 uses a complex, precise masking model that is much more signal dependent.

Chapter 2

Hardware profile

HARDWARE PROFILE

2.1 Nios II Embedded Evaluation Kit, Cyclone III Edition:

Success for an embedded system start rights from the evaluation stage. Choosing the right platform, development tools, operating systems may be the difference between success and failure. The Altera Nios II Embedded Evaluation Kit, Cyclone III Edition is an evaluation kit that enables you to make these critical decisions with minimal investment.

The Altera® Nios II Embedded Evaluation Kit, Cyclone III Edition includes a full-featured field-programmable gate array (FPGA) development board, LCD Multimedia High Speed Mezzanine Card (HSMC), hardware and software development tools, documentation, and accessories needed to begin embedded and system on a programmable chip (SOPC) designs using FPGAs.

The development board includes an Altera Cyclone III FPGA and comes preconfigured with an FPGA hardware reference design stored in flash memory as well as several Ready-to-Run demonstration applications stored on the SD-Card Flash provided. Hardware designers can use the FPGA reference design as a platform to build complex embedded systems. Software developers can use the hardware reference design plus sample software applications as a starting point for their own applications.

Fig.1: NIOS II EMBEDDED EVALUATION KIT, CYCLONE III EDITION

2.1.1 Features of Kit:

The Nios II Embedded Evaluation Kit include below features:

- Cyclone III Starter Board

- Cyclone III EP3C25F324 FPGA
- Configuration
    - Embedded USB-Blaster™ circuitry (includes an Altera EPM3128A CPLD) allowing download of FPGA configuration files via the users USB port
- Power and analog devices from Linear Technology
- Memory
    - 256-Mbit DDR SDRAM
    - 1-Mbyte Synchronous SRAM
    - 16-Mbytes Intel P30/P33 flash
- Clocking
    - 50-MHz on-board oscillator
- Switches and indicators
    - Six push buttons total, 4 user controlled
    - Four user-controlled LEDs

■ LCD Daughtercard

- LCD Touch-screen Display
    - 800 X 480 pixel size
- 10-bit VGA DAC
- Video Decoder
- 24-bit Audio Codec

- RS232 transceiver
- SD Flash
- 10/100 Mbps Ethernet Controller (PHY)
- Connectors
    - VGA Output
    - Composite Video in
    - Serial connector (RS-232 DB9 port)
    - PS/2
    - Ethernet Connector (RJ 45)
    - SD Card Socket

2.1.2 About the Nios II Processor:

Nios II is a fully configurable 32-bit processor optimized for use in Altera's FPGA. The embedded processor system is easily customized for a particular application using the SOPC Builder feature of the Quartus II FPGA design software.

Assembling a microprocessor system involves four elements:

1. Adding and configuring of the core processor and memory

2. Adding peripherals such as memory interfaces, I/O, or interfaces to external devices (such as the LCD Display)

3. Connecting the I/O pins of the processor in the FPGA to the external devices

4. Writing C/C++ software application for your custom processor with the Nios II Embedded Design Suite.

In the vast majority of cases, hardware design can be accomplished using drop-down menus and drag and drop operations in SOPC Builder. The sophistication of Altera's designs tools brings creating custom hardware processor systems within the reach of embedded developers.

2.1.3 About the Nios II Standard Design:

Nios II "standard" is a SOPC Builder system featuring the Nios II processor and common peripherals that has been put together. Hardware designers can accelerate their SOPC Builder system development by using the Nios II Standard design example as a starting point. The board boots up with this pre-built design, so software developers can use it for software development without having to concern themselves with the details of generating the FPGA hardware system. The Nios II Standard System is a pre-generated hardware system that includes:

- Nios II core (32-bit soft processor) Application
- LCD Controller
- Multi-port memory controlle
- Communication Interface controllers

Nios II system design builds upon a NIOS II processor system by including a software application that runs on the processor system.

2.1.4 Blocks of Kit:

Nios II Embedded Evaluation Kit, Cyclone III Edition is comprises of 2 boards

- the Cyclone III FPGA Starter Board
- the LCD Multimedia Daughtercard.

On the Cyclone III FPGA Starter board resides the Cyclone III 3c25 FPGA which configures from flash with the Nios II Standard Processor System on startup.

The HSMC Connector is actually a flex extension cable with HSMC connectors on each end going between the two boards. This detail was removed for simplicity.On the LCD Multimedia Daughtercard resides a MAX II CPLD whose function is to relay data and control signals to the various peripheral devices. The MAX II CPLD performs voltage translation and de-multiplexing of video pipeline signals to the LCD Touch panel. The video pipeline signals have been multiplexed inside the FPGA and de-multiplexed by the MAX II CPLD to provide a full range of functionality on the daughter card over a limited number of pins on the HSMC connector.

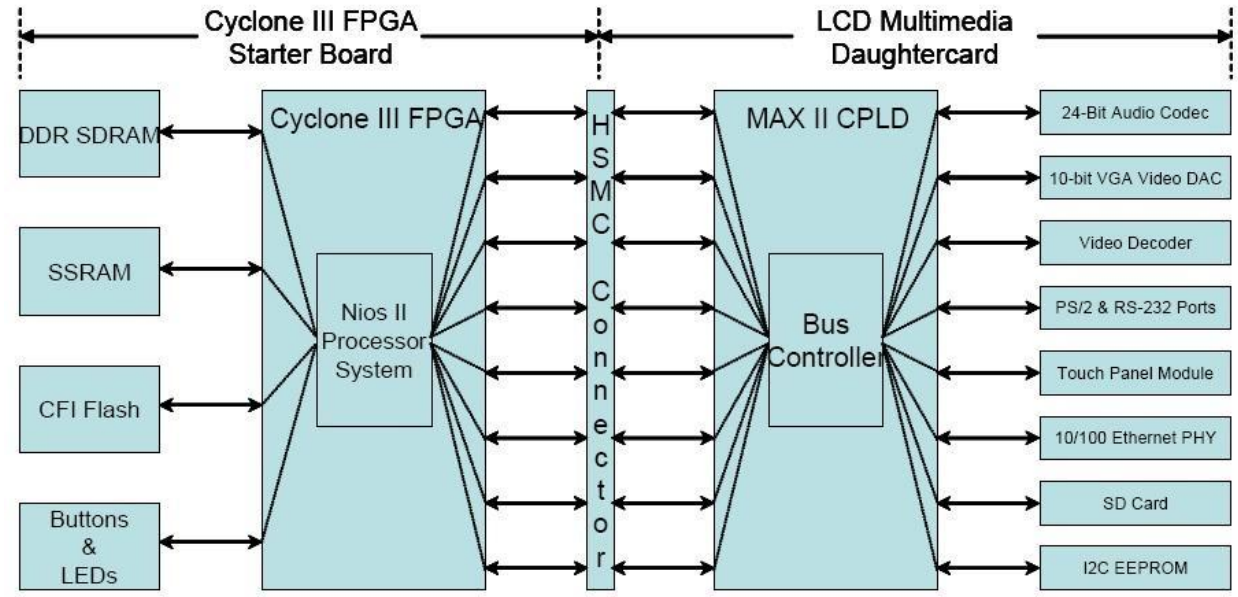

Fig. 2 : BLOCK DIAGRAM OF NIOS II EMBEDDED EVALUATION KIT, CYCLONE III EDITION

2.2 INTERFACING:

The interfacing of design to the kit is mainly done by different methods. Main interfacing is done using application selector utility.

2.2.1 Application Selector Utility :

The application selector is the default utility that boots up on power on and allows users to quickly select, load, and run different Ready-to-Run applications or demos stored on an SD Card using the LCD touch panel.

An application consists of a FPGA hardware image and an application software image. When you select an application the application selector copies these images from the SD Card to the Flash memory and reconfigures the FPGA with our selection.

In addition to the pre-packaged Ready to Run SD Card Demo applications which come with the Nios II Embedded Evaluation Kit, Cyclone III Edition, more are available from Altera or through third party vendors. you can easily convert your own applications to be loadable by the application selector. There are a couple of ways the application selector can update your board.

- In system update via the on board SD Card
- Remote-System Update via Ethernet

2.2.2 Menu of Application Selector:

- Altera Picture Viewer
- Altera Mandelbrot C2H
- Altera Web Server
- Altera Spinning Cube
- Imagem Taquin Game

2.2.3 In system update using SD Card:

To run the applications , load and view demos stored on SDCard , we can use in system update and have to follow below instructions.

1, Connect power to Nioos II Embedded Evaluation Kit, Cyclone III Edition.

2, Switch ON the power (using SW1)

If board is already powered, reset the board by pressing reconfigure button, then the application selector boots from splash & a splash screen appears, while application selector is searching for applications on SDCard.

Fig . 3: Application selector window on Kit

3, To highlight the selection of application , just have to touch it.

List can be viewed completely by scrolling through the window using Scroll Up and Scroll Down buttons on the right hand side of screen.

4, For every application there is certain information about it & this can be viewed by highlighting the specified application by touching it, then touching the button labeled "Info". To return to the main menu, have to touch button "OK".

5, To load & run the application, touch button "Load". Loading begins and a small window showing progress is displayed. It may take 2 to 30 mins for loading depending on the size of the application and also whether it was previously cauched in on board flash memory.

2.2.4 Remote System update via Ethernet:

FPGA has capability for remote reconfiguration, thus it allows to update our system with a new FPGA image as long as there is persistent Ethernet Connection.

Requirements:

1, A host PC with a connection to a working Ethernet port

2, A separate working Ethernet port to connect the board.

3, Flash files for software & hardware images of specified application to update the board with. These files must present on host PC.

The .flash file format is an SREC file with addressing offset from the base address of our flash device, for this ext_flash device is used.

Instructions:

1, Apply power to the board using power cable and switch SW1.

The application selector appears on LCD screen , on right bottom there is a button “NOT CONNECTED”, just touching it we can see remote system update instructions.

2, Connect an Ethernet cable to a pin RJ-45 on the LCD Multimedia HSMC to a working network.

3, Have to wait , while webserver application establishes a connection to interent and acquires an IP Address via DHCP. After completion, the IP Address will display on LCD Screen.

4, Ensure that even host PC is connected to working Ethernet port & launches a web browser.

5. In web browser window, have to type the IP Address displayed on the LCD screen & ‘enter’.

6, A web page is served, on the upper left side on the form there is a link under Go to instructions, clicking this we will be directed to the remote configuration instruction page and then follow the instructions.

7, On the left hand side of web page , there is CFI flash upload section. Click browse button & browse to the hardware flash image on host PC & click open.

8, On web page click upload, when upload is completed we will be directed to another web form entitled program CFI flash.

9, Click on program flash button to program the on board flash with the uploaded flash image.

10, If we have software flash image also then click return to instructions and repeat the previous 3 steps to upload & program software flash.

11, Then click on Reset System button . The FPGA will now reconfigure from the newly programmed contents of flash file.

2.2.5 Creating Flash files for System update:

The image required for system update consists of a Flash image for FPGA configuration and if system has a software application then it consist of a Flash image for the software application. To create the flash files we must have the Nios II EDS and Quartus II FPGA design software installed on your PC.

■ A hardware SRAM object file (*.SOF) must have the cpu reset address configured from the Flash device at offset 0x0.

■ Have to create the software Executable link format file (ELF) in the standard fashion.

■ On host PC, launch a Nios II Command Shell from **Start -> Programs -> Altera -> Nios II** <*version #*> **EDS -> Nios II Command Shell**

■ From the command shell navigate to where required SOF file is located and create corresponding hardware Flash image using the following command:

sof2flash --activeparallel --input=”our SOF.sof”

--output=”our SOF.flash” --

offset=”RECONFIG_ADDRESS”

■ From the command shell navigate to where required ELF file is located and create corresponding software Flash image using the following command:

elf2flash --base=0x04000000 --end=0x04FFFFFF --

reset=0x04240000 --input=”our ELF.efl” --

output=”our FLASH.flash”

-- boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_ loader_cfi.srec

Chapter3

Design Analysis

Design Analysis:

3.1 Shipping of Design:

To ship a design as an application , we use

Application Selector based on processor system.

Location of the design: <*install dir*>/examples/application_selector

Description: Video, Ethernet and SD Card controller based processor system for LCD Color touch panel control, in-system update using SD Card, remote system update using Ethernet

3.1.1 IP licenses required to ship design:

- SD/MMC SPI Core IP (with FAT file system) from El Camino
- Triple Speed Ethernet-MAC Core license from Altera (Ordering code IP-TRIETHERNET)
- Nios II IP evaluation license with Nios II EDS, shipping license from Altera (Ordering Code IP-NIOS)
- DDR SDRAM memory controller core shipping license from Altera (comes free with Quartus II Subscription edition as part of Altera IP Base Suite)

3.1.2 Software and middleware licenses required to ship design:

- NicheStack TCP/IP Network Stack, Nios II Edition free evaluation license available with Nios II EDS, shipping license from Altera (Ordering Code IPSW-TCP/IP-NIOS)
- MicroC/OS-II real time operating system free evaluation license available with Nios II EDS, shipping license to be purchased frombMicrium

The full design example for the application selector utility is available in Nios II Embedded Evaluation kit installed under the examples directory.

The application selector design examples illustrates several aspects of developing designs and using software device drivers for the Nios II Embedded Evaluation Kit.

- Interfacing to the LCD touch panel
- Interfacing to the SD Card using the FAT file system
- Implementing a HTTP web server application using the sockets interface of NicheStack TCP/IP Network Stack, Nios II Edition
- Implementing remote system update over Ethernet
- Managing multiple FPGA configurations from Flash
- Using the MicroC/OS-II real time operating system

3.2 Required files for loadable application:

Each loadable application consists of two flash files, and an optional text file, all stored on an SD Card.

- The first flash file represents the software portion of the example and must be derived from an .ELF file as described .This flash file can be named anything supported by the FAT16 file system, the only restriction being that the name must end with *_sw.flash*.
- The second flash file represents the hardware portion of the example and must be derived from a *.SOF* file as described .This file can be named anything supported by the FAT 16 file system, the only restriction being that the name must end with *_hw.flash.*
- The optional **info.txt** file contains additional information about the application. In the application selector utility, touching the "Show Info" button while our application is highlighted, brings up a window showing the text contained in this file. The name of this text file must be *info.txt*, or the application selector will not recognize it.

3.3 SD Card Directory Structure

All loadable applications on the SD Card must be located in a top-level Directory named Altera_EEK_Applications. Under the Altera_EEK_Applications directory, each application is located in its own subdirectory. The name of that subdirectory is important because the application selector utility uses that name as the title of the application when displaying it in the main menu. The name of the subdirectory is the title that will be displayed for your application in the menu. The subdirectory names can be anything so long as they adhere to the FAT file system long file name rules. Spaces are permitted.

3.4 Design Worked & Observations:

3.4.1 MP3 Player:

Other than this specified application, Nios II Embedded Evaluation Kit can be used for many other various designs and applications. To make it as one of the application and to play MP3's on kit, we have to follow the instructions:

1, We have to create a directory on the SD Card named MP3/media.

2, Have to dump all selected MP3s in that directory, they can be in separate subdirectories also.

3, Have to copy .flash files related to MP3 application to the SDCard directory/ Altera_EEK_application /MP3 Player.

4, Thus load the MP3 player with the application selector.

3.4.2 Way it work:

The player will recursively scan the MP3/media directory and build a database of all the MP3 files and verifies also. This takes time.Then it starts playing.

Any time we can play and change the MP3 files on the card (or the player fails to open one it has in its database) it will rescan the /MP3/media directory and rebuilds the database.

3.4.3 Controls implemented in this application:

- Skip
- Play
- Pause
- Touching the progress bar will skip the song to that place
- Touching vol or bal to change volume or for left right balance
- Touch and release a song in the playlist to begin playing that song
- Touching the scroll bar n the playlist, it scrolls through the playlist
- Touch the scroll bar in the now playing window to see more information about that song
- Touch Random or repeat to enable thse functions.

The player is not a bug free but seems to pretty stable.

Thus we have touch controlled MP3 Player.

Fig. 4 Mp3 Player application on Nios II embedded evaluation kit

Chapter 4

Conclusion

Conclusion:

The design of MP3 Player application was successfully implemented. Audio can be listened through 24-bit audio codec out pin with any speakers. But there are certain problems in this application like the player fails to open the files that it has in its database. Still it has many vast applications like Network MP3 player which can be used Public broadcasting, CD audio player in music store and many more shopping malls etc.

There are lot many applications and hardware designs that can be implemented in this kit, NIOS II EMBEDDED EVALUATION KIT, CYCLONE III EDITION. This is the best student friendly kit which can be used in labs for developing realtime knowledge of FPGA implementations.

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