



# **POWER FACTOR CORRECTION USING PARALLEL BOOST CONVERTER**

**A thesis submitted in partial fulfillment of the requirements for the  
Degree of**

**BACHELOR OF TECHNOLOGY**

**IN**

**ELECTRICAL ENGINEERING**

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# National Institute of Technology Rourkela

## CERTIFICATE

This is to certify that the project entitled, **“POWER FACTOR CORRECTION USING PARALLEL BOOST CONVERTER”**

submitted by Miss Roma Dash is an authentic piece of work carried out by her under our supervision and guidance for the partial fulfillment of the requirements for the award of **Bachelor of Technology Degree in Electrical Engineering at National Institute of Technology, Rourkela.**

To the best of my knowledge, the matter embodied in the project has not been submitted to any other University / Institute for the award of any Degree or Diploma

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## **ABSTRACT**

Power Factor, the ratio between the real or average power and the apparent power forms a very essential parameter in power system. It is indicative of how effectively the real power of the system has been utilized.

With rapid development in power semiconductor devices, the usage of power electronic systems has expanded to new and wide application range that include residential, commercial, aerospace and many others. Power electronic interfaces e.g. switch mode power supplies (SMPS) have proved to be superior over traditional linear power supplies. However, their non-linear behaviour puts a question mark on their high efficiency. The current drawn by the SMPSs from the line is distorted resulting in a high Total Harmonic Distortion(THD) and low Power Factor(PF).

Individually, a device with harmonic current does not pose much serious problem however when used on a massive scale the utility power supply condition could be deteriorated. Other adverse effects on the power system include increased magnitudes of neutral currents in three-phase systems, overheating in transformers and induction motors etc.

Hence, there is a continuous need for power factor improvement and reduction of line current harmonics. Development of new circuit topologies and control strategies for Power Factor Correction (PFC) and harmonic reduction has become still more essential with the introduction of strong technical IEC standards.

This project aims to develop a circuit for PFC using active filtering approach by implementing two boost converters arranged in parallel. It shall be based on an optimised power sharing strategy to improve the current quality and at the same time reduce the switching losses.

The work initially involves simulation of basic power electronic circuits and the analysis of the current and voltage waveforms. It starts with simple circuits with a gradual increase in complexity by inclusion of new components and their subsequent effect on the current and voltage waveforms. We focus on the objective of improving the input current waveform i.e. making it sinusoidal by tuning the circuits.

All the simulation work is done in MATLAB Simulink environment and the results are attached herewith.

## **ACKNOWLEDGEMENT**

On the submission of my thesis report of “**Power Factor Correction using parallel boost converter**”, I would like to extend my gratitude & my sincere thanks to my supervisor **Prof. A K Panda**, Professor, Department of Electrical Engineering for giving me the opportunity to work in the field of PFC. The idea of using parallel boost converters being new in itself, gave enough scope of research oriented study. I am indebted to him for having helped me shape the problem and providing insights towards the solution.

I would like to thank research scholars in the Power Electronics Lab (Suresh Sir) and a few other students (Asima, Aurabind) of our institute whose invaluable tips came handy in obtaining the correct simulation results and will definitely be useful in the days to come.

I am thankful for the constant moral support of my friends and family without which this work would have been impossible .

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## CHAPTER 1: INTRODUCTION

### 1.1 POWER FACTOR:

Power factor is defined as the cosine of the angle between voltage and current in an ac circuit. There is generally a phase difference  $\phi$  between voltage and current in an ac circuit.  $\cos \phi$  is called the power factor of the circuit. If the circuit is inductive, the current lags behind the voltage and power factor is referred to as lagging. However, in a capacitive circuit, current leads the voltage and the power factor is said to be leading.

In a circuit, for an input voltage  $V$  and a line current  $I$ ,

$VI \cos \phi$  –the active or real power in watts or kW.

$VI \sin \phi$ - the reactive power in VAR or kVAR.

$VI$ - the apparent power in VA or kVA.

Power Factor gives a measure of how effective the real power utilization of the system is. It is a measure of distortion of the line voltage and the line current and the phase shift between them.

Power Factor=Real power(Average)/Apparent power

Where, the apparent power is defined as the product of rms value of voltage and current.

### **LINEAR SYSTEMS:**

In a linear system, the load draws purely sinusoidal current and voltage, the current and voltage, hence the power factor is determined only by the phase difference between voltage and current.

i.e.  $PF = \cos\theta$

### **POWER ELECTRONIC SYSTEMS:**

In power electronic system, due to the non-linear behaviour of the active switching power devices, the phase angle representation alone is not valid. A non linear load draws typical distorted line current from the line. The PF of distorted waveforms is calculated as below:

The fourier representation for line current  $i_s$  and line voltage  $v_s$  are given by,

$$i_s = I_{DC} + \sum I_{sn} \sin(n\omega t + \theta)$$

$$v_s = V_{DC} + \sum V_{sn} \sin(n\omega t + \theta)$$

The line current is non-sinusoidal when the load is nonlinear. For sinusoidal voltage and non-sinusoidal current the  $PF$  can be expressed as

$$PF = \frac{V_{rms} I_{1rms}}{V_{rms} I_{rms}} \cos \Phi = \frac{I_{1rms}}{I_{rms}} \cos \Phi = K_p \cos \Phi$$
$$K_p = I_{1,rms} / I_{rms}, K_p \in [0,1]$$

Where,  $\cos\Phi$  is the displacement factor of the voltage and current.

$K_p$  is the purity factor or the distortion factor.

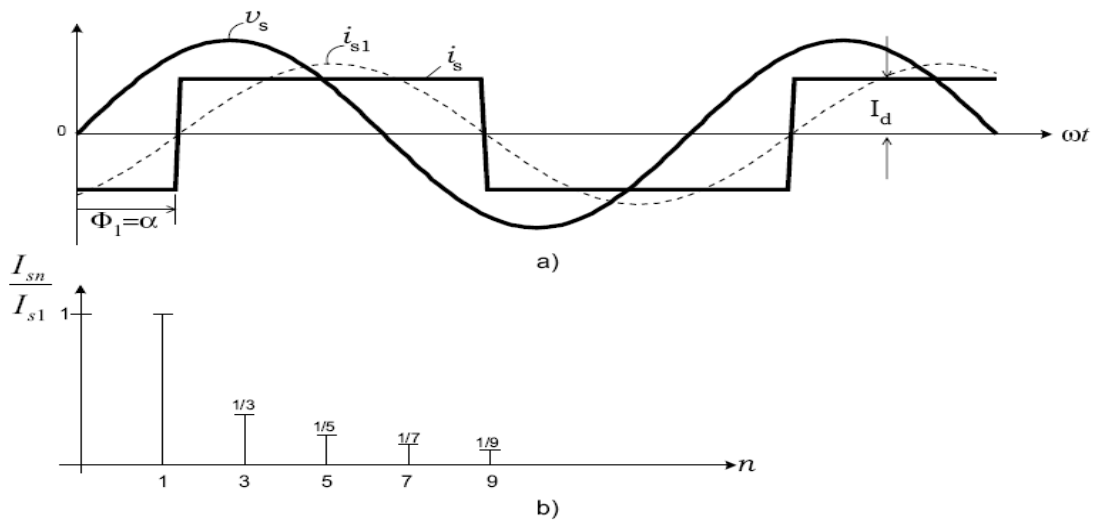


Figure 1.1: Input current of a single phase bridge rectifier [2]

(a) Waveforms (b) harmonics spectrum

Another important parameter that measures the percentage of distortion is known as the current total harmonic distortion ( $THD_i$ ) which is defined as follows:

Hence the relation between  $K_p$  and  $THD_i$  is

$$K_p = \frac{1}{\sqrt{1 + THD_i^2}}$$

$$THD_i = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{1,rms}}$$

## **1.2 HARMONICS:**

Switching converters of all types produce harmonics because of the non-linear relationship between the voltage and current across the switching device. Harmonics are also produced by “conventional” equipment including:

- 1) Power generation equipment(slot harmonics).
- 2) Induction motors(saturated magnetics).
- 3) Transformers (overexcitation leading to saturation)
- 4) Magnetic-ballast fluorescent lamps (arcing) and
- 5) AC electric arc furnances.

All these devices cause harmonic currents to flow and some devices, actually, directly produce voltage harmonics.[2]

## **1.3 AFFECTS OF HARMONICS ON POWER QUALITY**

The contaminative harmonics can decline power quality and affect system performance in several ways:

- 1) Conductor loss and iron loss in transformers increase due to harmonics decreases the transmission efficiency and causes thermal problems.
- 2) The odd harmonics in a three phase system overload of the unprotected neutral conductor.
- 3) High peak harmonic currents may cause automatic relay protection devices to mistrigger.
- 4) Excessive current in the neutral conductor of three-phase four-wire systems, caused by odd triple-n current harmonics (triple-n: 3<sup>rd</sup>, 9<sup>th</sup>, 15<sup>th</sup>, etc.). This

leads to overheating of the neutral conductor and tripping of the protective relay.

- 5) Telephone interference and errors in metering equipment
- 6) The line rms current harmonics do not deliver any real power in watts to the load, resulting in inefficient use of equipment capacity(i.e. low power factor).
- 7) Harmonics could cause other problems such as electromagnetic interference to interrupt communication, degrading reliability of electrical equipment, increasing product defective ratio, insulation failure, audible noise etc..[2]

#### **1.4 THE PROBLEM OF POWER FACTOR IN SINGLE PHASE LINE COMMUTATED**

##### **RECTIFIERS:**

Classical line commutated rectifiers suffer from the following disadvantages :

- 1) They produce a lagging displacement factor w.r.t the voltage of the utility.
- 2) They generate a considerable amount of input current harmonics.

These aspects negatively influence both power factor and power quality. The massive use of single-phase power converters has increased the problems of power quality in electrical systems.

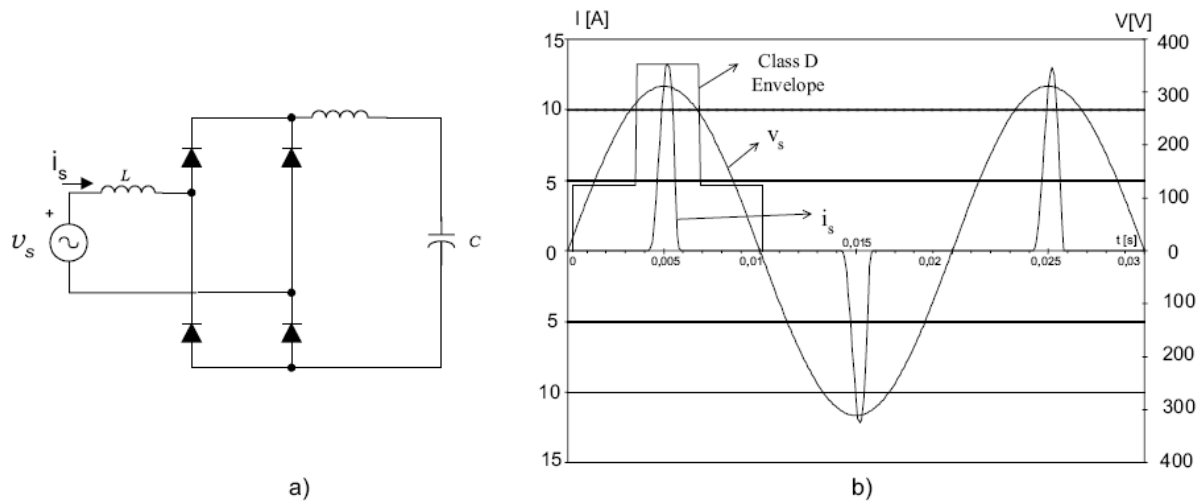


Figure 1.2 :Single phase rectifier (a) circuit (b) waveforms of input voltage and current[2]

### **1.5 STANDARDS FOR HARMONICS IN SINGLE PHASE RECTIFIERS:**

The relevance of the problems originated by harmonics in single-phase line-commutated rectifiers has motivated some agencies to introduce some restrictions to these converters. Standardization activities in this area have been carried out for many years. As early as 1982, the International Electro-technical Committee-IEC published its standard IEC 555-2, which was also adopted in 1987 as European standard EN 60555-2, by the European Committee for Electro-technical Standardization - CENELEC. Standard IEC 555-2 has been replaced in 1995 by standard IEC 1000-3-2 [1], also adopted by CENELEC as European standard EN 61000-3-2.

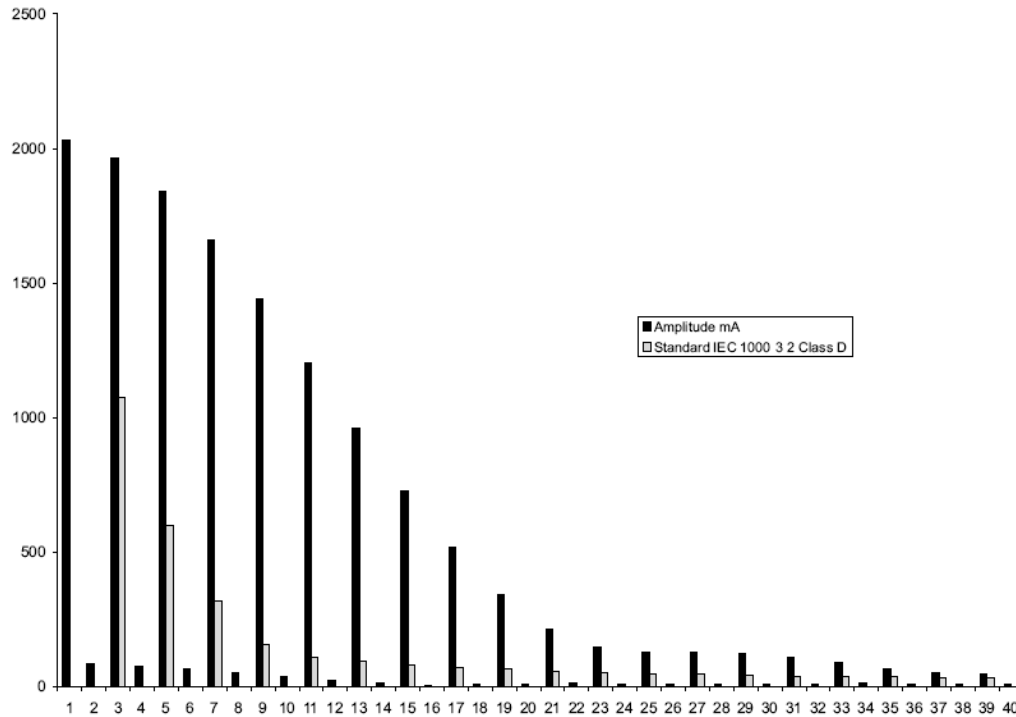


Figure 1.3: Input current harmonics produced by a single-phase diode bridge rectifier compared against IEC standards[2]

**Standard IEC 1000-3-2:**

1. It applies to equipment with a rated current up to and including  $16A_{rms}$  per phase which is to be connected to 50Hz or 60 Hz,  $220-240V_{rms}$  single-phase or  $380-415V_{rms}$  three-phase mains.
2. Electrical equipments are categorized into four classes(A, B, C, and D), for which specific limits are set for the harmonic content of the line current.
3. These limits do not apply for the equipment with rated power less than 75W, other than lighting equipment



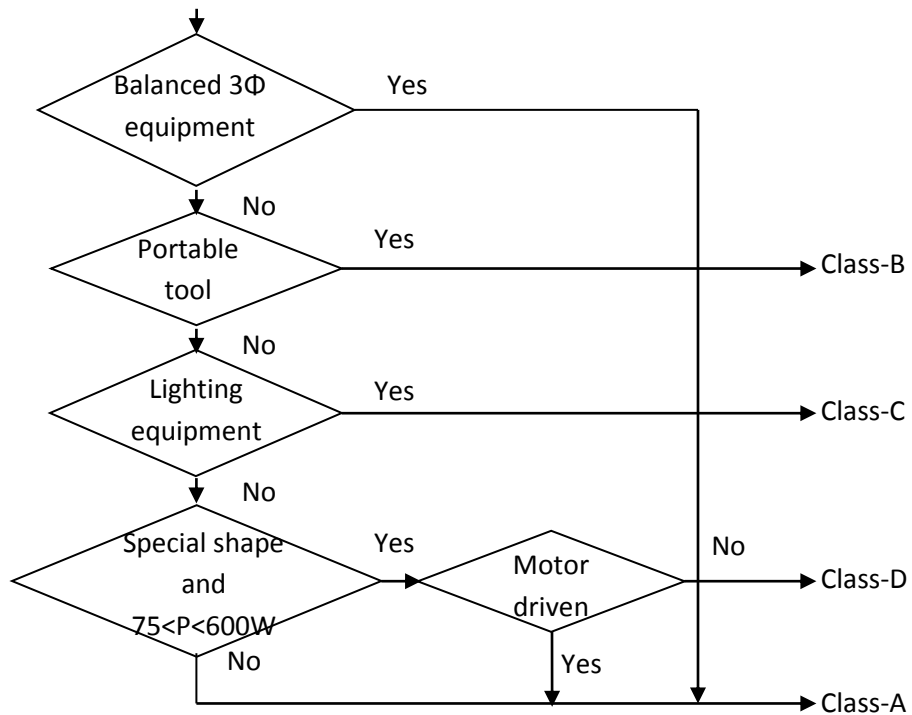


FIGURE 1.4: Flowchart showing the Classification of equipment under Standard IEC 1000-3-2

CLASS-A:

It includes balanced three-phase equipments, household appliances, excluding the equipment identified as class-D. Equipment not specified in one of the other three classes should be considered as class-A equipment.

CLASS-B:

It includes portable tools, and non-professional arc welding equipment.

### CLASS-C:

It includes lighting equipment (except for dimmers for incandescent lamps, which belong to class-A).

### CLASS-D:

Equipment with special line current shape i.e. includes equipment having an active input power less than or equal to 600w, of the following types:

- i. Personal computers.
- ii. Personal computer monitors.
- iii. Television receivers.

The classification can also be represented using the flowchart: Fig: 1.2

### Limits in standard IEC 1000-3-2:

Besides standard IEC 1000-3-2, there are also other documents addressing the control of current harmonics. Standard IEC/TS 61000-3-4 gives recommendations applicable to equipment with rated current greater than  $16A_{rms}$  per phase and intended to be connected to 50Hz or 60Hz mains, with nominal voltage up to  $240V_{rms}$  single-phase, or up to  $600V_{rms}$  three-phase.

Table 1.1(a): Limits for Class-A and Class-D

Table 1.1(b): Limits for Class-B and C

Harmonic order	Class-A	Class-D	
	$A_{rms}$	$A_{rms}$	$mA/W$
3	2.30	2.30	3.40
5	1.14	1.14	1.90
7	0.77	0.77	1.00
9	0.40	0.40	0.50
11	0.33	0.33	0.35
13	0.21	0.21	0.29
15 to 39	$2.25/n$	$2.25/n$	$3.85/n$
2	1.08		
4	0.43		
6	0.30		
8 to 40	$1.84/n$		

odd harmonics

Even harmonics

Harmonic order	Class-B	Class-C
	$A_{rms}$	%
3	3.45	30*PF
5	1.71	10
7	1.15	7
9	0.60	5
11	0.49	3
13	0.31	3
15 to 39	$3.375/n$	3
2	1.62	2
4	0.64	
6	0.45	
8 to 40	$2.76/n$	

odd harmonics

Even harmonics

## **Standard IEEE 519-1992**

Gives recommended practices and requirements for harmonic control in electrical power systems for both individual consumers and utilities. The limits for line current harmonics are given as a percentage of the maximum demand load current  $I_L$  at the point of common coupling-PCC at the utility. They decrease as the ratio  $I_{SC}/I_L$  decreases where  $I_{SC}$  is the maximum short circuit current at PCC, meaning that the limits are lower in weaker grids. This standard covers also high voltage loads of much higher power.

### **Limits in standard IEEE 519-1992**

Table 1.2: Odd harmonic limits

$I_{SC}/I_L$ (%)	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	TDD*
<20	4.0	2.0	1.5	0.6	0.3	5
20 to 50	7.0	3.5	2.5	1.0	0.5	8
50 to 100	10.0	4.5	4.0	1.5	0.7	12
100 to 1000	12.0	5.5	5.0	2.0	1.0	15
>1000	15.0	7.0	6.0	2.5	1.4	20

\*TDD: Total Demand Distortion is the harmonic current distortion in % of a maximum demand load current

Standard IEC 1000-3-2 sets limits on the harmonic content of the current but does not specifically regulate the purity factor  $K_p$  or the total harmonic distortion of the line current  $THD_i$ . The values of  $K_p$  and  $THD_i$  for which compliance with IEC 1000-3-2 is achieved depend on the power level. For low power level, even a relatively distorted line current may comply with the

standard. In addition to this, it can be seen that the distortion factor  $K_p$  of a waveform with a moderate  $THD_i$  is close to unity (e.g.  $K_p=0.989$  for  $THD_i=15\%$ ). The following statements can be made regarding power factor:

1. A high power factor can be achieved even with a substantial harmonic content. The power factor  $PF$  is not significantly degraded by harmonics, unless their amplitude is quite large (low  $K_p$ , very large  $THD_i$ ).
2. Low harmonic content does not guarantee high power factor ( $K_p$  close to unity, but low  $\cos\Phi$ ).
3. As  $PF$  and  $THD$  are related to distortion and displacement factors, hence improvement in power factor i.e. power factor correction (PFC) also implies harmonic reduction

## CHAPTER 2:POWER FACTOR CORRECTION

### 2.1:SOURCES OF POOR PF

>> Poor power factor caused by reactive linear circuit elements results as the current either leads or lags the voltage, depending on whether the load looks capacitive or inductive.

>> Less than acceptable power factor typically associated with electronic power conversion equipment is caused by nonlinear circuit elements.

In most off-line power supplies, the AC-DC front end consists of a bridge rectifier followed by a large filter capacitor.

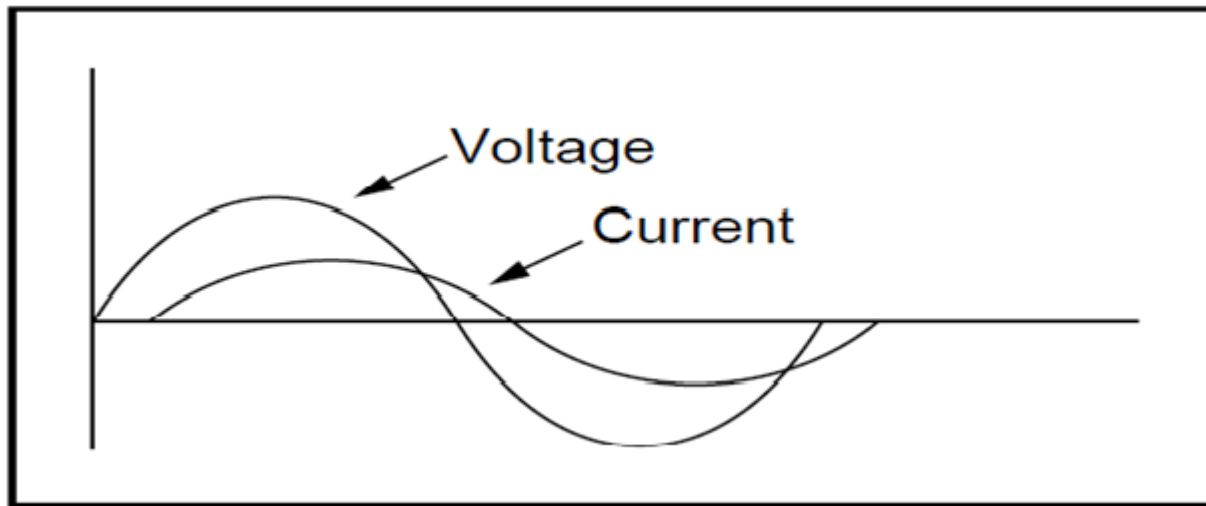


FIGURE 2.1(a): Traditional poor power factor—the current either leads or lags the voltage[1]

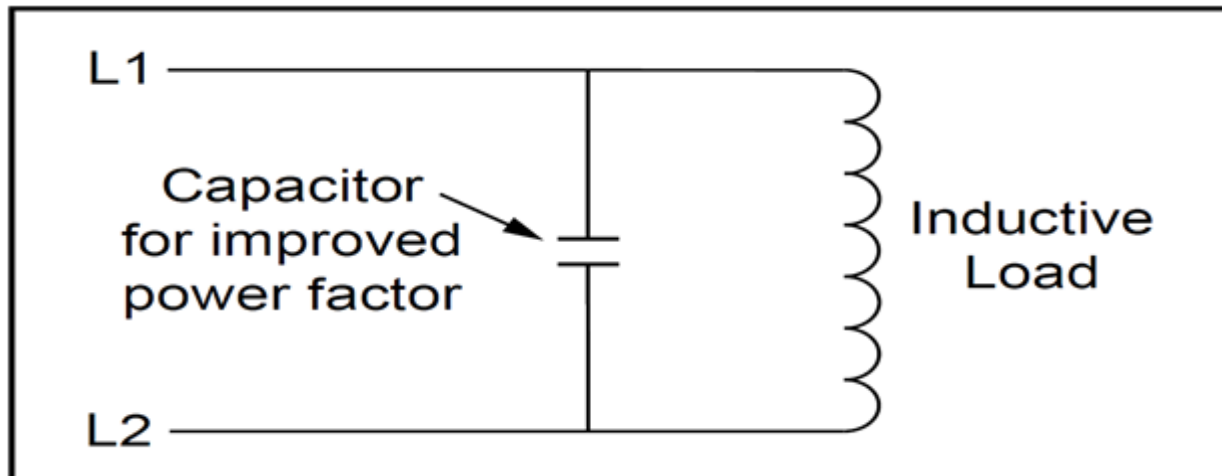


FIG 2.1(b) : Improvement of power factor[1]

In this circuit, current is drawn from the line only when the peak voltage on the line exceeds the voltage on the filter capacitor. Since the rate of rise and fall of current is greater than that of line voltage, and the current flows discontinuously, a series of predominantly odd harmonics are generated.

It is these harmonics that cause problems with the power distribution system. The power factor of the system can be improved slightly by either adding series inductance with the line or decreasing the value of the holdup capacitor, which will lengthen the conduction angle. However, both these methods severely limit the amount of power that can be drawn from the line.

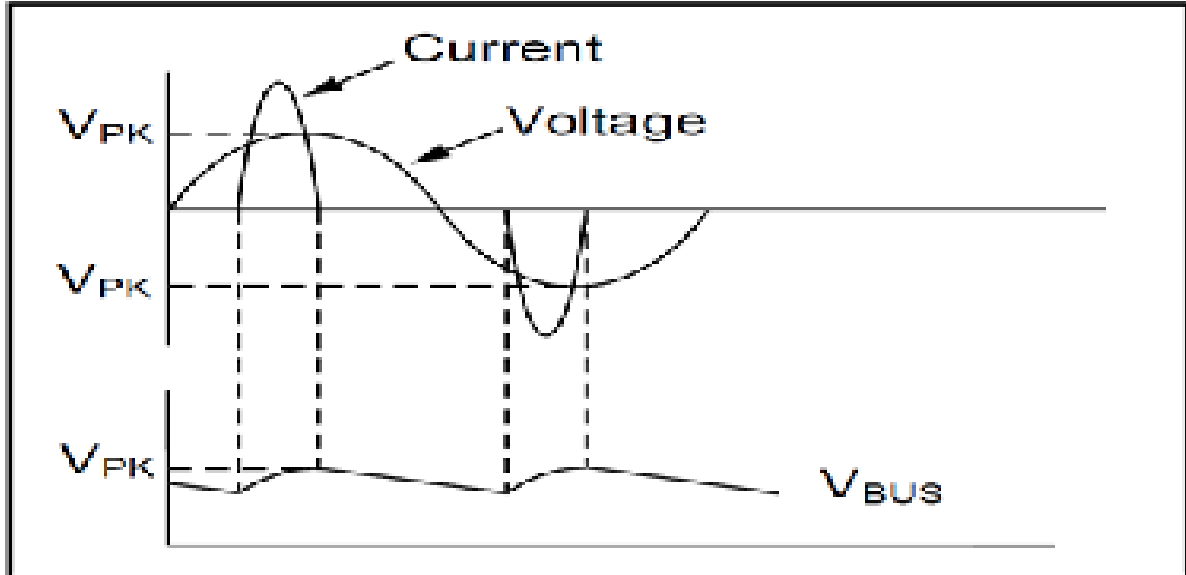


FIGURE 2.2(a): Current drawn from the line only when line voltage exceeds the voltage across the capacitor[1]

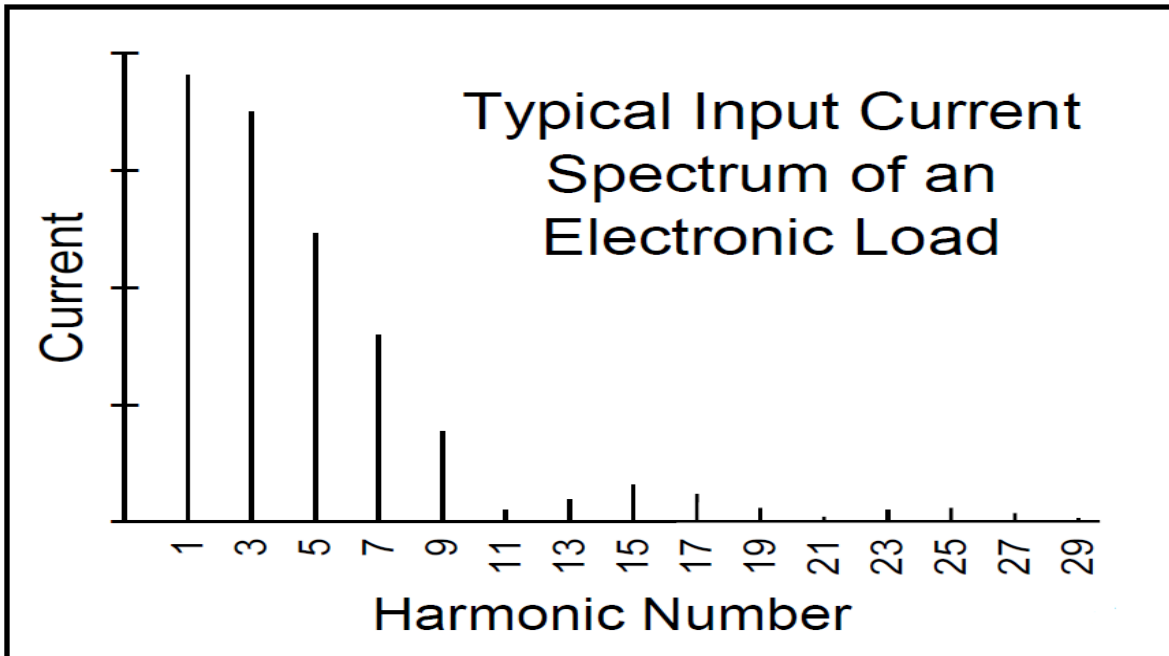


FIGURE 2.2(b): Front end of an AC-DC converter[1]



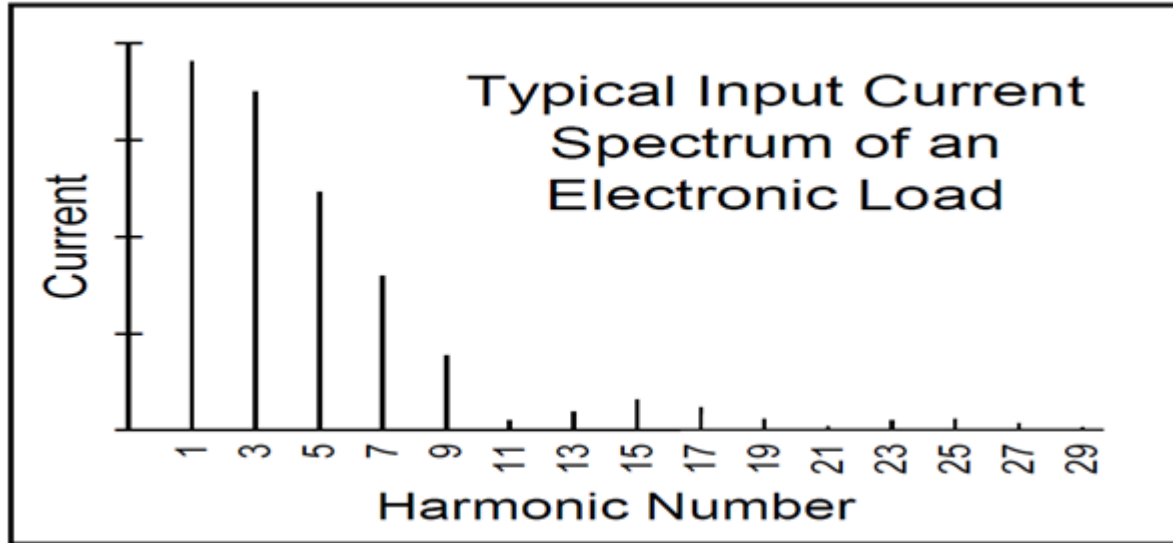


FIGURE 2.2(c): The poor power factor occurring in electronic loads generates odd harmonics[1]

## **2.2:Energy Balance in PFC circuits**

Let  $v_1(t)$  and  $i_1(t)$  be the line voltage and line current respectively. For an ideal PFC unit (PF=1),

we assume

$$v_1(t) = V_{1m} \sin \omega_1 t$$

$$i_1(t) = I_{1m} \sin \omega_1 t$$

where  $V_{1m}$  and  $I_{1m}$  are the amplitudes of line voltage and line current respectively. The instantaneous input power contains the real power (average power) component and an alternative component with frequency  $2\omega_1$ . The working principle of a PFC circuit is to process the input power in such a way that it stores the excessive input energy when instantaneous power  $P_{in}$  is greater than the power demanded  $P_o$ . The excessive input energy,  $w_{ex}(t)$  is given by

$$w_{ex}(t) = P_o / 2\omega_1 (1 - \sin 2\omega_1 t)$$

The excessive input energy is stored in the dynamic components (inductor and capacitor) of the PFC circuit.[2]

## **2.3 TYPES OF POWER FACTOR CORRECTORS**

### **2.3.1 PASSIVE PFC**

Harmonic current can be controlled in the simplest way by using a filter that passes current only at line frequency (50 or 60 Hz). Harmonic currents are suppressed and the non-linear device looks like a linear load. Power factor can be improved by using capacitors and inductors i.e. passive devices. Such filters with passive devices are called passive filters.

Disadvantage : They require large value high current inductors which are expensive and bulky.

A passive PFC circuit requires only a few components to increase efficiency, but they are large due to operating at the line power frequency

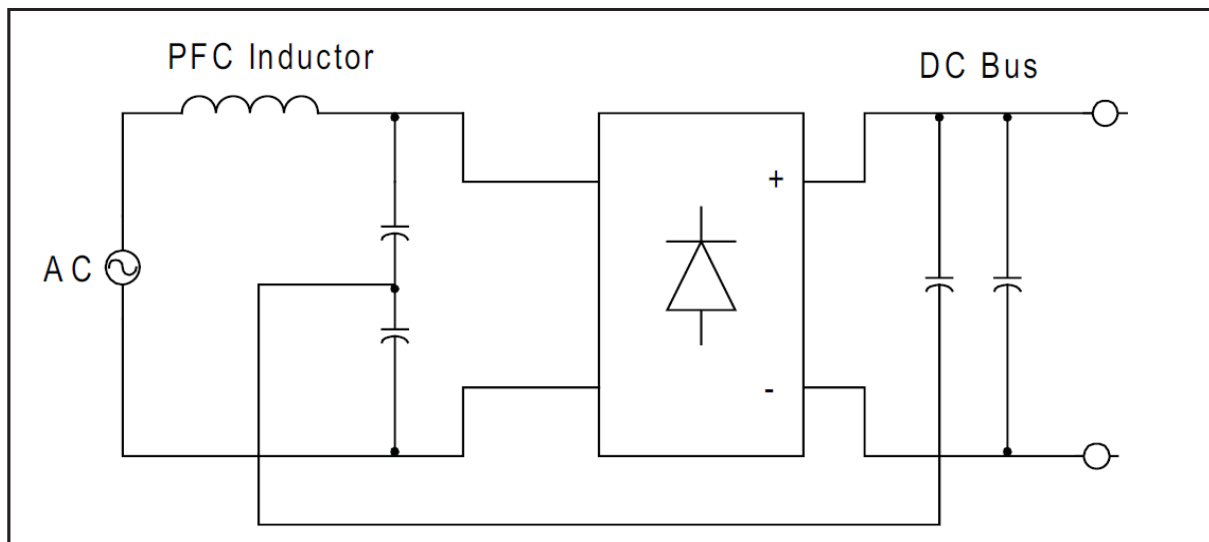


FIGURE 2.3 : A passive PFC circuit[2]

### **2.3.2 ACTIVE PFC**

An active approach is the most effective way to correct power factor of electronic supplies. Here, we place a boost converter between the bridge rectifier and the main input capacitors. The converter tries to maintain a constant DC output bus voltage and draws a current that is in phase with and at the same frequency as the line voltage.

#### **WORKING PRINCIPLE:**

The incoming line voltage passes through a bridge rectifier that produces a full wave rectified output. No current flows into the holdup capacitor unless the line voltage is boosted above the voltage present in the holdup capacitor. This allows the control circuit to adjust the boost voltage to maintain a sinusoidal input current. The control circuit uses the input voltage waveform as a template, to maintain a sinusoidal input current.

Hence,

>>The control circuit:

- 1) measures the input current, compares it to the input voltage waveform, and adjusts the boost voltage to produce an input current waveform of the same shape (2.4a-I).
- 2) It monitors the bus voltage and adjusts the boost voltage to maintain a coarsely regulated DC output (2.4a-B). [1]

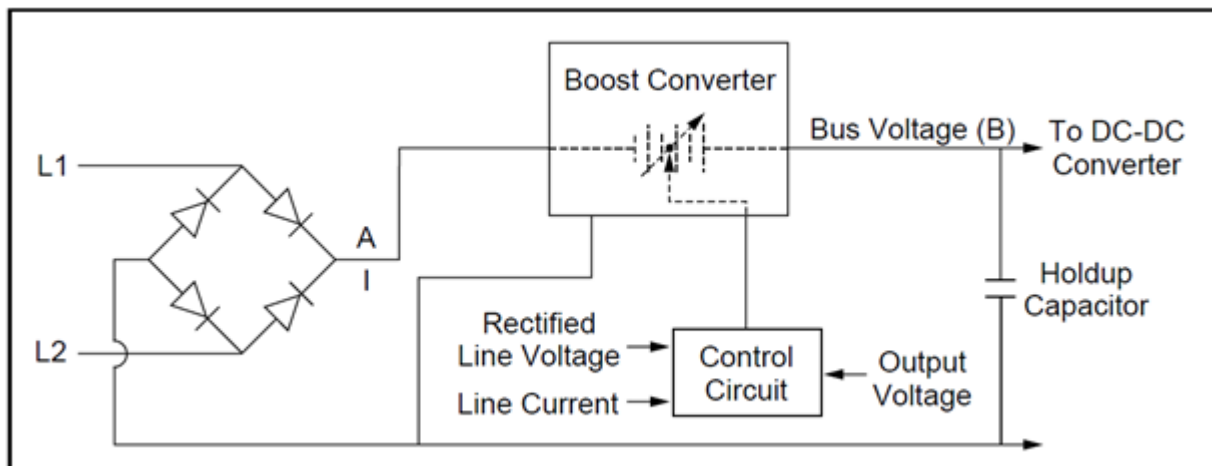
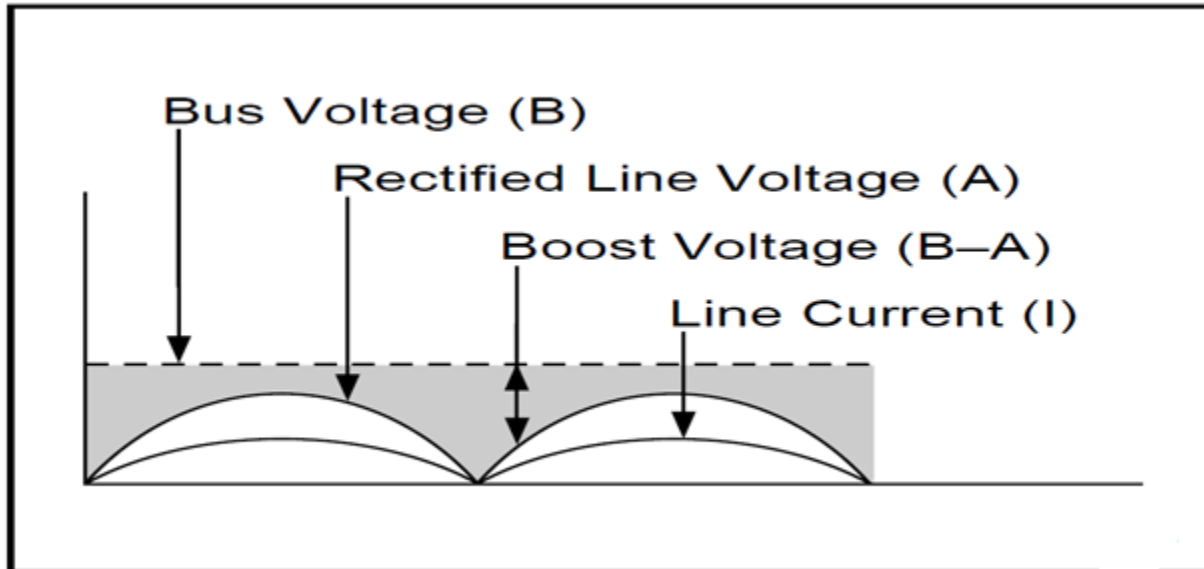


FIGURE 2.4(a & b) : Correcting the poor power factor associated with electronic power supplies requires an active approach in which a control circuit adjusts a boost voltage to maintain a sinusoidal input current[1]

### **USAGE:**

It is frequently used in practice. Due to their very wide input voltage range, many power supplies with active PFC can automatically adjust to operate on AC power from about 100 V (Japan) to 240 V (UK). That feature is particularly welcome in power supplies for laptops and cell phones.

### **ACTIVE PFC FUNCTIONS:**

- Active wave shaping of the input current
- Filtering of the high frequency switching
- Feedback sensing of the source current for waveform control
- Feedback control to regulate output voltage

### **DISADVANTAGES:**

1)The use of an active power factor correcting circuit results in few discontinuities in the input current and consequently low distortion and harmonic content of the input current being drawn from the line.

## **CHAPTER 3:ROLE OF DC-DC CONVERTERS**

Power electronic converters are essentially required when we need to convert electricity from one form to other. They form an interface between the source and load side.

In the last several years, the massive use of single phase power converters has increased the problems of power quality in electrical systems.

High-frequency active PFC circuit are preferred for power factor correction. Any DC-DC converters can be used for this purpose, if a suitable control method is used to shape its input current or if it has inherent PFC properties.

The DC-DC converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle.

In CICM, different control techniques are used to control the inductor current. Some of them are (1) peak current control (2) average current control (3) Hysteresis control (4) borderline control. The average mode control technique is specifically developed for PFC boost converters and is analyzed here.

### 3.1 BASIC CIRCUIT TOPOLOGIES OF ACTIVE POWER FACTOR CORRECTORS

Many circuits and control methods using switched-mode topologies have been developed to comply with standard. The active PFC's employ six basic converter topologies

- 1) Buck Corrector
- 2) Boost Corrector
- 3) Buck-Boost corrector
- 4) Cuk, Sepic and Zeta Correctors

We go for boost rectifiers which is one of the most important high power factor rectifiers from a theoretical and conceptual point of view. It is obtained from a classical non-controlled bridge rectifier, with the addition of transistor, diode and inductor.[2]

### 3.2 WORKING PRINCIPLE OF A BOOST CONVERTER

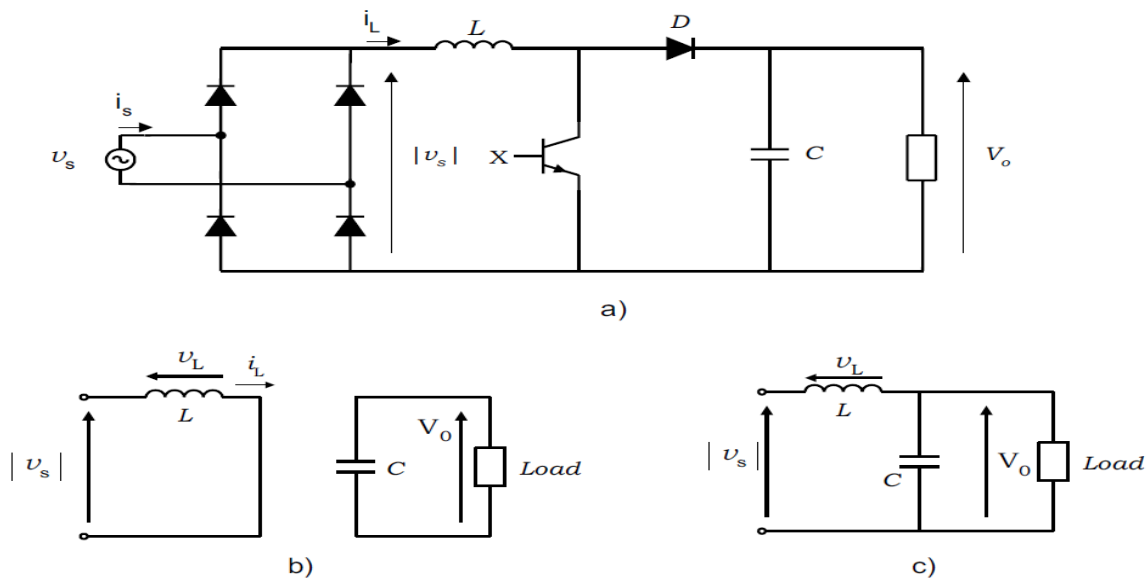


FIGURE 3.1:Figure representing the on and off states of a boost rectifier[2]

The input current  $i_s(t)$  is controlled by changing the conduction state of transistor. By switching the transistor with appropriate firing pulse sequence, the waveform of the input current can be controlled to follow a sinusoidal reference, as can be observed in the positive half wave in Fig.3.2(a,b). This figure shows the reference inductor current  $i_{Lref}$ , the inductor current  $i_L$ , and the gate drive signal  $x$  for transistor. Transistor is ON when  $x = 1$  and it is OFF when  $x = 0$ . The ON and OFF state of the transistor produces an increase and decrease in the inductor current  $i_L$ .

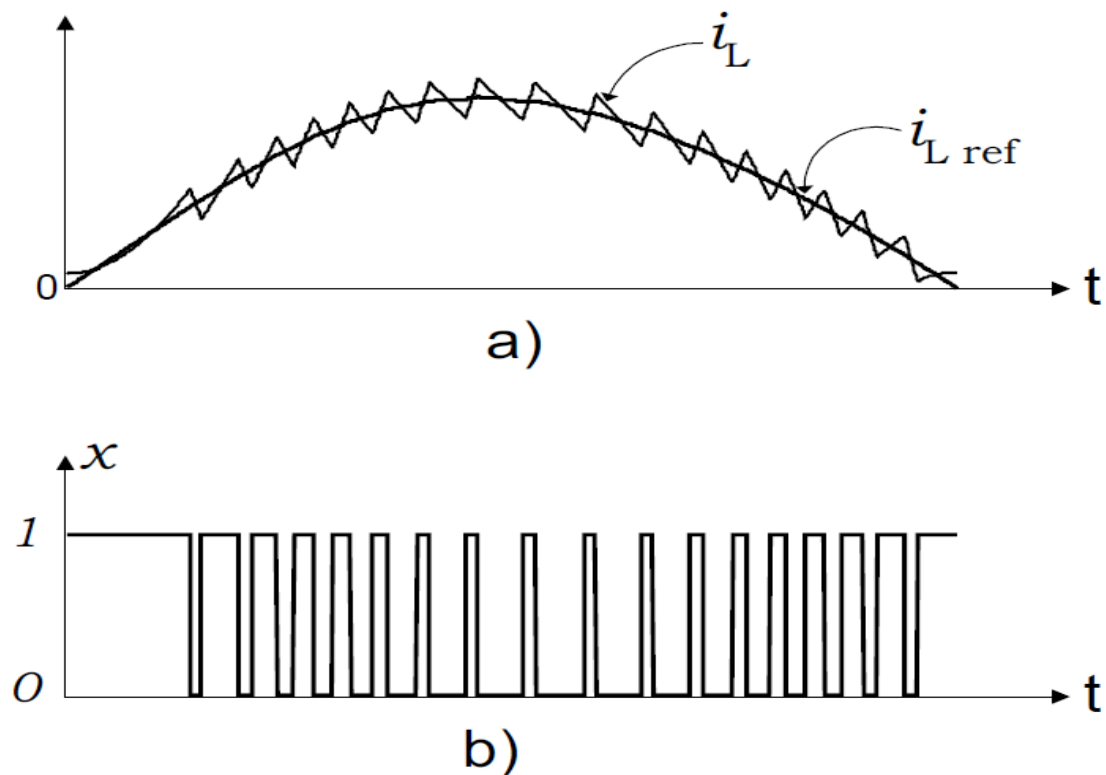


FIGURE 3.2:Behavior of inductor current[2]

(a) Waveforms

(b) Transistor T gate drive signal  $x$



The PFC properties of a boost converter can be estimated from the given plots:

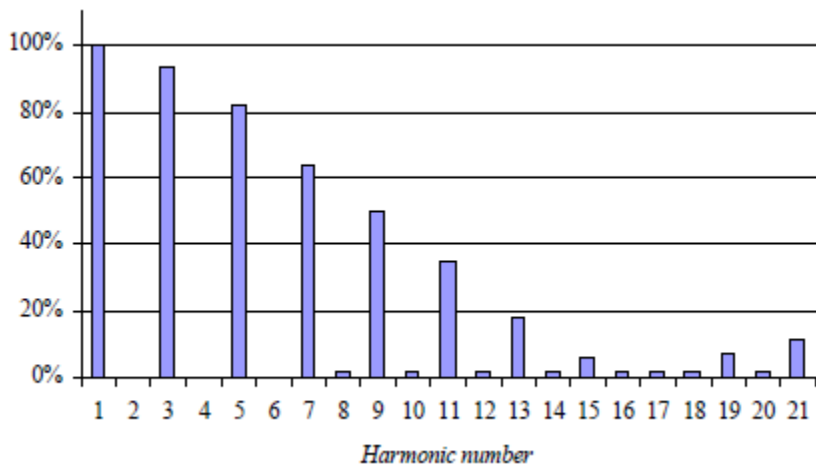


FIGURE 3.3: Harmonic content of the current waveform obtained from a rectifier circuit[3]

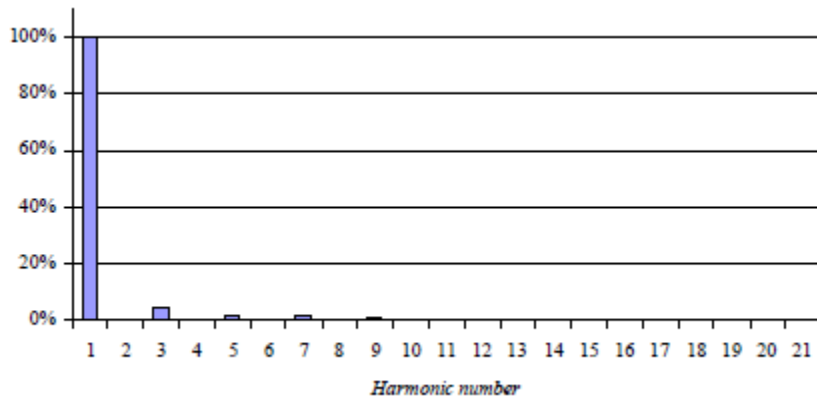


FIGURE 3.4: Harmonic content of the current waveform of a boost PFC converter[3]

As can be clearly seen, the higher order harmonics are considerably reduced in the line current by using a boost converter.

### **3.3: SYSTEM CONFIGURATIONS FOR PFC POWER SUPPLY**

The most common configuration of ac-dc power supply with PFC are **two-stage scheme** and **one-stage scheme**.

#### **Two stage scheme:**

>>In two stage scheme, a non-isolated PFC ac-dc converter is connected to the line to create an intermediate dc bus. This dc bus voltage is usually full of second harmonic ripple. Therefore followed by the ac-dc converter, a dc-dc converter is cascaded to provide electrical isolation and tight voltage regulation.

>> The advantage of two stage structures of PFC circuits is that the two power stages can be controlled separately, and thus it makes it possible to have both converters optimized.

>> The drawbacks of this scheme are lower efficiency due to twice processing of the input power, complex control circuits, higher cost and low reliability.

#### **One stage scheme:**

>>One stage scheme combines the PFC circuit and power conversion circuit in one stage.

>>Due to its simplified structure, it is more efficient in low to medium power applications.

>>However, it has a very slow dynamic response.

### **The parallel pfc scheme:**

>>To avoid twice power process in two-stage scheme, two converters can be connected in parallel to form the parallel PFC scheme.

>>Here, power from the ac main to the load flows through two parallel paths. The main path is a rectifier, in which power is not processed twice for PFC, whereas the other path processes the input power twice for PFC purpose. To achieve both unity power factor and tight output voltage regulation, only the difference between the input power and output power needs to be processed twice. Therefore, high efficiency can be obtained by this method.[2]

## CHAPTER 4: DUAL BOOST CONVERTERS

Conventionally, boost converters are used as active Power factor correctors. However, a recent novel approach for PFC is to use dual boost converter i.e. two boost converters connected in parallel. Circuit diagrams for both types of PFCs are as given below:

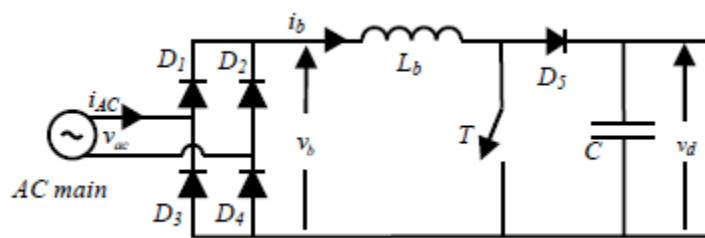


FIGURE 4.1: Classical PFC circuit[8]

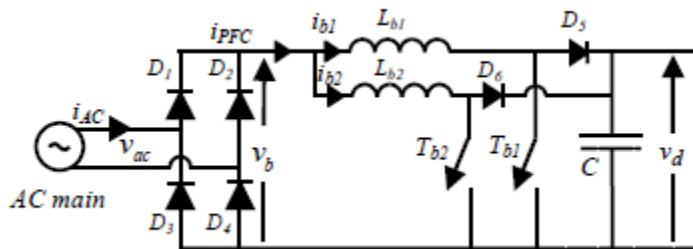


FIGURE 4.2: Dual Boost PFC circuit[8]

Here, we use a parallel scheme, where choke  $L_{b1}$  and switch  $T_{b1}$  are for main PFC while  $L_{b2}$  and  $T_{b2}$  are for active filtering. The filtering circuit serves two purposes i.e. improves the quality of

line current and reduces the PFC total switching loss. The reduction in switching losses occurs due to different values of switching frequency and current amplitude for the two switches.

The parallel connection of switch mode converter is a well known strategy. It involves phase shifting of two or more boost converters connected in parallel and operating at the same switching frequency.[8]

**Advantages of this approach include:**

- 1) Overall high efficiency.
- 2) Reduction of the development cost due to the modular design.
- 3) High reliability.
- 4) Reduction in the current ripple
- 5) Reduction of conduction losses
- 6) size reduction of active and passive components as boost choke

**4.1: DUAL PFC MODELING**

With reference to Fig.4.2 considering working in the continuous conduction mode, we obtain the following voltage equations:

$$\begin{cases} v_b = L_{b1} \frac{d}{dt} i_{b1} + R_{b1} i_{b1} + f_{b1} v_d \\ v_b = L_{b2} \frac{d}{dt} i_{b2} + R_{b2} i_{b2} + f_{b2} v_d \\ i_{PFC} = i_{b1} + i_{b2} \end{cases}$$

where:

$$v_b(t) = |v_b(t) \sin(\omega t)|$$

$$f_{b1} = \begin{cases} 0 & \text{if } T_{b1}=1 \text{ (switch on)} \\ 1 & \text{if } T_{b1}=0 \text{ (switch off)} \end{cases}$$

$$f_{b2} = \begin{cases} 0 & \text{if } T_{b2}=1 \text{ (switch on)} \\ 1 & \text{if } T_{b2}=0 \text{ (switch off)} \end{cases}$$

The above set of equations can also be written as:

$$f_{b1} = 0 \rightarrow \frac{di_{b1}(t)}{dt} = \frac{v_b(t)}{L_{b1}}$$

$$f_{b1} = 1 \rightarrow \frac{di_{b1}(t)}{dt} = \frac{v_b(t) - v_d(t)}{L_{b1}}$$

$$f_{b2} = 0 \rightarrow \frac{di_{b2}(t)}{dt} = \frac{v_b(t)}{L_{b2}}$$

$$f_{b2} = 1 \rightarrow \frac{di_{b2}(t)}{dt} = \frac{v_b(t) - v_d(t)}{L_{b2}}$$

where:

$$i_{b1} \geq 0 \quad i_{b2} \geq 0$$

[8]

## **4.2: DUAL PFC CONTROLLING**

PFC currents  $i_{b1}$  and  $i_{b2}$  can be achieved if the following condition occurs:

$$V_d(t) > v_b(t)$$

If the above condition is satisfied, it is possible to control the derivative of the total PFC current

iPFC[8]

$$\frac{di_{PFC}}{dt} = \frac{di_{b1}}{dt} + \frac{di_{b2}}{dt}$$

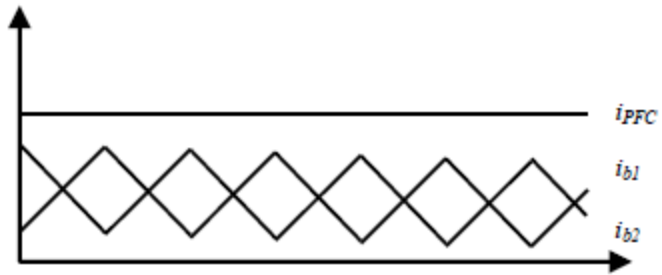


FIGURE 4.3: Input current of two interleaved PFC in ideal working condition[8]

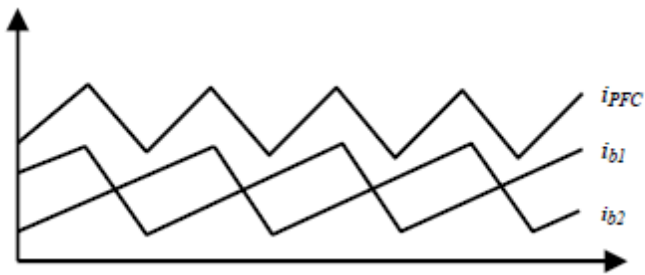


FIGURE 4.4: Input currents of two interleaved PFC under actual working condition[8]



## CHAPTER 5: CONTROL PRINCIPLES OF DC-DC CONVERTERS

Control strategy for an electrical system is intended to develop a set of actions that can detect the time evolution of electrical quantities and to impose them to follow a desired time evolution. In general, a control algorithm can be split into three functional sub-blocks:

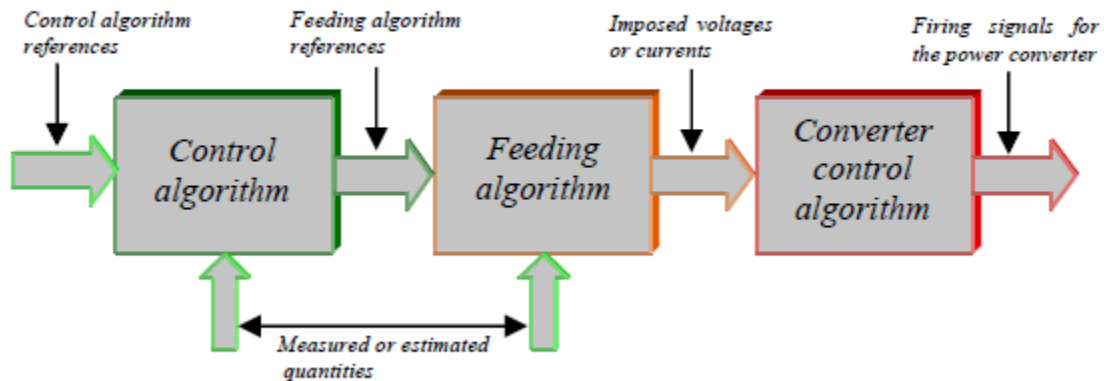


FIGURE 5.1: Basic description and splitting of the Control algorithm[8]

- 1) Control Algorithm-Operates to generate reference values to the feeding algorithm on the basis of reference values imposed to the controller.
- 2) Feeding Algorithm- gives the voltage or current values to impose at the considered system in order to follow the time evolution of the reference values coming from the control algorithm

- 3) Converter control Algorithm-provides the right sequence of firing pulses for management of the power modules based on the information derived from control and feeding algorithm.

A dc-dc converter provides a regulated dc output voltage under varying load and input voltage conditions. The converter component values are also changing with time, temperature and pressure. Hence, the control of the output voltage should be performed in a closed-loop manner using principles of negative feedback. The two most common closed-loop control methods for PWM dc-dc converters, namely the voltage-mode control and the current-mode control, are presented schematically in figures 5.2 and 5.3.

### **5.1: VOLTAGE MODE CONTROL**

The voltage-mode control scheme shown in Fig. 5.2. Here the converter output voltage that is to be regulated is sensed and fed back through a resistive voltage divider. It is then compared with a precision external reference voltage,  $V_{ref}$  in a **voltage error amplifier**. The error amplifier produces a control voltage that is compared to a constant-amplitude **sawtooth waveform**. The **comparator or the PWM Modulator** produces a **PWM signal** that is fed to drivers of controllable switches in the dc-dc converter. The duty ratio of the PWM signal depends on the value of the control voltage. The frequency of the PWM signal is the same as the frequency of the sawtooth waveform.[2]

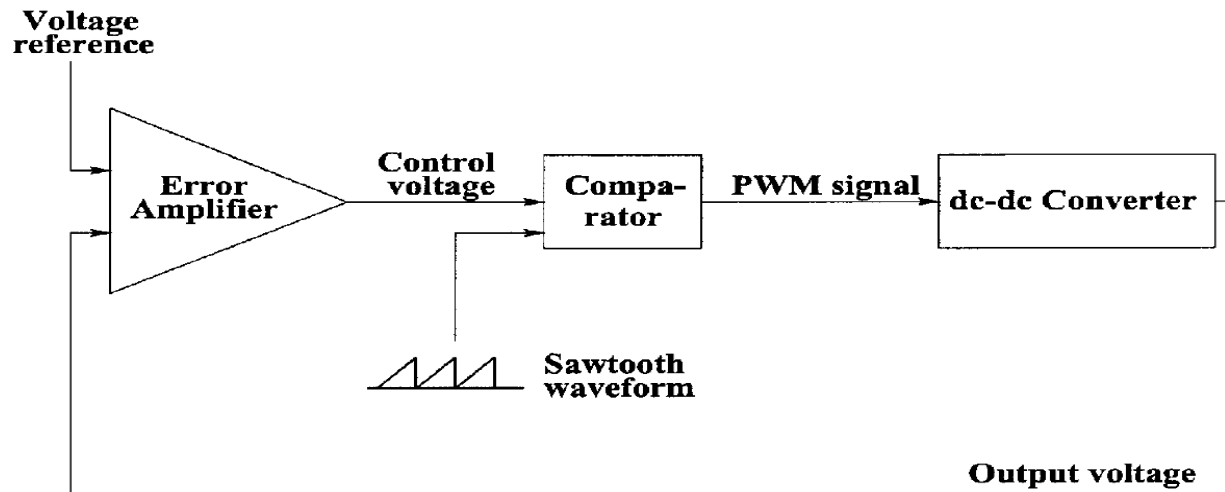


FIGURE 5.2 : Schematic diagram for voltage mode control[2]

### **ADVANTAGES:**

- 1) The simple hardware implementation and flexibility is the greatest advantage of voltage mode control scheme.
- 2) The error amplifier keeps a fast track of changes in the converter output voltage. Thus, it provides good load regulation, that is, regulation against variations in the load.

### **DISADVANTAGES:**

- 1) This scheme has a poor line regulation i.e. regulation against variations in the input voltage. It is delayed since any change in the input voltage must manifest itself in the converter output before it can be corrected.

To alleviate this problem, the voltage-mode control scheme is sometimes augmented by a so-called voltage-feedforward path. The feedforward path affects directly the PWM duty ratio according to variations in the input voltage.

## **5.2: CURRENT MODE CONTROL**

Signals in current form have a natural advantage over voltage signals. Voltage being an accumulation of electron flux, is slow in time as far as control mechanism is concerned. This led to the development of a new area in switch mode power supply design, i.e. the current mode control. Here, the averaged or peak current of magnetic origin is employed in the feedback loop of the switch mode power converters. It has given new avenues of analysis and at same time introduced complexities in terms of multiple loops.

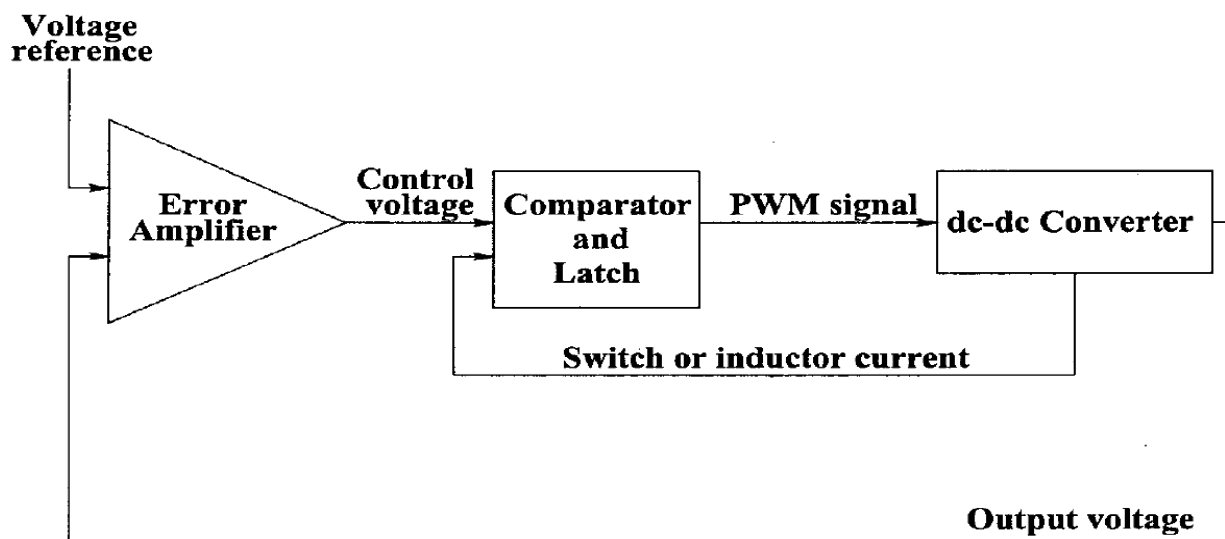


FIGURE 5.3: Schematic diagram for current mode control[2]

A schematic diagram of current mode control is shown in Fig.5.3. It comprises of an additional inner control loop. The inductor current signal, converted to its voltage analog fed back by this loop is compared to the control voltage. The dynamic behavior of the converter is significantly altered by this modification of replacing the sawtooth waveform by the converter current signal.

The key difference between voltage and current mode control is the way the reference map is generated.

In the case of voltage mode control, the ramp is external from the viewpoint of the power plant, whereas for current mode control, it is internal.

### **WORKING PRINCIPLE:**

This scheme controls both the input current and the output voltage. The control strategy is designed such that the input current follows the sinusoidal line voltage i.e. input to the converter appears resistive. An analog multiplier generates the current programming signal by multiplying the rectified line voltage with the output of the voltage error amplifier. This modulation makes the current programming signal follow the shape of input voltage. The current programming signal acts as a reference current. It is compared with the switch current in a PWM comparator. The resulting pulses drive a MOSFET. Thus output voltage is controlled by changing the average value of current programming signal.

When a current mode control technique is implemented practically, it is feasible to sense the peak inductor current instead of the average value. As the peak inductor current is equal to the peak switch current, the latter can be used in the inner loop, which often simplifies the current

sensor. As the peak inductor (switch) current is proportional to the input voltage. Hence, the inner loop of the current-mode control naturally accomplishes the input voltage-feedforward technique .

### **ADVANTAGES:**

The performance merits of current mode control over voltage mode control can be appreciated more by looking at the transient response when the converter is subjected to a step load disturbance or a step line change. When subjected to a volt-second(flux) drive, the magnetic device develops a current. The time rate of such a current is easily expressed as:

$$di/dt \text{ proportional to } (\text{voltage across})/\text{inductance}=(V_{\text{input}}-V_o)/L$$

The equation tells us that the magnetic device's current rate of change is in phase with either the input or the output, voltage changes that, in turn, are reflected in error voltage. Hence, the average value of the magnetic device's current rapidly tracks the step load and minimizes the error voltage. In other words, the phase delay property of a magnetic device is removed. In terms of control system theory, a lagging pole is eliminated and system response speed is improved. This is the key merit of current-mode control.

### 5.3: IMPLEMENTATION OF THE INNER LOOP FOR CURRENT MODE CONTROL

There are several ways to implement the high bandwidth inner loop in the current mode control technique. These are:

1. Peak current control
2. Average current control
3. Hysteresis control
4. Borderline control

#### 5.3.1: PEAK CURRENT CONTROL

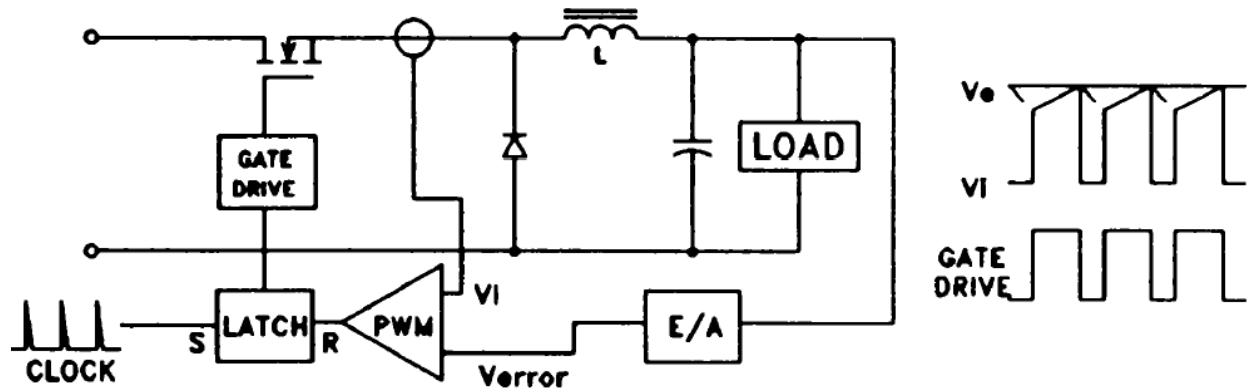


FIGURE 5.4: Peak current mode control circuit and its waveforms[2]

The objective of the inner loop is to control the state-space averaged inductor current, but in practice the instantaneous peak inductor current is the basis for control. The switch current during the ON time is equal to the inductor current. If the inductor ripple current is small, peak

current control is nearly equivalent to the average inductor current control. In a conventional switching power supply employing a buck derived topology, the inductor current is in the output. Current mode control is then the output current control. On the other hand, in a high power factor preregulator using the boost topology, the inductor is in the input. Current mode control then controls the input current, allowing it to be easily conformed to the desired sinusoidal waveshape.

The peak method of inductor current control functions by comparing the upslope of inductor current (or switch current) to a current program level set by the outer loop. The comparator turns the power switch off when the instantaneous current reaches the desired level.

### **5.3.2 PRACTICAL PROBLEMS IN PEAK CURRENT MODE CONTROL:**

#### **1. POOR NOISE IMMUNITY:**

The current ramp is usually quite small compared to the programming level, especially when  $V_{IN}$  is low. As a result, this method is extremely susceptible to noise. Whenever the switch turns on, a noise spike is generated. Even a fraction of a volt if coupled into the control circuit can cause it to turn off immediately, resulting in a subharmonic operating mode with much greater ripple. Circuit layout and bypassing are critically important to successful operation.

#### **2. SLOPE COMPENSATION REQUIRED:**

The peak current control method is inherently unstable at duty ratios exceeding 0.5, resulting in sub-harmonic oscillation. A compensating ramp (with slope equal to the inductor current



downslope) needs to be applied to the comparator input to eliminate the instability. In a buck regulator, the inductor current downslope equals  $V_o/L$ . With  $V_o$  constant, the compensating ramp is fixed and easy to calculate. With a boost regulator in a high power factor application, the downslope of inductor current equals  $(V_{IN}-V_o)/L$  and thus varies considerably as the input voltage follows the rectified sine waveform. A fixed ramp providing adequate compensation will overcompensate much of the time, with resulting performance degradation and increased distortion.

### **3. PEAK TO AVERAGE CURRENT ERROR:**

In high power factor boost preregulators, the peak/avg error is a serious issue because it causes distortion of the input current waveform. While the peak current follows the desired sine wave current program, the average current does not. The peak/avg error becomes much worse at lower current levels, especially when the inductor current becomes discontinuous as the sine wave approaches zero every half cycle. To achieve low distortion, the peak/avg error must be small. This requires a large inductor to make the ripple current small. The resulting shallow inductor ramp makes the already poor noise immunity much worse.

### **4. TOPOLOGY PROBLEMS:**

Conventional peak current mode control actually controls inductor current. As normally used for output current control, it is more effective when applied to a buck regulator where the inductor is in the output. But for flyback or boost topologies the inductor is not in the output, the wrong current is controlled, and much of the advantage of current mode control is lost. Likewise, the

boost topology with its inductor at the input is well suited for input current control in a high power factor preregulator, but buck and flyback topologies are not suited because the inductor is not in the input and the wrong current is controlled.[4]

### **5.3.3: AVERAGE CURRENT MODE CONTROL**

Average current mode control(ACMC) is a two loop control method, inner loop being the current and the outer loop being the voltage loop for power electronic converters. This control method has many applications in the higher switching frequency, lower power segment upto 10kW, at higher switching frequency and above, but this too is subject to change.

It is frequently being used for the control of DC/DC converters and single phase Power factor correctors.

Average current mode control has the following advantages over peak current mode control:

- 1) An external compensation ramp is not required.
- 2) Increased DC closed loop gain at low frequencies.
- 3) Improved immunity to noise in the sensed current signal.
- 4) The increased current loop DC gain at low frequencies is especially useful for single phase PFC applications using boost derived topologies. This is because here it is desirable that the average rather than the peak of the inductor current follows sinusoidal reference.[2],[3]

**WORKING PRINCIPLE:**

A block diagram representation of average current mode control is given as below:

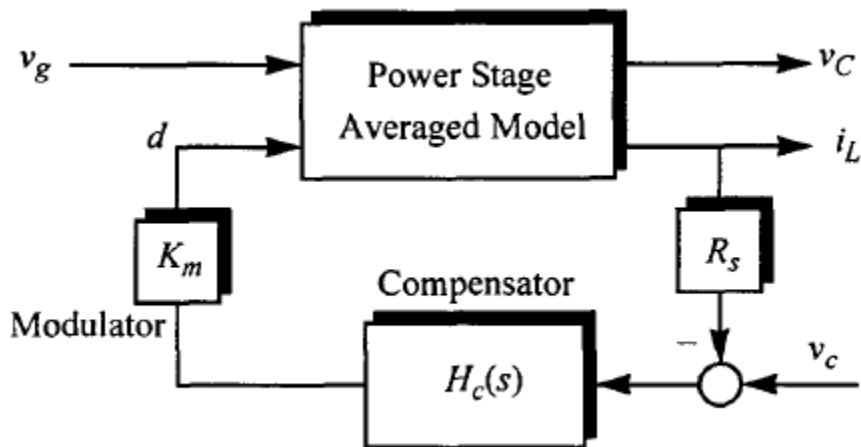


FIGURE 5.5: Block diagram representation of the averaged model[5]

The main functional block of the averaged model is the current compensator. Schematic diagram of the current compensator block is as given below:

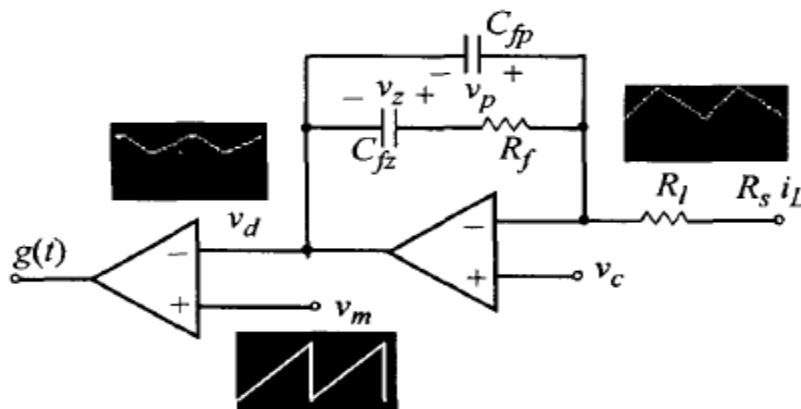


FIGURE 5.6: Current Compensator and PWM in average current control[5]

The control method works on the following principle: The inductor current of the converter  $i_L$  is sensed by a resistor  $R_s$  and compared with a control voltage  $v_c$  that represents the required average value of the inductor current. The difference is amplified by the compensator comprising of  $R_i, R_f, C_{fz}$  and  $C_{fp}$ . The output of the amplifier is compared to a triangular PWM signal  $v_m$  at the comparator inputs to generate switching control signals for the converter.

The transfer function of the compensator can be written as:

$$H_c(s) = \frac{K_c(1 + s/\omega_z)}{s(1 + s/\omega_p)}$$

where the DC gain,  $K_c$  the high frequency pole,  $\omega_p$  and the zero  $\omega_z$  are defined by:

$$K = \frac{1}{R_f(C_{fp} + C_{fz})}, \omega_z = \frac{1}{R_f C_{fz}}, \omega_p = \frac{C_{fz} + C_{fp}}{R_f C_{fz} C_{fp}}.$$

The Poles:

at origin is used to boost DC and low frequency gain of the current loop.

high frequency pole is added to filter the switching ripple of the sensed current signal and increase noise immunity.

The zero:

is needed for extending the current loop crossover frequency

The PWM converter can be modeled by a constant gain:

$$K_m = 1/V_m$$

where,  $V_m$  is the peak-to-peak voltage of the triangular carrier signal  $v_m$ . [5]

The transfer functions for the compensator and the PWM can be combined to form a complete model for the converter

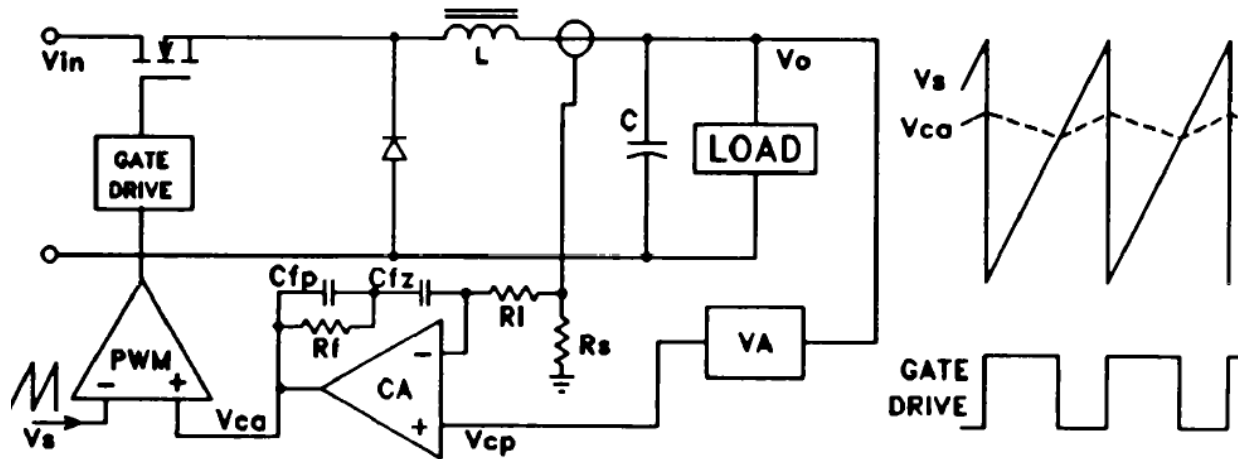


FIGURE 5.7: Average current mode control circuit and waveforms [2]

#### ADVANTAGES:

- 1) Average current tracks the current program with a high degree of accuracy. This is especially important in high power factor preregulators, enabling less harmonic distortion to be achieved with a relatively small inductor. In fact, average current mode control functions well even when the mode boundary is crossed into the discontinuous mode at low current levels. The outer voltage control loop is crossed into the discontinuous mode at low current levels. The outer voltage control loop is oblivious to this mode change.

- 2) Slope compensation is not required but there is a limit to loop gain at switching frequency in order to achieve stability.
- 3) Noise immunity is excellent. When the clock pulse turns the power switch on, the oscillator ramp immediately dives to its lowest level, volts away from corresponding current error level at the input of the PWM comparator.
- 4) The average current control mode method can be used to sense and control the current in any circuit branch. Thus it can control input current accurately with buck and flyback topologies.

#### **5.4: DESIGN OF THE CURRENT CONTROL LOOP[5],[7]**

Designing of the average current control loop is basically fixing the poles, zeroes and gain of the transfer functions defined above. This is done taking into account loop gain and switching instability.

The current compensator has three parameters: the DC gain  $K_c$ , the zero  $\omega_z$  and the high frequency pole  $\omega_p$ . The high frequency pole is placed near the switching frequency in order to provide sufficient filtering for switching frequency ripple. The zero  $\omega_z$  is placed before the resonant  $\omega_o$  of the power stage usually between one third and half of  $\omega_o$  to maximize the current loop crossover frequency.

As far as the design of  $K_c$  is concerned is obtained by setting the upslope of the current compensator output in the off-time interval of the switch equal to the slope of the ramp

signal  $v_m$ . The upslope of compensator output is obtained by multiplying the downslope of the voltage across current sensing resistor by the gain of the compensator at switching frequency, that is approximately  $R_f/R_i$

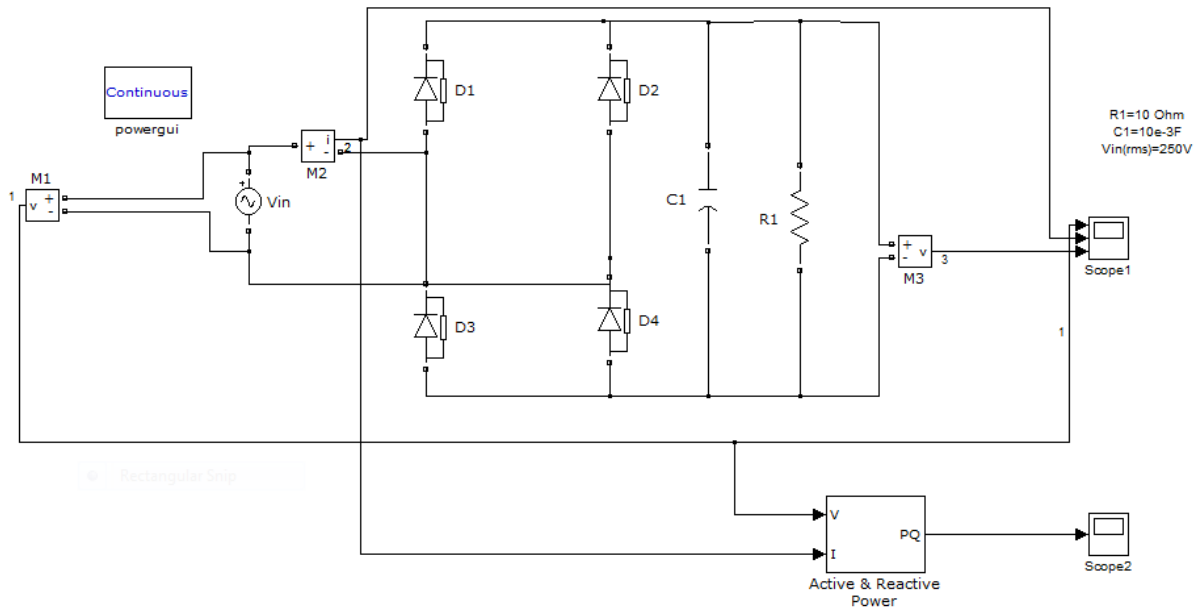
$$\frac{R_f}{R_i} \cdot \frac{R_s V_0}{L} \leq V_m f_s \quad \rightarrow \quad \frac{R_f}{R_i} \leq \frac{V_m f_s L}{V_0 R_s}$$

The compensator output may intersect the ramp signal again in the off-time period if the DC gain is higher than that defined by the above equation. This leads to switching instability.

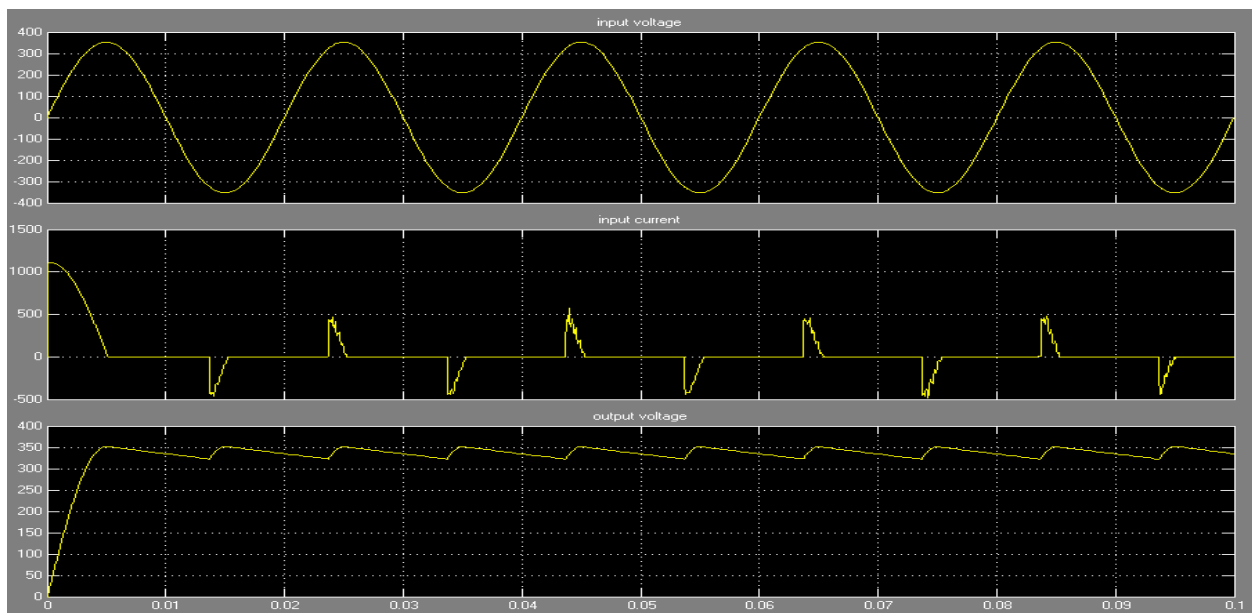
## CHAPTER 6: RESULTS AND CONCLUSION

### 1) MODEL AND SIMULATION RESULTS FOR A RECTIFIER CIRCUIT WITHOUT PFC CIRCUIT:

#### 1A) MODEL:

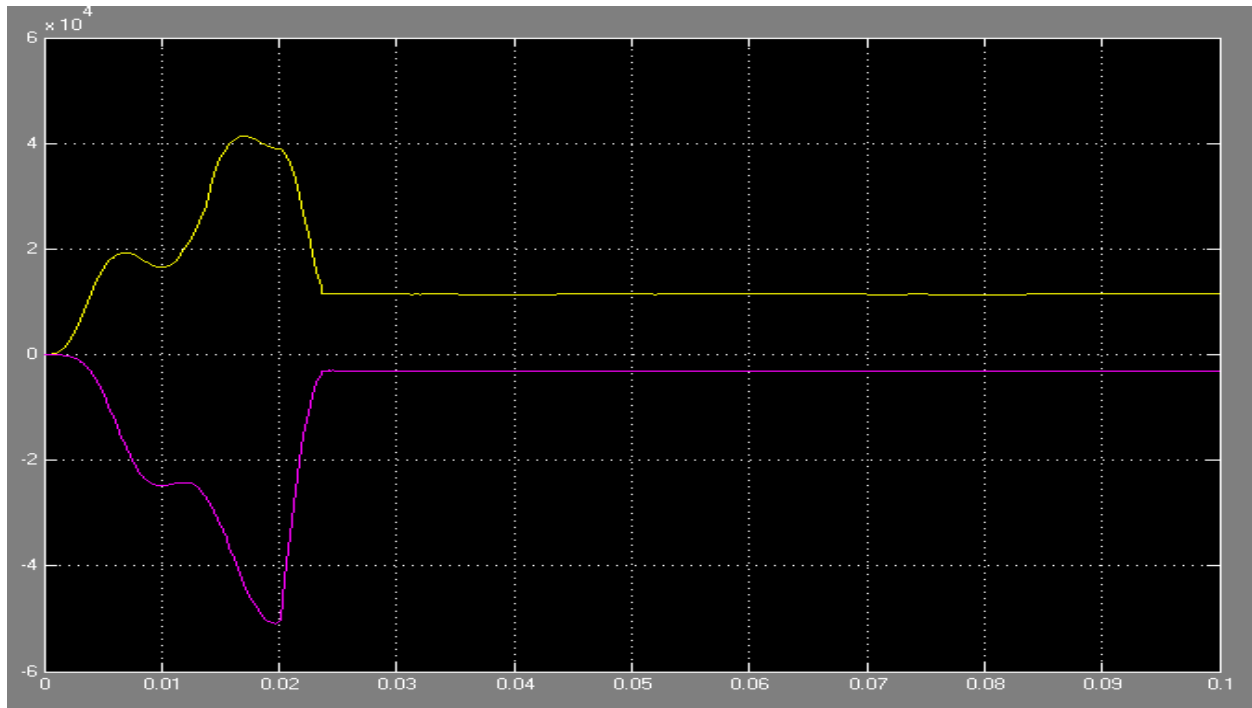


#### 1B) SIMULATION RESULT:

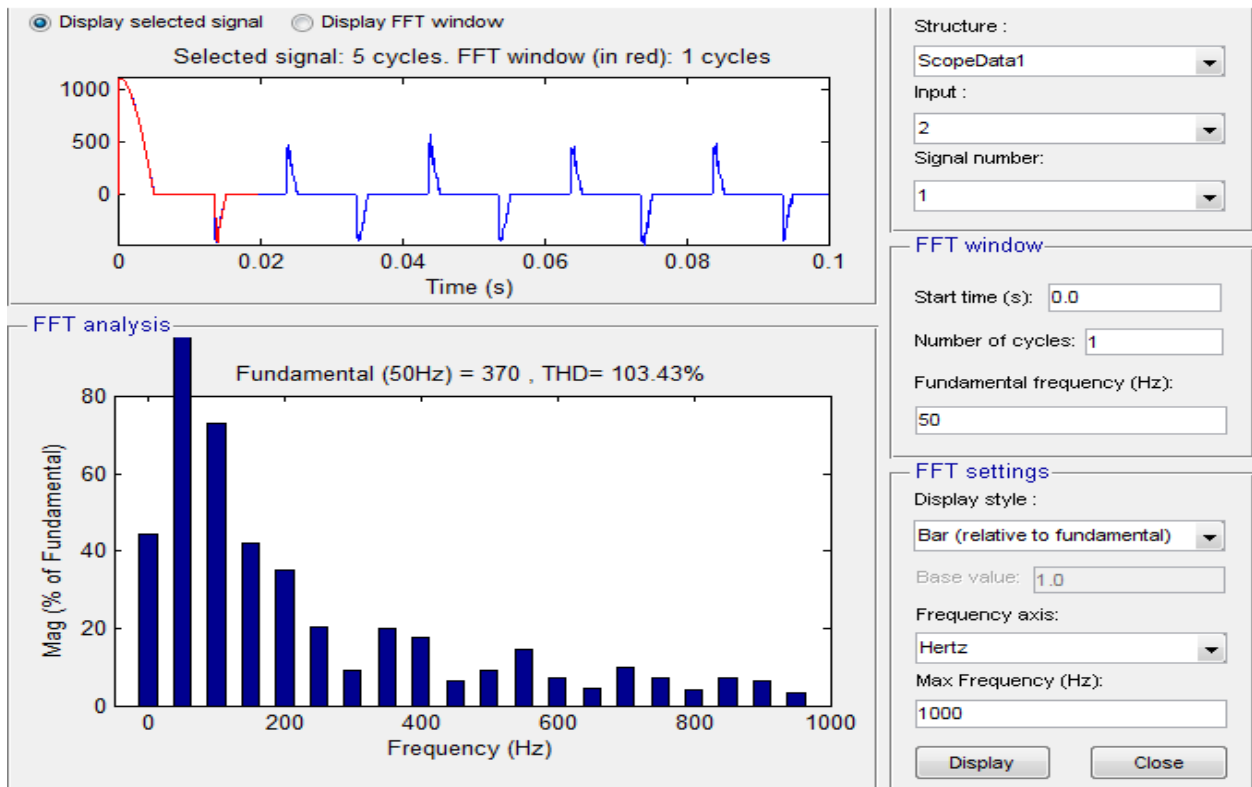




### 1C) ACTIVE AND REACTIVE POWER:



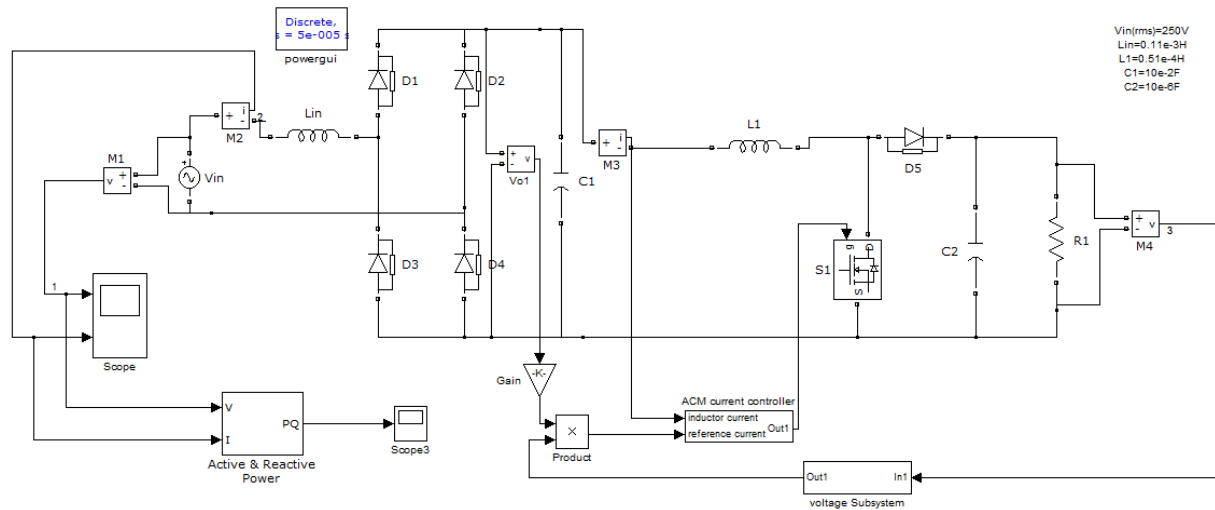
### 1D) FFT ANALYSIS OF INPUT CURRENT:



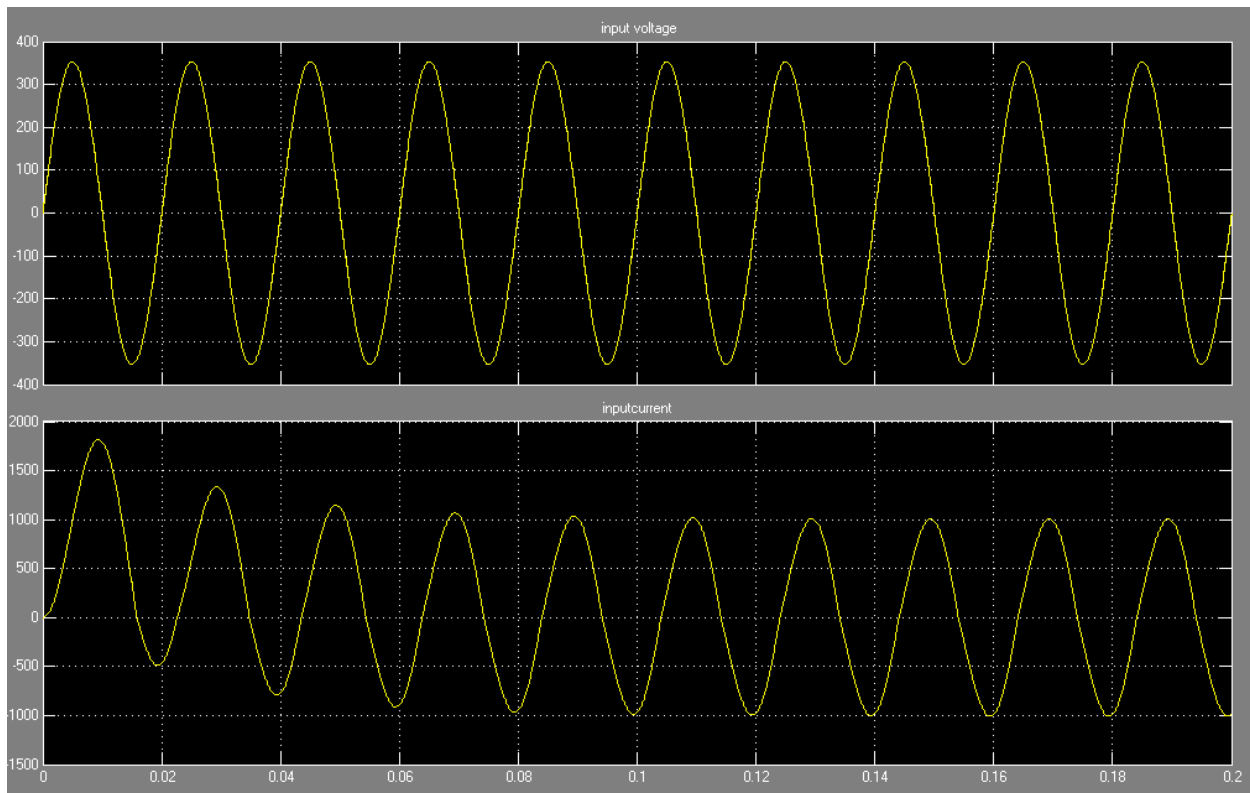
## 2) MODEL AND SIMULATION RESULTS FOR PFC CIRCUIT HAVING A BOOST CONVERTER:

### BOOST CONVERTER:

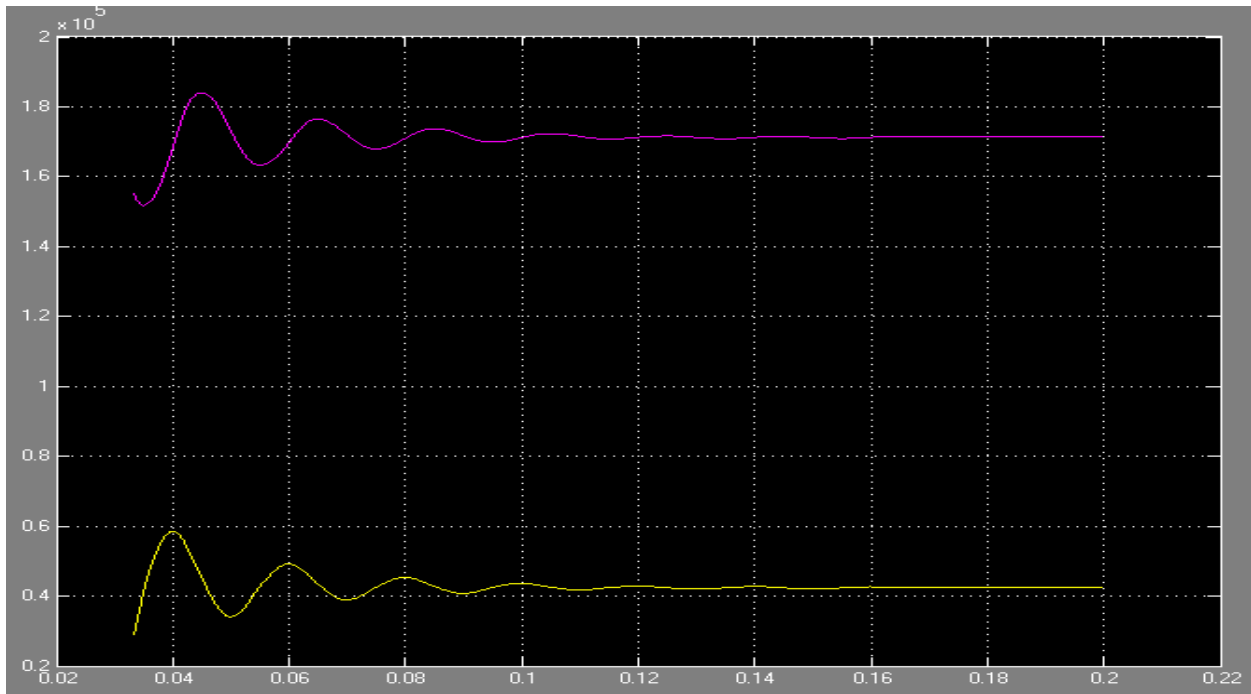
#### 2A) MODEL:



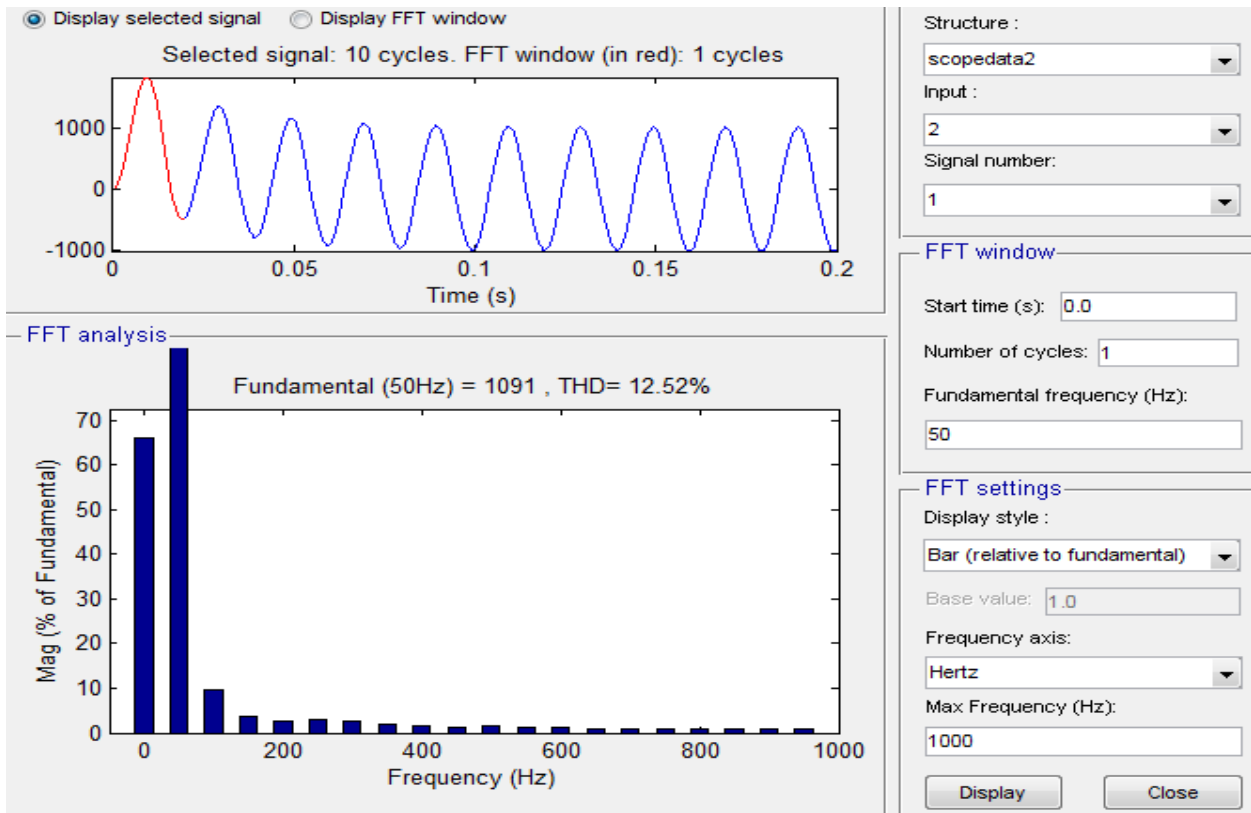
#### 2B) SIMULATION RESULT:



## 2C) ACTIVE AND REACTIVE POWER:

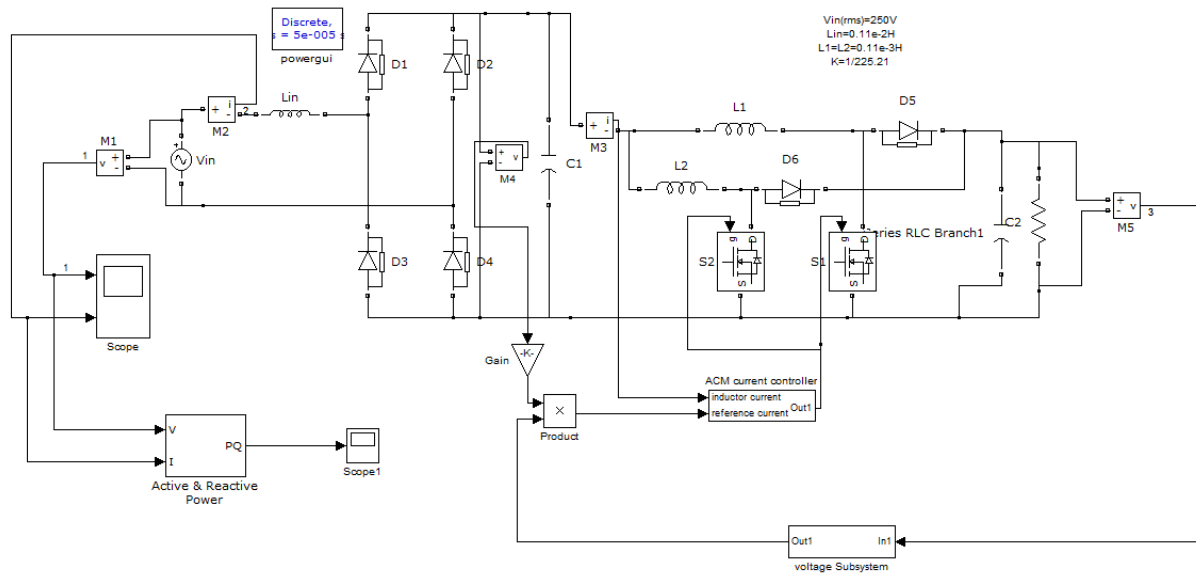


## 2D) FFT ANALYSIS FOR INPUT CURRENT:

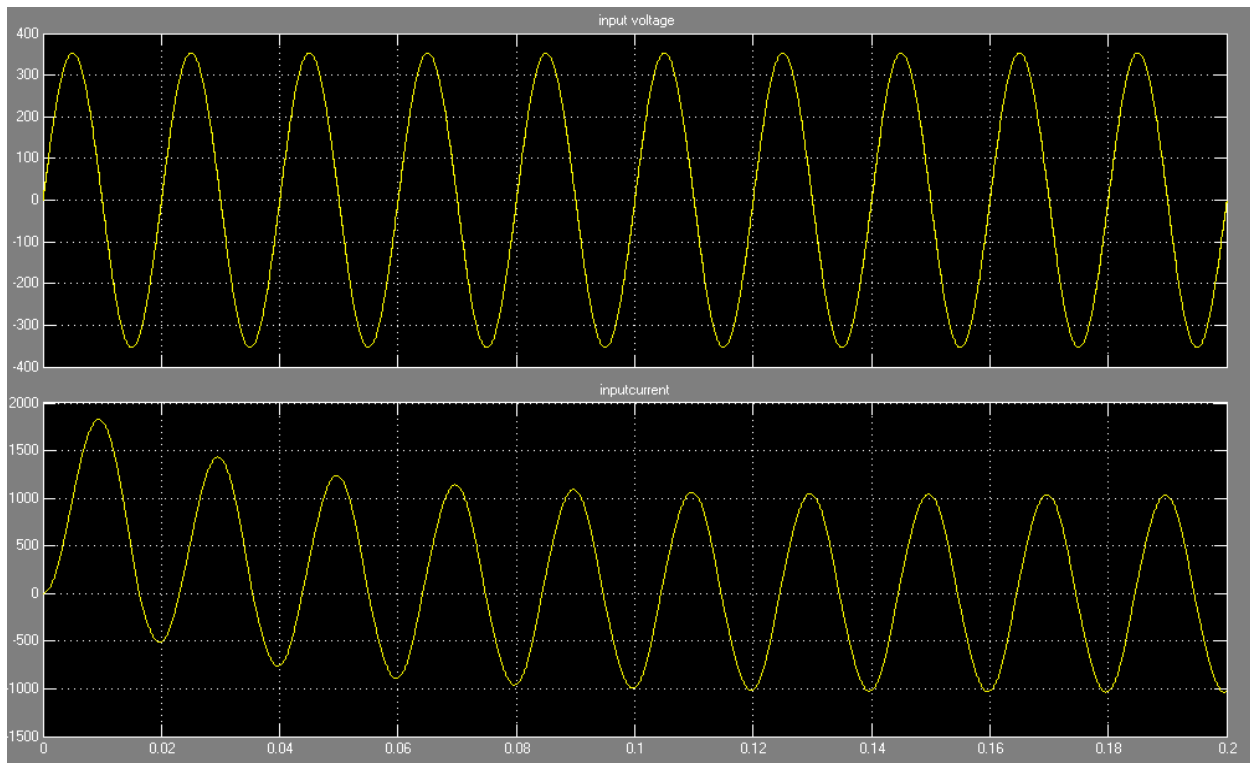


### 3) MODEL AND SIMULATION RESULTS FOR A PFC CIRCUIT WITH A PARALLEL BOOST CONVERTER:

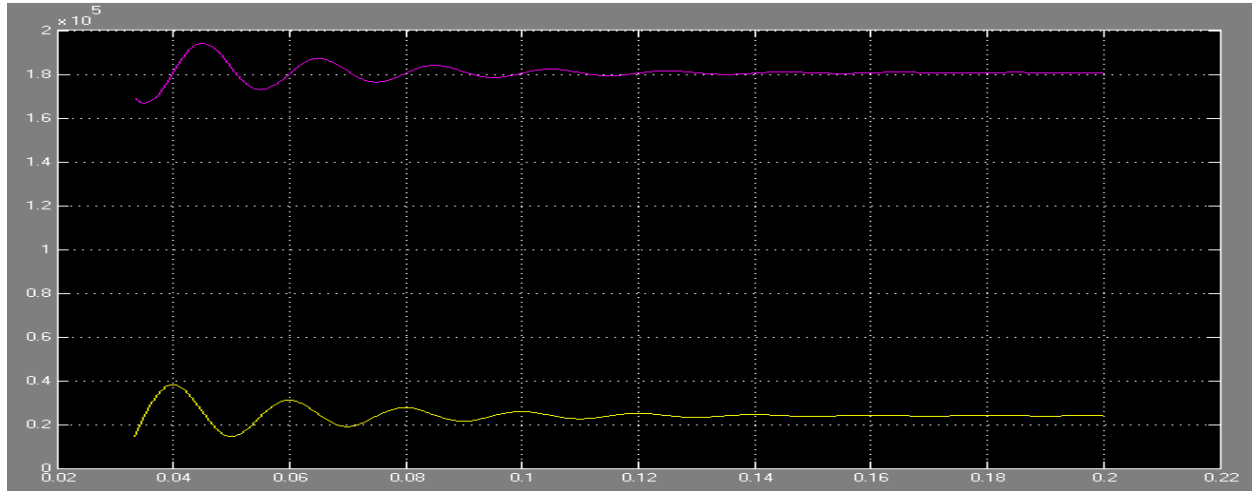
#### 3A) MODEL:



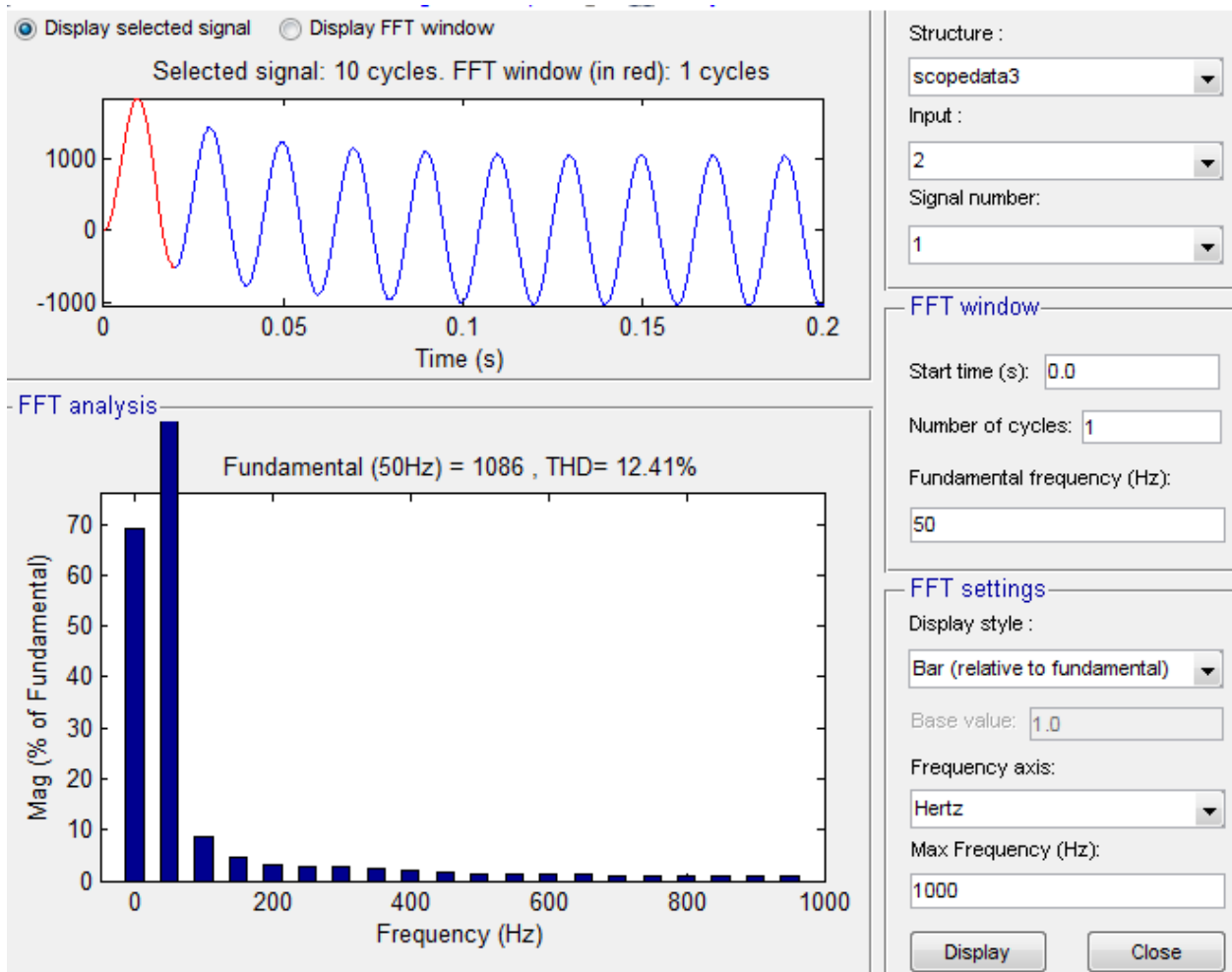
#### 3B) SIMULATION RESULTS:



### 3C) ACTIVE AND REACTIVE POWER:



### 3D) FFT ANALYSIS OF INPUT CURRENT:



## **CALCULATIONS:**

### **1) RECTIFIER CIRCUIT WITHOUT ANY PFC CIRCUIT:**

Active Power,  $P= 11.5 \text{ KW}$

Reactive Power,  $Q= 3.1 \text{ KVAR}$

Power Factor = 96.55%

THD = 1.03

### **2) RECTIFIER CIRCUIT WITH A BOOST CONVERTER FOR PFC:**

Active Power,  $P= 171.54 \text{ KW}$

Reactive Power,  $Q= 42.57 \text{ KVAR}$

Power Factor = 97.05%

THD = 0.1252

### **3) RECTIFIER CIRCUIT WITH A PARALLEL BOOST CONVERTER FOR PFC:**

Active Power,  $P= 180.53 \text{ KW}$

Reactive Power,  $Q= 23.98 \text{ KVAR}$

Power Factor = 99.12%

THD = 0.1241

## **CONCLUSION:**

The main objective throughout the project has been to improve the input Power Factor with simultaneous reduction of input current harmonics.

Simulations were initially done for elementary rectifier circuits without employing any PFC circuit. These simulations included circuits with and without source side inductors and capacitors. The changes in the input current waveform were observed and studied.

A PFC circuit having a parallel boost converter i.e. two boost converters arranged in parallel was designed. The control strategy was based on average current mode control due to its relative advantages over voltage mode control and peak current mode control.

The key points that were taken into account while designing were:

- 1) Placing the two poles at origin and somewhere near the switching frequency.
- 2) Placing the zero at half the crossover frequency.
- 3) Gain of the inner current control loop should be in accordance to the switching frequency of the PWM modulator.

Calculation of Power Factor was done base on active and reactive power measurement with the inbuilt MATLAB block for the same.

For the purpose of comparison and to validate the improvement in power factor, Power factor and THD (Total Harmonic Distortion) for three circuits:

**CIRCUIT 1) Rectifier Circuit only without any PFC.**

**CIRCUIT 2) Rectifier Circuit with a single boost converter for PFC.**

**CIRCUIT 3) Rectifier Circuit with a parallel boost converter for PFC.**

were calculated. The results are summarised as below:

	<b>INPUT POWER FACTOR</b>	<b>THD</b>
<b>CIRCUIT 1</b>	<b>96.55%</b>	<b>1.03</b>
<b>CIRCUIT 2</b>	<b>97.05%</b>	<b>0.1252</b>
<b>CIRCUIT 3</b>	<b>99.12%</b>	<b>0.1241</b>

As, can be seen from the above table, the power factor has improved from 96.55% in a rectifier circuit without any PFC to 99.12% in a circuit employing a parallel boost converter for Power Factor Correction.

As regards, the reduction of harmonics, it was observed an inductor placed on the input side acts as filter and reduces the higher order harmonics considerably. For e.g. In circuit 3 introduction of a source side inductor reduced the THD from 0.41 to 0.125 which is indeed a considerable reduction.



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