STUDY THE EFFECT OF INPUT FILTER FOR BUCK CONVERTER

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE
REQUIRMENTS FOR THE DEGREE OF BACHELOR OF TECHNOLOGY IN
ELECTRICAL ENGINEERING

BY

PRASANTA KUMAR THAKUR (107EE014)

SUDAM CHARAN MAJHI (107EE019)

Under the guidance of

Prof. S. SAMANTA

NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA

DEPARTMENT OF ELECTRICAL ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
ROURKELA -769008

CERTIFICATE

This is to certify that the thesis entitled "**STUDY THE EFFECT OF INPUT FILTER FOR BUCK CONVERTER**" submitted by **Prasanta Kumar Thakur (roll no.-107ee014) and Sudam Charan Majhi (roll no.-107ee019) in** the partial fulfillment of the requirement for the degree of Bachelor of Technology in Electrical Engineering, National Institute of Technology, Rourkela, is an authentic work carried out by them under my supervision.

To the best of my knowledge the matter embodied in the thesis has not been submitted to any other university/institute for the award of any degree or diploma.

Date
Rourkela

Professor S. Samanta
Department of Electrical Engineering
National Institute of Technology
Rourkela-769008

ACKNOWLEDGEMENT

We have taken efforts in this project. However, it would not have been possible without the kind support and help of many individuals and organizations. we would like to extend our sincere thanks to all of them. We would like to express our sincere gratitude towards our teacher and guide **Prof S. Samanta** for his guidance and constant supervision as well as for providing necessary information regarding the project & also for his support in completing the project.

Last but not least we would like to thanks all our dear friends for helping us throughout the project work and people who have willingly helped out with their abilities.

Regards;

Prasanta Kumar Thakur
Roll no.-107EE014

Sudam Charan Majhi
Roll no.-107EE019

ABSTRACT

Small signal model of current-controlled mode DC-DC buck converter is studied using small signal block diagrams. Input filter reduces the electromagnetic interference (EMI) of power input of converter and improves the performance of load. However, input filter added to reduce the electromagnetic interference will changes the system transfer function, which may create instability in the converter. Therefore, input filter should be such that it will reduce the electromagnetic interference as well as it should not induce any negative effect on current-controlled mode DC-DC converter.

CONTENTS

CHAPTER 1.

CHAPTER 2

CHAPTER 3.

CHAPTER 4.

CHAPTER 5.

CHAPTER 6.

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 Overview

1.2 Basics of DC-DC converters.

  1.2.1 Buck converter

  1.2.2 Boost converter

1.3 Modeling of DC-DC converter

1.1 OVERVIEW

Electromagnetic interference (EMI) is disturbance due to either electromagnetic induction or electromagnetic radiation emitted from external source that affect the electrical circuit. The EMI may interrupt or reduce the effective performance of the electrical circuit. The EMI source may be any object or artificial or natural, that carries rapidly changing electrical current, such as an electrical device.

Hence an input filter is generally used to reduce the electromagnetic interference in power source side of a converter. An input filter is a combination of resistor, capacitor and inductor that used to reject signals, vibrations, or radiations of certain frequencies while allowing others to pass through it. Capacitor blocks low-frequency signals and conduct high-frequency signals, while inductor does the reverse.

However, the input filter added to the peak current-mode (PCM)-controlled converter as it offers desired characteristics such as, automatic overload protection, dynamic response, automated feedback compensation, input disturbance rejection and current sharing loop [4]. But PCM controlled converter changes the dynamic properties, stability, current loop gain, transfer function of the converter[1].so not only should the input filter meet the design criteria to reduce the EMI, but the induced dynamic effect of the converter should be consider.

1.2 BASICS OF DC-DC CONVERTERS

DC-DC converter is an electronic circuit which converts a dc signal from one voltage level to another level by storing the input energy and realizing that energy to the output at different voltage. The energy storage be in either magnetic field storage component (inductors)or electric field storage components (capacitors).Most of the DC-DC converter are designed only in unidirectional power flow, from the input to output. However, all switching regulators can be made bidirectional by replacing all diodes with independently controlled active rectification.

1.2.1 BUCK CONVERTER

Buck converter is a step-down dc-dc converter that uses two switches (generally a transistor and a diode), an inductor and a capacitor. Here the switches are controlling the inductor [2].

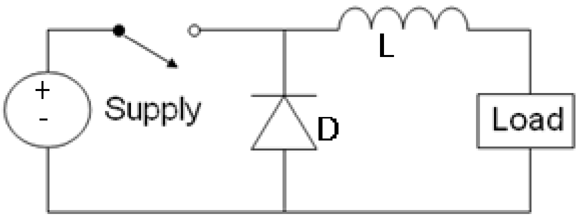

Fig 1.1

When the switch is closed (i.e. On-state), the voltage across the inductor is $V_L = V_i - V_0$. The current flowing through inductor linearly rises. As the diode is reversed biased by input voltage source (V_i) it doesn't allow current to flow through it.

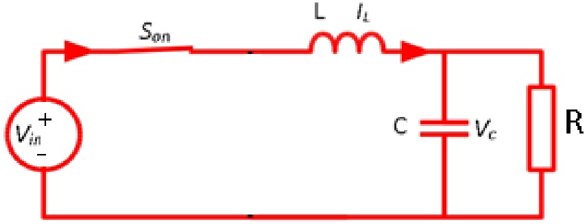

Fig 1.2

For Off Case (when switch is opened), diode is forward biased and voltage is $V_L = -V_0$

(Neglecting drop across diode) across inductor. The inductor current which was rising in ON case now decreases.

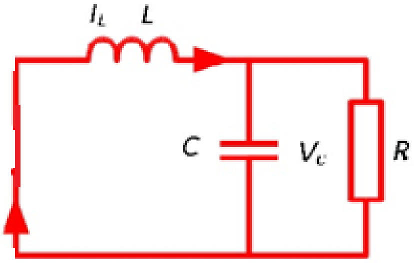

Fig 1.3

OPERATION

There are two modes of operation

(A) Continuous current mode (CCM)

Here the current through the inductor (I_L) never falls to zero during the whole switching period.

(B) Discontinuous current mode (DCM)

In some cases the energy required by the load is small enough to be transferred in a time lower than the whole commutation period. So the inductor current falls to zero during a part of the commutation period.

1.2.2 BOOST CONVERTER

A boost converter is a DC-DC step-up converter, as its name suggests steps up the input DC voltage value and provides at output. This converter contains generally a diode, a transistor as switches and at least one energy storage element. Capacitors are generally added to output so as to removing the output voltage ripple and sometimes inductors are also combined with [2].

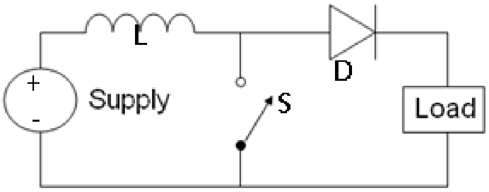

Fig 1.4

OPERATION

- During the ON period, Switch is closed its contacts and current through inductor increases.

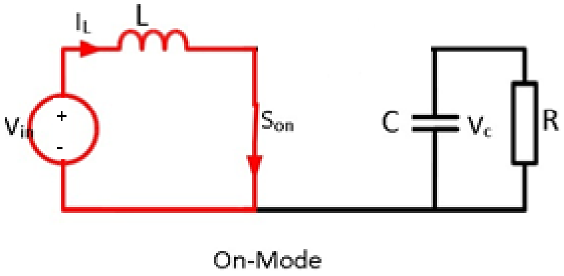

Fig 1.5

- During the OFF period, Switch is opened and thus the only path for inductor current to flow is through the fly-back diode 'D' and the parallel combination of capacitor and load. This makes inductor to transfer energy gained by it during ON period.

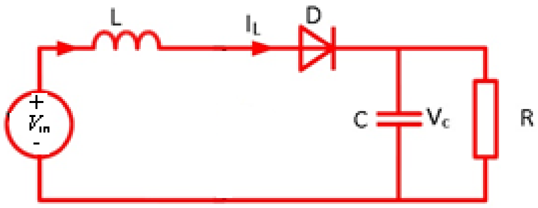

Fig 1.6

1.3 MODELING OF DC-DC CONVERTER

For modeling of converter two techniques can be use:

- Circuit averaging technique.
- State space averaging technique.

The circuit averaging technique approach has a number of advantages over state space averaging technique, these include:

- It’s applicable for both small and large signal modeling of converters.
- Rather than averaging and linearizing the converter state Equations, the averaging and linearization operations are performed directly on the converter circuit [5].
- Both DC and AC transfer function models of converters are obtained.
- We will use it to model DCM, CCM, and resonant converters [5].

CHAPTER 2

CIRCUIT AVERAGE MODEL

2.1 INTRODUCTION

Circuit averaging is a method to derive the AC/DC converter models. We will average DC-DC converters waveforms and topologies rather than the circuit differential equations. It works not only for dc-dc converters but also for, three phase inverters, Phase Controlled Rectifiers, resonant Converters, and Current Controlled Converters. The main aim to replace the time varying switches by time invariant current and voltage sources or PWM(pulse width modulated) switch.

It is also called time invariant model for DC-DC converters.

2.2 CIRCUIT AVERAGING METHOD

- First choose the dependent and independent variables and then averaging them over switching time period $T_S (< >T_S)$ [3].
- Perturbation, linearize and then neglecting the second order effects.
- Placed the dependent current and voltage sources as per circuit topologies requirement.
- Combine input and output to achieve one AC/DC transformer [4].

Before starting circuit averaging we assumed some circuit requirement.

- ➢ Converter switch network is less than or equal to the number of SPST (single pole single throw) switches.
- ➢ For simple DC-DC converters it contains two SPST switches and switch network contains two ports.
- ➢ The switch network terminal waveforms are representing the port voltage and current: $v_1(t),\ i_1(t), v_2(t)$ and $i_2(t)$.
- ➢ Two of these above parameters can be taken as independent inputs to the switch network and the remaining two are taken as dependents outputs of the switch network.

2.2.1 CIRCUIT AVERAGE MODEL FOR BUCK CONVERTER

Buck converter is a step-down DC-DC converter. It's containing two switch network and two switching ports.

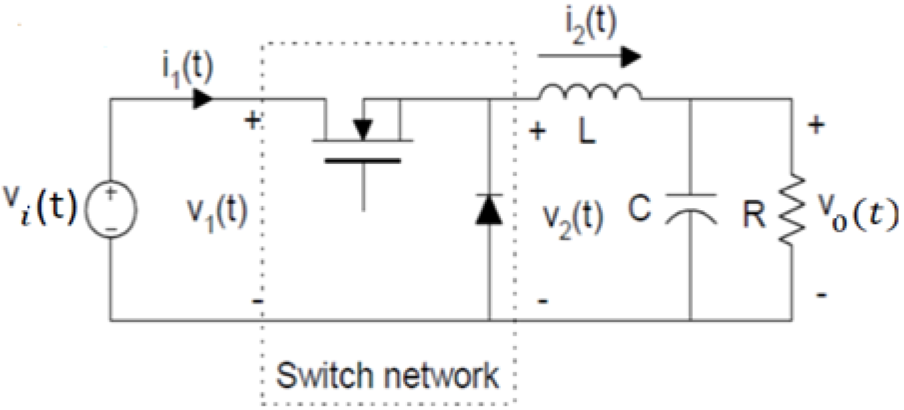

Fig 2.1

SWITCHING PORTS

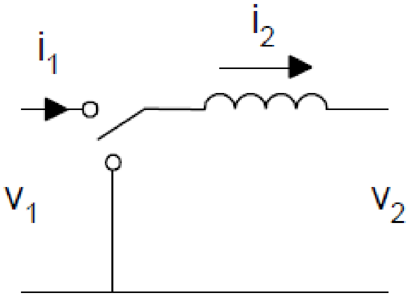

Fig 2.2

Buck converter having two switching ports with four variables (v_1, i_1, v_2 and i_2). Here i_2 and v_1 are the best choice of independent variables.
Dependent variables are v_2 and i_1.

Now we can plot both $i_2(t)$ and $v_1(t)$ versus time easily.

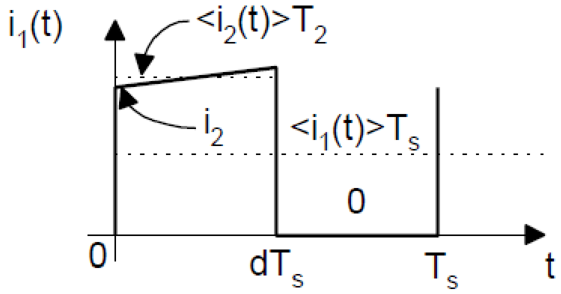

Fig 2.3

$<i_1>T_s=<i_2>dT_s+<0>(1-d)\ T_s$

Here $d'=1-d$ and T_s=switching period of buck converter

So $i_1= f_x\ (i_2,v_1)$

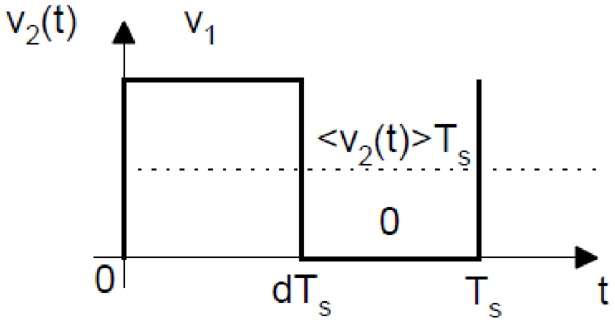

Fig 2.4

$<v_2>=<v_1>dT_s+<0>(1-d)\ T_s$

So $v_2 = f_y(i_2, v_1)$

By averaging the above dependent variables over switching time period T_s then we get a time invariant switch model [4].

DEPENDENT INDEPENDENT

$<i_1>T_s = d<i_2>T_s\ =di_2$

$<v_2>T_s = d<v_1>T_s\ =dv_1$

Where: $d=D+\hat{d}$

$\hat{d}$=duty ratio

The above large signal models are then linearized to obtain small signal models.

2.2.2 CIRCUIT AVERAGE MODEL FOR BOOST CONVERTER.

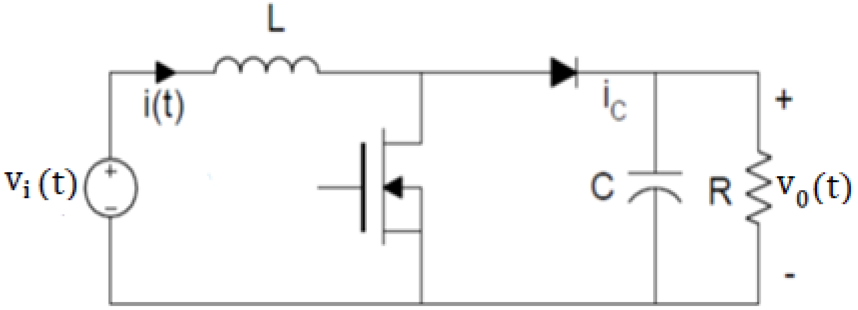

Fig 2.8

The controlling inductor with the right terminal going from ground to v_0 will be replaced by a time invariant two port which containing a DC transformer, a dependent voltage (input) and current (output) source [5].

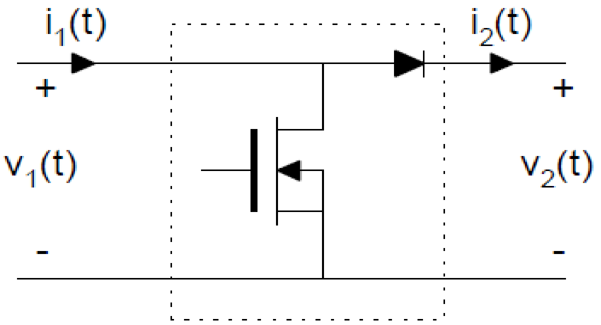

Fig 2.9

Here $i_1(t)$ and $v_2(t)$ are the two independent variables and we can easily plot $i_1(t)$ and $v_2(t)$ versus switching time.

Moreover, both $i_1(t)$ and $v_2(t)$ are not varying during ON period.

We can write dependent variables $(i_2(t), v_1(t))$ in terms of independent variables $(i_1(t), v_2(t))$.

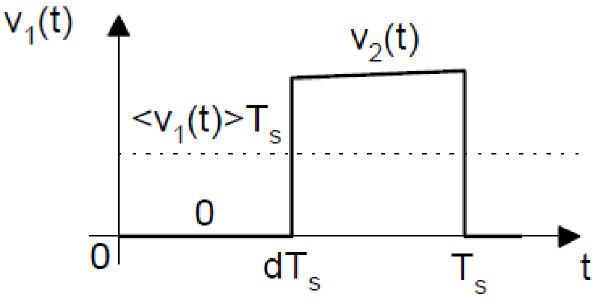

Fig 2.10

$v_1 = f_1(i_1, v_2)$

Then averaging the dependent variable $v_1(t)$ over switching period T_S.

$<v_1(t) > T_S =< 0 > dT_S + d'<v_2(t)>T_S = d'v_2$

Where d'=1-d

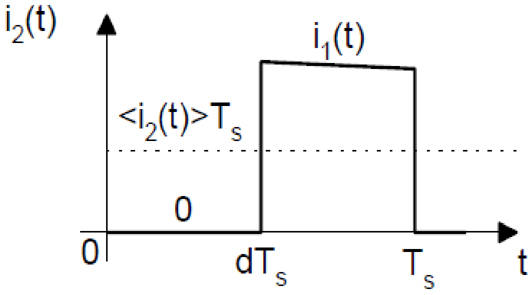

Fig 2.11

$i_2 = f_2(i_1, v_2)$

Then averaging the dependent variable $i_2(t)$ over switching period T_S in terms of independent variable.

$<i_2(t) > T_S = <0>dT_S + d' < i_1(t) > T_S = d'i_1$

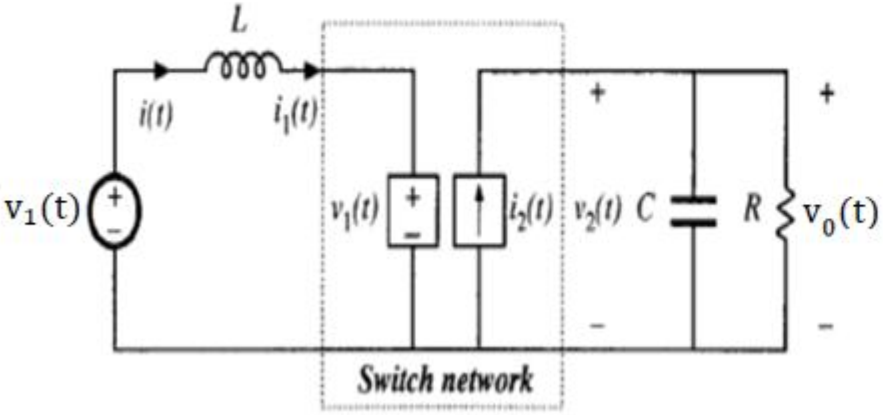

Fig 2.12

2.3 LINEARIZATION OF DC-DC CONVERTERS.

The large signal model have non-linear terms comes from product of two time varying quantities. We can liberalize the large signal model by expanding about the operating point and remove the second order terms [5].

$$d(t)=D+\hat{d}(t) \;\; => \;\; d'(t) = D' - \hat{d}(t)$$

$$< v_i(t) >_{T_S} = V_i + \hat{v}_i(t)$$

$$< i(t) >_{T_s} =< i_1(t) >_{T_s} = I + \hat{\imath}(t)$$

$$< v(t) >_{T_s} = < v_2(t) >_{T_s} = V+\hat{v}(t)$$

$$< v_1(t) >_{T_s} = V_1 + \hat{v}_1(t)$$

$$< i_2(t) >_{T_s} = I_2 + \hat{\imath}_2(t)$$

2.3.1 LINEARIZATION OF BUCK CONVERTER

(A) <u>Dependent current source in primary</u>

Here di_2 is the dependent current source and large signal model is the starting point.

$di_2 = (D + \hat{d})(I_2 + \hat{\imath}_2) = D(I_2 + \hat{\imath}_2) + I_2\hat{d} + \hat{\imath}_2\hat{d}$

To simplify, multiply out and neglect second order terms, $\hat{\imath}_2\hat{d}$

To get small signal model input circuit.

$=> D\,(I_2 + \hat{\imath}_2) + I_2\hat{d}$

RESULT

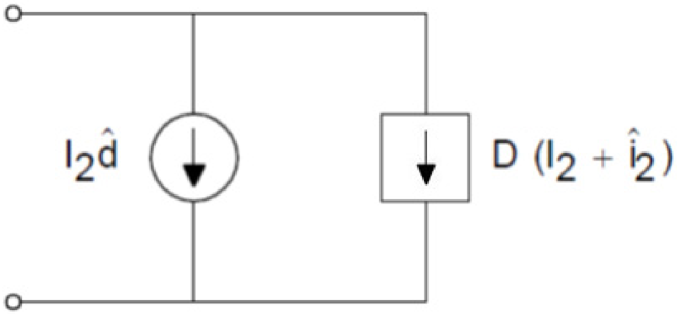

Fig 2.5

(B) Dependent voltage source in secondary

Here dv_1 is the dependent voltage source

$dv_1 = (D+\hat{d})\,(V_1 + \hat{v}_1)$

$= D\,(V_1 + \hat{v}_1) + V_1\hat{d} + \hat{v}_1\hat{d}$

To simplify, multiply out and neglect second order terms to
Get small signal output model.

$= D(V_1 + \hat{v}_1) + V_1\hat{d}$

RESULT

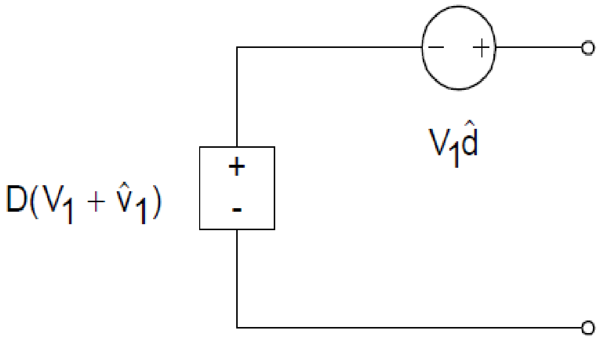

Fig 2.6

(C) Combine small signal I/O circuits via ac/DC transformer.

The dependent DC sources are replaced by an equivalent ideal DC transformer with turns ratio 1:D. This gives final DC and small signal AC circuit averaged model [5], [3].

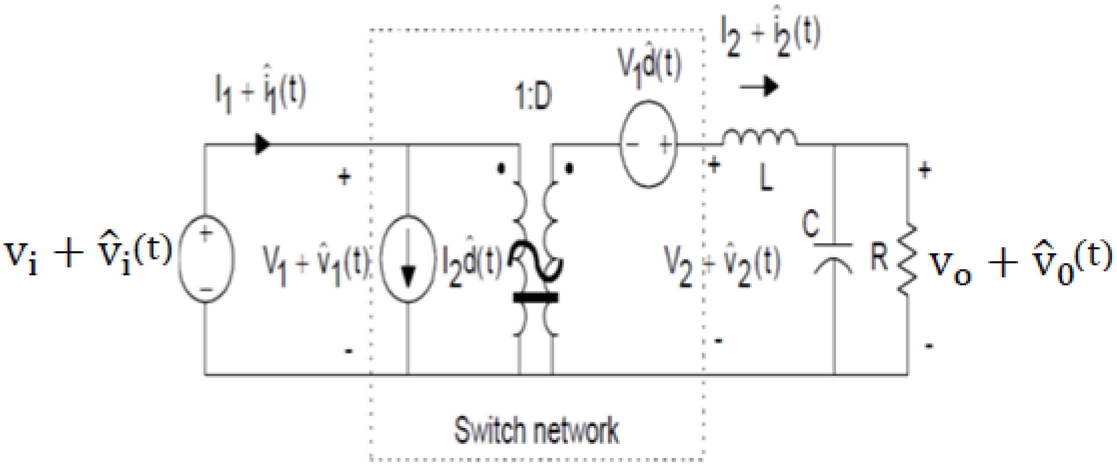

Fig 2.7

For a DC model only, assume $\hat{d} \to 0$ and we get the old DC Buck converter model.

2.3.2 LINEARIZATION OF BOOST CONVERTER

(A) Dependent voltage source in primary side.

Here $d'=D'-\hat{d}(t)$

$<v_1(t)>T_S=d'<v_2(t)>T_S=d'v_2=(D'-\hat{d}(t))\left(V_2+\hat{v}_2(t)\right)$

$$= D'\left(V_2+\hat{v}_2(t)\right) - V_2\hat{d}(t) - \hat{v}_2(t)\hat{d}(t)$$

Multiply out the product terms and neglect second order
Terms $\hat{v}_2(t)\hat{d}(t)$ in the input circuit. The result is the new input circuit model:

$$= D'\left(V_2+\hat{v}_2(t)\right) - V_2\hat{d}(t)$$

RESULT

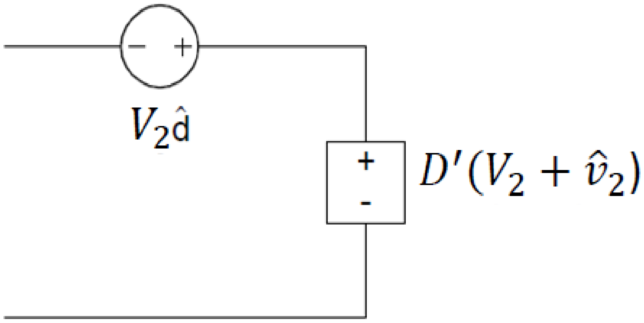

Fig 2.13

(B) Dependent current source in secondary

$<i_2(t)>_{T_S} = <0> dT_S + d' <i_1(t)>_{T_S} = d'i_1$

$\Rightarrow d'i_1 = (D'-\hat{d})(I_1+\hat{i}_1)$

To simplify, multiply out and neglect second order terms in the output circuit.

$(D'-\hat{d}(t))(I_1+\hat{i}_1(t)) = D'(I_1+\hat{i}_1(t)) - I_1\hat{d}(t) - \hat{i}_1(t)\hat{d}(t)$

$\Rightarrow D'\left(I_1+\hat{i}_1(t)\right) - I_1\hat{d}(t)$

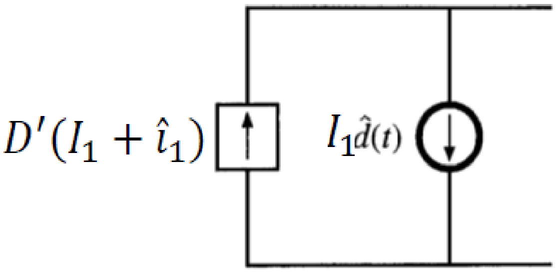

Fig 2.14

(C) Combine the small signal I/O circuits via DC/ac transformer

The dependent sources are replaced by an equivalent ideal DC transformer with turns ratio $D':1$. This gives the final DC and small-signal ac circuit-averaged model for boost converter.

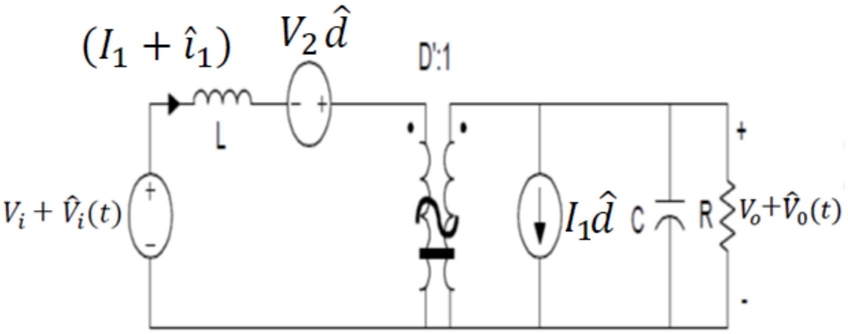

Fig 2.15

For DC model only, let $\hat{d} \rightarrow 0$ and we get the old DC boost converter model.

CHAPTER 3

SMALL SIGNAL MODELING OF PCM-CONTROLLED DC-DC BUCK CONVERTER

3.1 peak current mode control for buck converter.

3.2 Derivation of current loop transfer function.

- 3.2.1 Derivation without input filter (without k_f andk_r)
- 3.2.2 Derivation with input filter (without k_f andk_r)
- 3.2.3 Derivation without input filter (with k_f andk_r)
- 3.2.4 Derivation with input filter (with k_f andk_r)

3.1 PEAK CURRENT MODEL CONTROL FOR BUCK CONVERTER

Current mode-control is the standard industrial method for controlling switching power supplies for different electrical drives. The peak current of the converter is regulated by a control reference signal. Current-mode control employs an inductor current feedback loop and a voltage feedback loop [12].

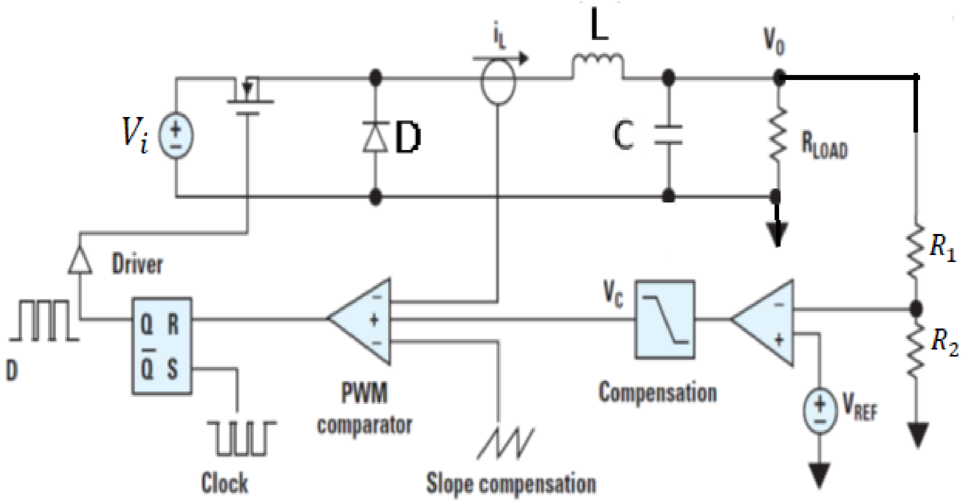

Fig 3.1

The output voltage(V_0) of DC-DC converter is fed back to an error amplifier where its compare with some reference voltage. When there is a difference between output voltage and amplifier reference voltage it gives an amplified error voltage signal. This amplified error voltage signal is known as control voltage signal then it fed back to PWM comparator forming outer voltage control loop [13].

The ripple current of inductor is sensed and converted into equivalent ramp signal. This ramp of inductor current is combined with a slope compensation signal and fed back to PWM comparator, forming inner current control loop. Here slope compensation signal increases the stability of converter beyond 50% duty ratio (D).

We have been motivated from paper [1], where they have derived the current loop gain for PCM controlled buck converter considering $\mathrm{k_f}$ and $\mathrm{k_r}$. Generally the effect of $\mathrm{k_f}$ and $\mathrm{k_r}$ is very negligible. So we neglected these two parameters and derived the current loop gain for PCM-controlled buck converter as well as the design criteria for input filter.

3.2 DERIVATION OF CURRENT LOOP TRANSFER FUNCTION.

PCM-controlled buck converter with an input filter

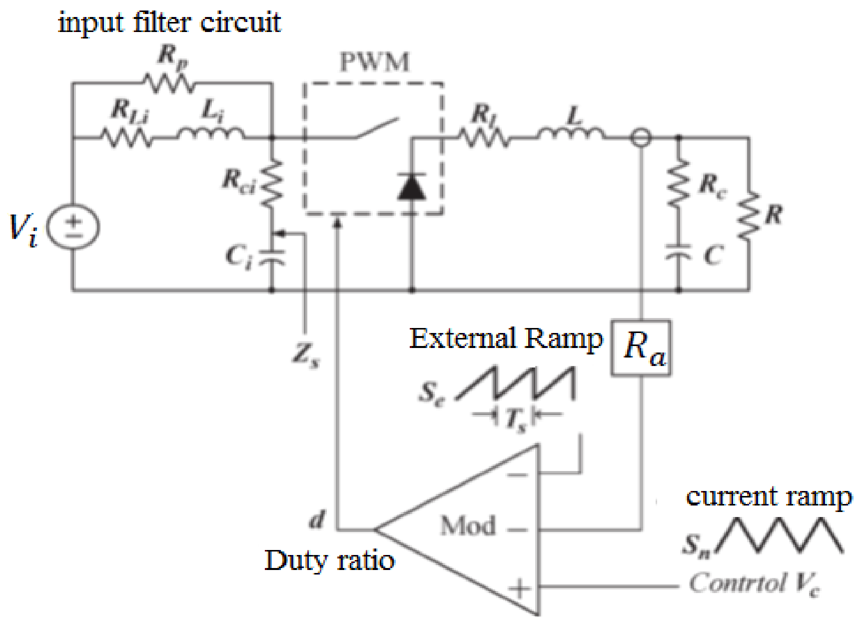

Fig 3.2

SMALL SIGNAL MODEL OF PCM-CONTROLLED BUCK CONVERTER WITH AN INPUT FILTER Z_S

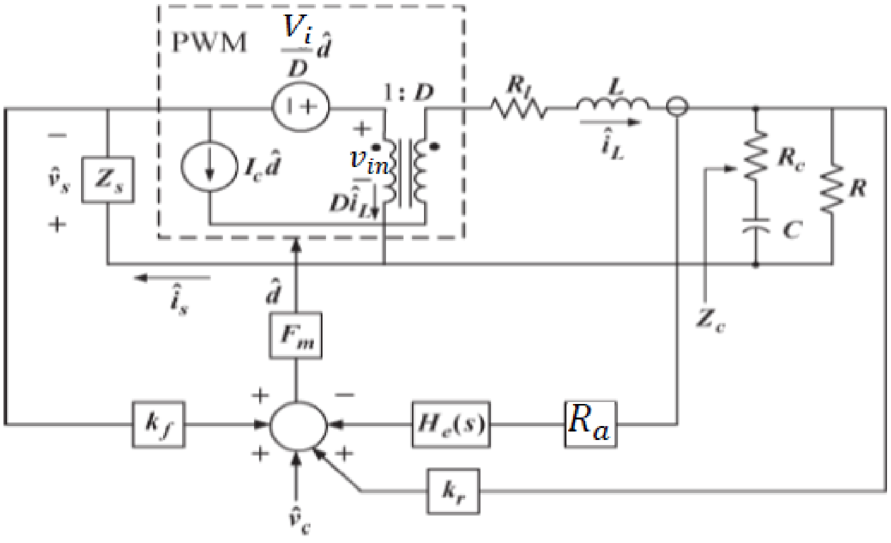

Fig 3.3

3.2.1 DERIVATION WITHOUT INPUT FILTER (without $\mathrm{k_f}$ and $\mathrm{k_r}$)

Without input filter impedance $\mathrm{Z_S}$, the dependent current source is shorted and the inductor current $\hat{\mathrm{i}}_\mathrm{L}$ is representing as:

$$\hat{\mathrm{i}}_\mathrm{L} = \frac{\mathrm{V_i}\hat{\mathrm{d}}}{\mathrm{sL + R_l + R \parallel \left(R_c + \frac{1}{sC}\right)}} = \mathrm{V_i Y}\hat{\mathrm{d}} \qquad (1)$$

Where;

$$\mathrm{Y} = \frac{1}{\mathrm{sL + R_l + R \parallel \left(R_c + \frac{1}{sC}\right)}} \qquad (2)$$

$$\mathrm{Z_c} = \mathrm{R} \parallel \left(\mathrm{R_c} + \frac{1}{\mathrm{sC}}\right) \qquad (3)$$

$$\hat{\mathrm{d}} = \mathrm{F_m}(\hat{\mathrm{v}}_\mathrm{c} - \hat{\mathrm{i}}_\mathrm{L}\mathrm{R_a})$$

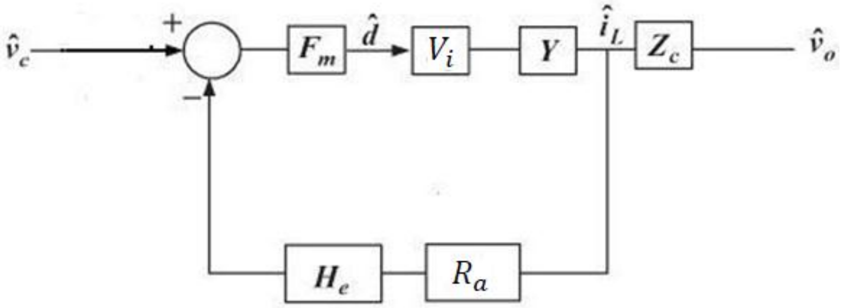

Fig 3.3

Here $\mathrm{H_e(s)}$=1

Now current loop gain given by;

$$\mathrm{T_g(s)} = \mathrm{F_m V_i Y H_e(s) R_a} \qquad (4)$$

3.2.2 DERIVATION WITH INPUT FILTER (without $\mathrm{k_f}$ and $\mathrm{k_r}$)

When input filter is considered, the terminal voltage of $\mathrm{Z_s}$ in figure can be expressed as below,

$$\hat{\mathrm{v}}_\mathrm{s} = \left(\mathrm{D}\hat{\mathrm{i}}_\mathrm{L} + \mathrm{I_c}\hat{\mathrm{d}}\right)\mathrm{Z_s} \qquad (5)$$

Applying KVL

$$\hat{\mathrm{v}}_\mathrm{in} = \frac{\mathrm{V_i}\hat{\mathrm{d}}}{\mathrm{D}} - \hat{\mathrm{v}}_\mathrm{s} \qquad (6)$$

Substituting equation (5) in (6) and rearranging we get,

$$\hat{v}_{in} = \left(\frac{V_i}{D} - Z_s I_c\right)\hat{d} - DZ_s\hat{\imath}_L \qquad (7)$$

Again we know,

$$\hat{\imath}_L = D\hat{v}_{in}Y$$

$$\gg \hat{v}_{in} = \frac{\hat{\imath}_L}{DY} \qquad (8)$$

Putting equation (8) in (7) we get,

$$\frac{\hat{\imath}_L}{DY} = \left(\frac{V_i}{D} - Z_s I_c\right)\hat{d} - DZ_s\hat{\imath}_L$$

$$\gg \hat{\imath}_L = \frac{(\frac{V_i}{D} - Z_s I_c)\hat{d}}{(\frac{1}{DY} + DZ_s)}$$

$$= \frac{DY(\frac{V_i}{D} - Z_s I_c)\hat{d}}{(1 + D^2 YZ_s)}$$

$$= \frac{YV_i\left(1 - \frac{DI_c Z_s}{V_i}\right)\hat{d}}{(1 + D^2 YZ_s)}$$

$$= \frac{V_i Y(1 - \frac{D^2 I_c Z_s}{DV_i})\hat{d}}{(1 + D^2 YZ_s)}$$

$$\gg \hat{\imath}_L = \frac{V_i Y(1 - \frac{D^2 Z_s}{R})\hat{d}}{(1 + D^2 YZ_s)} \qquad (9)$$

$\hat{d}$ Can be written as,

$$\hat{d} = Fm(\hat{v}_c - \hat{\imath}_L R_a) \qquad (10)$$

Now from eq.(9) and (10) we can draw the block diagram with modified current loop gain

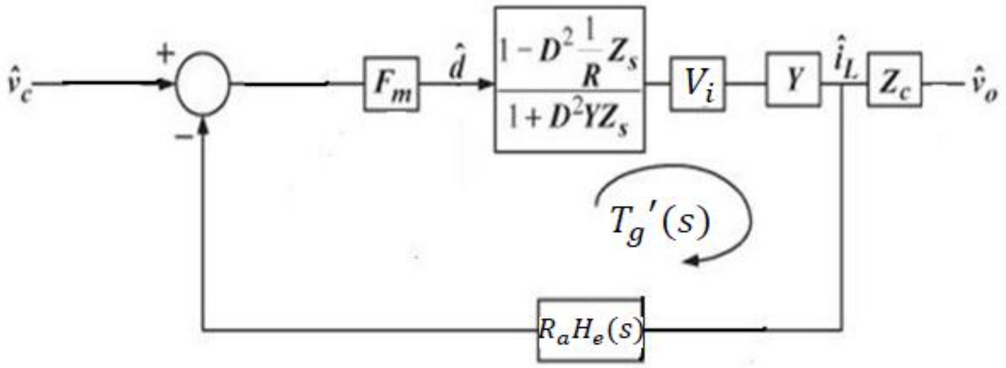

Fig 3.4

Thus modified current loop gain is given by;

$$T_g{}'(s) = F_m V_i Y R_a H_e(s)\left(\frac{1-\frac{D^2Z_s}{R}}{1+D^2YZ_s}\right) \tag{11}$$

3.2.3 DERIVATION WITHOUT INPUT FILTER (with k_f and k_r)

Without input filter impedance Z_s, the dependent current source $I_c\hat{d}$ should be shorted derectly.

Now;

$$\hat{v}_{in} = \frac{V_i\hat{d}}{D}$$

Its corresponding secondary voltage is

$$V_i\hat{d}$$

Thus current $\hat{i}_L$ is given by;

$$\hat{i}_L = \frac{V_i\hat{d}}{sL + R_l + R \parallel (R_c + \frac{1}{sC})} = V_iY\hat{d} \tag{12}$$

Where;

$$Y = \frac{1}{sL + R_l + R \parallel (R_c + \frac{1}{sC})} \tag{13}$$

$$Z_c = R + \left(R_c + \frac{1}{sC}\right)$$

Now the duty ratio $\hat{d}$ is given by

$$\hat{d} = F_m(\hat{v}_c - \hat{i}_L R_a H_e + \hat{v}_0 k_r) \tag{14}$$

From equation (14) and (16) we can draw the block diagram;

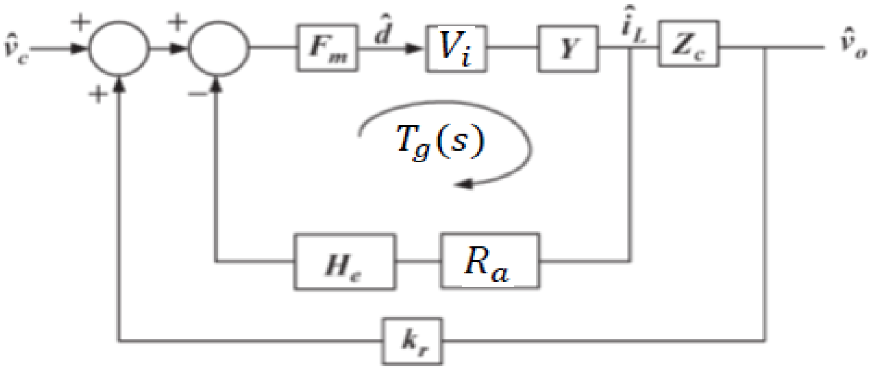

Fig 3.5

From the block diagram, the current loop gain is given by;

$$T_g(s) = F_m V_i R_a Y H_e \tag{15}$$

3.2.4 DERIVATION WITH INPUT FILTER (with k_f and k_r)

When input filter is considered the terminal voltage of Z_s will appear and is given by;

$$\hat{v}_s = (D\hat{i}_L + I_c\hat{d})Z_s \tag{16}$$

Applying KVL, we get;

$$\hat{v}_{in} = \frac{V_i\hat{d}}{D} - \hat{v}_s \tag{17}$$

Substituting equation (16) in (17) we get;

$$\hat{v}_{in} = \frac{V_i\hat{d}}{D} - (D\hat{i}_L + I_c\hat{d})Z_s$$

$$= \left(\frac{V_i}{D} - Z_s I_c\right)\hat{d} - DZ_s\hat{i}_L \tag{18}$$

Now the corresponding secondary voltage of $\hat{v}_{in}$ is $D\hat{v}_{in}$

Now the current $\hat{i}_L$ is given by;

$$\hat{i}_L = D\hat{v}_{in}Y$$

$$\gg \hat{v}_{in} = \frac{\hat{i}_L}{DY} \qquad (19)$$

Putting eq.(19) in (18) we get,

$$\frac{\hat{i}_L}{DY} = \left(\frac{V_i}{D} - Z_s I_c\right)\hat{d} - DZ_s\hat{i}_L$$

$$\gg \hat{i}_L = \frac{\left(\frac{V_i}{D} - Z_s I_c\right)\hat{d}}{\left(\frac{1}{DY} + DZ_s\right)}$$

$$= \frac{DY(\frac{V_i}{D} - Z_s I_c)\hat{d}}{(1 + D^2YZ_s)}$$

$$= \frac{YV_i(1 - \frac{DI_cZ_s}{V_i})\hat{d}}{(1 + D^2YZ_s)}$$

$$= \frac{V_iY(1 - \frac{D^2I_cZ_s}{DV_i})\hat{d}}{(1 + D^2YZ_s)}$$

$$\gg \hat{i}_L = \frac{V_iY(1 - \frac{D^2Z_s}{R})\hat{d}}{(1 + D^2YZ_s)} \qquad (20)$$

Now $-k_f$ multiplied by equation (16), we get;

$$-k_f\hat{v}_s = -k_f\left(D\hat{i}_L + I_c\hat{d}\right)Z_s \qquad (21)$$

From the figure duty ratio $\hat{d}$ will be given by;

$$\hat{d} = F_m(\hat{v}_c - R_aH_e\hat{i}_L + k_r\hat{v}_0 - k_f\hat{v}_s) \qquad (22)$$

Putting equation (21) in (22), the duty ratio will be

$$\hat{d} = F_m\left(\hat{v}_c - R_aH_e\hat{i}_L + k_r\hat{v}_0 - k_f\left(D\hat{i}_L + I_c\hat{d}\right)Z_s\right)$$

$$= F_m[\hat{v}_c - (R_aH_e + k_fZ_sD)\hat{i}_L + k_r\hat{v}_0 - F_mk_fI_cZ_s\hat{d}]$$

$$\gg \hat{d} + F_m k_f Z_s I_c \hat{d} = F_m[\hat{v}_c - (R_a H_e + k_f Z_s D)\hat{i}_L + k_r \hat{v}_0]$$

$$\gg \hat{d} = \frac{F_m[\hat{v}_c - (R_a H_e + k_f Z_s D)\hat{i}_L + k_r \hat{v}_0]}{1 + k_f I_c Z_s F_m} \qquad (23)$$

From equation (20) and (23) we can draw the block diagram;

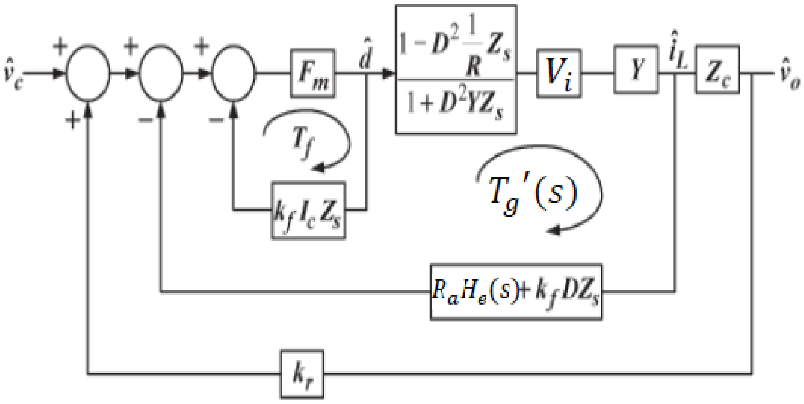

Fig 3.6

Now the modified current loop gain will be given by;

$$T'_g(s) = \frac{F_m V_i Y}{1 + k_f I_c Z_s F_m}\left(\frac{1 - \frac{D^2 Z_s}{R}}{1 + D^2 Y Z_s}\right)(R_a H_e + k_f Z_s D) \qquad (24)$$

CHAPTER 4

BASIC DESIGN CRITERIA FOR INPUT FILTER

4.1 Basic design criteria for input filter

4.2 Input filter parameters for buck converter

4.1 BASIC DESIGN CRITERIA FOR INPUT FILTER

(Considering $\mathrm{k_f}$ and $\mathrm{k_r}$)

Current loop gain from equation (15) without input filter is given by;

$$\mathrm{T_g(s)=F_m V_i Y R_a H_e(s)}$$

Current loop gain from eq (24) with inputfilter is given by;

$$\mathrm{T_g{}'(s) = \left(\frac{F_m}{1+k_f I_c Z_s F_m}\right)\left(\frac{1-D^2\frac{Z_s}{R}}{1+D^2 Y Z_s}\right) V_i Y (R_a H_e(s) + k_f D Z_s)}$$

If sampling effect is not taken into consideration ($\mathrm{i.e\ H_e(s)=1}$)

Now using eq(15) in eq(24), modified current loop gain($\mathrm{T_g{}'(s)}$) will be

$$\mathrm{T_g{}'(s) = \left(\frac{R_a + k_f D Z_s}{1+k_f I_c Z_s F_m}\right)\left(\frac{1-D^2\frac{Z_s}{R}}{1+D^2 Y Z_s}\right)\frac{T_g(s)}{R_a}}$$

$$\mathrm{= \left(\frac{1+k_f\frac{D}{R_a}Z_s}{1+k_f I_c Z_s F_m}\right)\left(\frac{1-D^2\frac{Z_s}{R}}{1+D^2 Y Z_s}\right)T_g(s)}$$

Now putting $\mathrm{Z_s = \frac{1}{Y_s}}$ (where $\mathrm{Y_s}$ is equivalent admittance of input filter)

$$\mathrm{T_g{}'(s) = \left(\frac{1+\frac{k_f D}{R_a Y_s}}{1+k_f I_c Z_s\frac{1}{Y_s}}\right)\left(\frac{1-\frac{D^2}{R Y_s}}{1+\frac{D^2 Y}{Y_s}}\right)T_g(s)}$$

$$\gg \mathrm{T_g{}'(s) = \left(\frac{1-\frac{Y_L}{Y_s}}{1+\frac{Y_h}{Y_s}}\right)\left(\frac{1-\frac{Y_c}{Y_s}}{1-\frac{Y_f}{Y_s}}\right)T_g(s)} \tag{25}$$

Where $\mathrm{Y_h = D^2 Y}$

$$\mathrm{Y_L = \frac{D^2}{R}}$$

$$\mathrm{Y_f = -k_f I_c F_m = \frac{D^2(1-\frac{D}{2})}{(1-D)R m_c}}$$

$$\mathrm{Y_c = -\frac{D k_f}{R_a} = \frac{D^2 T_s (1-\frac{D}{2})}{L}}$$

$m_c = 1 + \frac{S_e}{S_n}$

Where S_e=slope of external ramp ,S_n=slope of control ramp during on time

$k_f = -\frac{DT_sR_a}{L}(1 - \frac{D}{2})$

$k_r = \frac{T_SR_a}{2L}$

If the modified current loop gain is approximately equal to unmodified current loop gain

i.e $T_g{}'(s) \cong T_g(s)$

following fours conditions are obtained;

$$\left|\frac{Y_c}{Y_s}\right| \ll 1 \tag{26}$$

$$\left|\frac{Y_f}{Y_s}\right| \ll 1 \tag{27}$$

$$\left|\frac{Y_L}{Y_s}\right| \ll 1 \tag{28}$$

$$\left|\frac{Y_h}{Y_s}\right| \ll 1 \tag{29}$$

As the effect of $k_f$and k_r on converter is very less as they are very small, they can be neglected

Current loop gain from equation (4) without input filter is given by;

$$T_g(s)=F_mV_iYR_aH_e(s)$$

Current loop gain from equation(11)with inputfilter is given by;

$$T_g{}'(s) = F_m\left(\frac{1 - D^2\frac{Z_s}{R}}{1 + D^2YZ_s}\right)V_iYR_aH_e(s)$$

Now using eq(4) in eq(11), modified current loop gain($T_g{}'(s)$) will be

$$T_g{}'(s) = \left(\frac{1 - D^2\frac{Z_s}{R}}{1 + D^2YZ_s}\right)T_g(s)$$

$$T_g{}'(s) = \left(\frac{1 - \frac{Y_L}{Y_s}}{1 + \frac{Y_h}{Y_s}}\right)T_g(s) \tag{30}$$

Where $$Y_h = D^2 Y \qquad (31)$$

$$Y_L = \frac{D^2}{R} \qquad (32)$$

$$Z_s = \frac{1}{Y_s} \qquad (33)$$

If the modified current loop gain is approximately equal to unmodified current loop gain.

i.e $T_g{}'(s) \cong T_g(s)$

following two conditions will be satisfied

$$\left|\frac{Y_L}{Y_s}\right| \ll 1 \qquad (34)$$

$$\left|\frac{Y_h}{Y_s}\right| \ll 1 \qquad (35)$$

If inequality (34) not satisfied it will lead to oscillate and if inequality (35) is not satisfied converter dynamic performance will be degraded.

4.2 INPUT FILTER PARAMETERS FOR BUCK CONVERTER

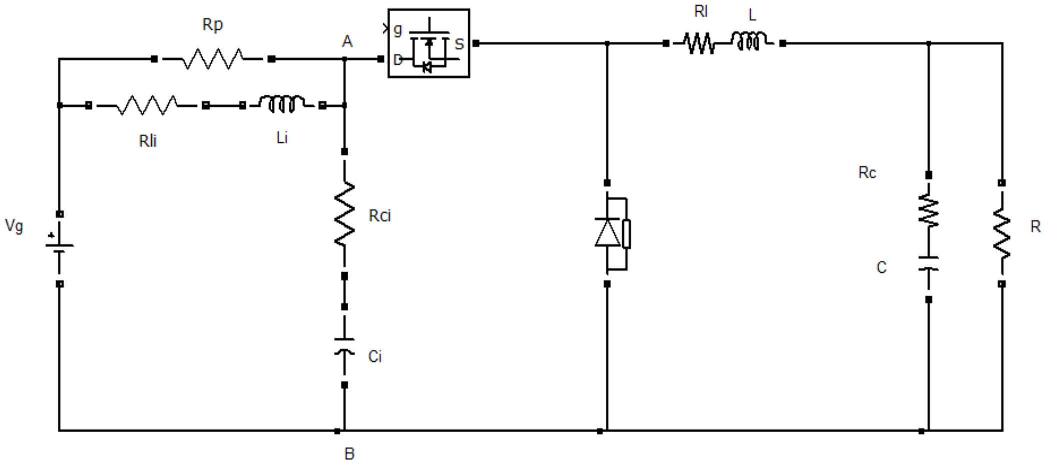

Fig 4.1

The equivalent circuit between point A and B excluding R_p is shown below;

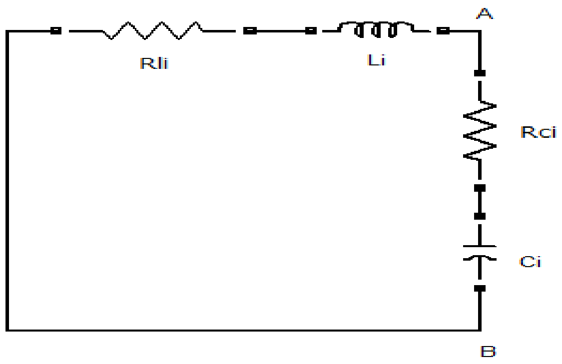

Fig 4.2

Now equivalent impedence(Z_s) between point A and B given by;

$$\frac{1}{Z_s} = \frac{1}{R_{li} + jwL_i} + \frac{1}{R_{ci} - j\frac{1}{wC_i}}$$

$$= \frac{R_{li} + R_{ci} + jwL_i - j\frac{1}{wC_i}}{(R_{li} + jwL_i)(R_{ci} - j\frac{1}{wC_i})}$$

Multiplying $(R_{li} - jwL_i)(R_{ci} + j\frac{1}{wC_i})$ both in neumerator and denominator ,we get;

$$= \frac{\left(R_{li} + R_{ci} + jwL_i - j\frac{1}{wC_i}\right)(R_{li} - jwL_i)(R_{ci} + j\frac{1}{wC_i})}{[{R_{li}}^2 + (wL_i)^2][{R_{ci}}^2 + (\frac{1}{wC_i})^2]}$$

$$= \frac{R_{ci}\left[{R_{li}}^2 + (wL_i)^2\right] + R_{li}\left[{R_{ci}}^2 + \left(\frac{1}{wC_i}\right)^2\right] + \frac{j}{wC_i}[{R_{li}}^2 + (wL_i)^2] - jwL_i[{R_{ci}}^2 + (\frac{1}{wC_i})^2]}{[{R_{li}}^2 + (wL_i)^2][{R_{ci}}^2 + (\frac{1}{wC_i})^2]}$$

$$= \frac{R_{ci}}{{R_{ci}}^2 + (\frac{1}{wC_i})^2} + \frac{R_{li}}{{R_{li}}^2 + (wL_i)^2} + j\frac{1}{wC_i[{R_{ci}}^2 + (\frac{1}{wC_i})^2]} - j\frac{wL_i}{{R_{li}}^2 + (wL_i)^2} \qquad (36)$$

Above equation can be written as;

$$\frac{1}{Z_s} = \frac{1}{R_{eq}} + \frac{1}{jwL_{eq}} + jwC_{eq}$$

Where $$\frac{1}{R_{eq}} = \frac{R_{li}}{{R_{li}}^2 + (wL_i)^2} + \frac{R_{ci}}{{R_{ci}}^2 + (\frac{1}{wC_i})^2} \qquad (37)$$

When frequency(w) is close to resonant frequency of inputfilter, it will have minimum admittance.

i.e

$$\mathrm{Y_{s(min)}} \approx \frac{1}{\mathrm{R_{eq(max)}}} + \frac{1}{\mathrm{R_p}} \qquad (38)$$

Where ;

$$\frac{1}{\mathrm{R_{eq(max)}}} = \frac{\mathrm{R_{li}}}{\mathrm{R_{li}}^2 + (\mathrm{wL_i})^2} + \frac{\mathrm{R_{ci}}}{\mathrm{R_{ci}}^2 + (\frac{1}{\mathrm{wC_i}})^2}$$

Putting w = $\frac{1}{\sqrt{\mathrm{LC}}}$

$$\frac{1}{\mathrm{R_{eq(max)}}} = \frac{\mathrm{R_{li}}}{\mathrm{R_{li}}^2 + \frac{\mathrm{L_i}}{\mathrm{C_i}}} + \frac{\mathrm{R_{ci}}}{\mathrm{R_{ci}}^2 + \frac{\mathrm{L_i}}{\mathrm{C_i}}} \approx \frac{\mathrm{R_{li}} + \mathrm{R_{ci}}}{\frac{\mathrm{L_i}}{\mathrm{C_i}}} \qquad (39)$$

The input filter of PCM controlled buck converter remains stable as long as $Y_{s(min)}$ satisfy the inequalities (34), (35). From equation (39) $R_{eq(max)}$ is directly proportional to $\frac{L_i}{C_i}$. If $\frac{L_i}{C_i}$ is large, $R_{eq(max)}$ will increase and not satisfy inequalities (34), (35) causing the converter to oscillate. So $\frac{L_i}{C_i}$ should not be very large [1].

CHAPTER 5

MATLAB SIMULATION

5.1 BUCK CONVERTER CIRCUIT PARAMETERS(R, L, C)

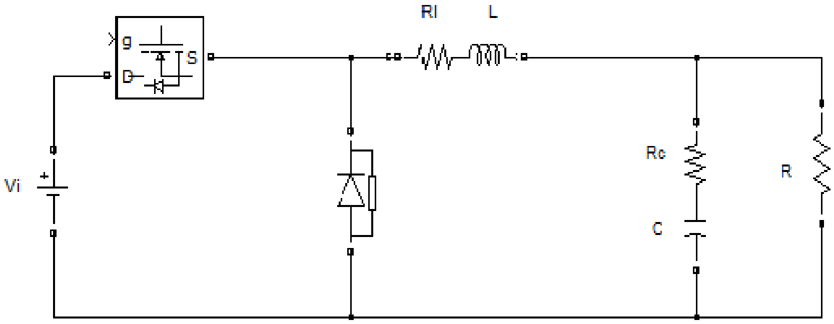

Fig 4.3

Let’s assume;

Input voltage (V_{in}) =12 volt

Output voltage (V_o) =4.8 volt

Load current (I_o) =3 ampere

As we know;

$V_o = DV_i$ ………… (1) Where D is duty ratio,

Given by $D=\frac{T_{on}}{T_{on}+T_{off}}$)

Putting the values V_{in} and V_o in eq(1)

$D =\frac{V_o}{V_{in}} = \frac{12}{4.8} =0.4$

Let us assume switching frequency (f_s) =100KH_z

$R= \frac{4.8}{3} = 1.6\ \Omega$

Taking inductor current ripple (ΔI_l) equal to 30% of I_o

Thus ΔI_l= 0.9 amp

Taking capacitor voltage ripple (ΔV) equal to 0.4% of V_o

Thus ΔV= 0.0192 volt

CALCULATION OF VALUE OF INDUCTOR

Current ripple factor is given by;

$\frac{\Delta I_l}{I_l} = \frac{(1-D)RT_s}{L}$ (where T_s is switching period)

$$\gg 0.3 = \frac{(1-0.4) \times 1.6 \times 10^{-5}}{L}$$

$$\gg L = 3.2 \times 10^{-5}\ H = 32\ \mu H$$

CALCULATION OF VALUE OF CAPACITOR

Voltage ripple factor is given by;

$$\frac{\Delta V}{V} = \frac{1-D}{8LCf^2}$$

$$\gg 0.004 = \frac{(1-0.4) \times 10^{-10}}{8 \times 32 \times 10^{-6} C}$$

$$\gg C = 0.5859 \times 10^{-4}\ F = 58.59\ \mu F$$

Assuming the Values of $R_l = 100 m\Omega$

$R_c = 50 m\Omega$

5.2 CALCULATION OFADMITTANCE Y_L, Y_h, Y_s:-

Here given data are D=0.4,R=1.6Ω ,L=32 µH,C=58.59μF,$R_l = 100\ m\Omega, R_c = 50\ m\Omega$,

$$R_{Li} = 0.3\Omega, R_{ci} = 0.01\Omega, L_i = 500\ \mu H, C_i = 700\ \mu F$$

From equation (32)

$$|Y_L| = \frac{D^2}{R} = \frac{0.4^2}{1.6} = 0.1$$

As we know from equation (31)

$$Y_h = D^2 Y$$

Where $Y = \frac{1}{sL + R_l + \frac{\frac{R(sCR_c+1)}{sC}}{R + sCR_c + 1}}$

Putting the value of L, C, R, R_c, R_l in above equation

Thus $Y = \frac{1}{20.1j+0.1+0.08836-0.24552j}$

$$= \frac{1}{19.85448j+0.18836}$$

$$= 0.000477785 - 0.050361933j$$

Putting the value of 'Y' in equation (31)

$$Y_h = 0.4^2(0.000477785 - 0.050361933j)$$

$$= 0.0000764456 - 0.0080579093j$$

Magnitude of Y_h is given by $|Y_h| = 0.008$

From equation (38) we know $|Y_s| \approx \frac{1}{R_{eq}} + \frac{1}{R_p}$

$$\approx \frac{R_{ci} + R_{Li}}{\frac{L_i}{C_i}} + \frac{1}{R_p}$$

$$\approx \frac{0.3 + 0.01}{\frac{500}{700}} + \frac{1}{2.5}$$

$$\approx 0.834$$

The values of $|Y_L|$, $|Y_h|$, $|Y_s|$ satisfies the inequalities(34), (35) and converter is stable and wave forms are shown in fig.5.6

When the value of L_i is larger than C_i

Let $L_i = 500$ µH and $C_i = 35$ µF

$$|Y_s| \approx 0.0717$$

Which does not satisfy the inequalities (34), (35) and converter oscillate. Wave forms are shown in fig.5.9

5.3 SIMULINK MODEL FOR PCM-CONTROLLED BUCK CONVERTER WITHOUT INPUT FILTER

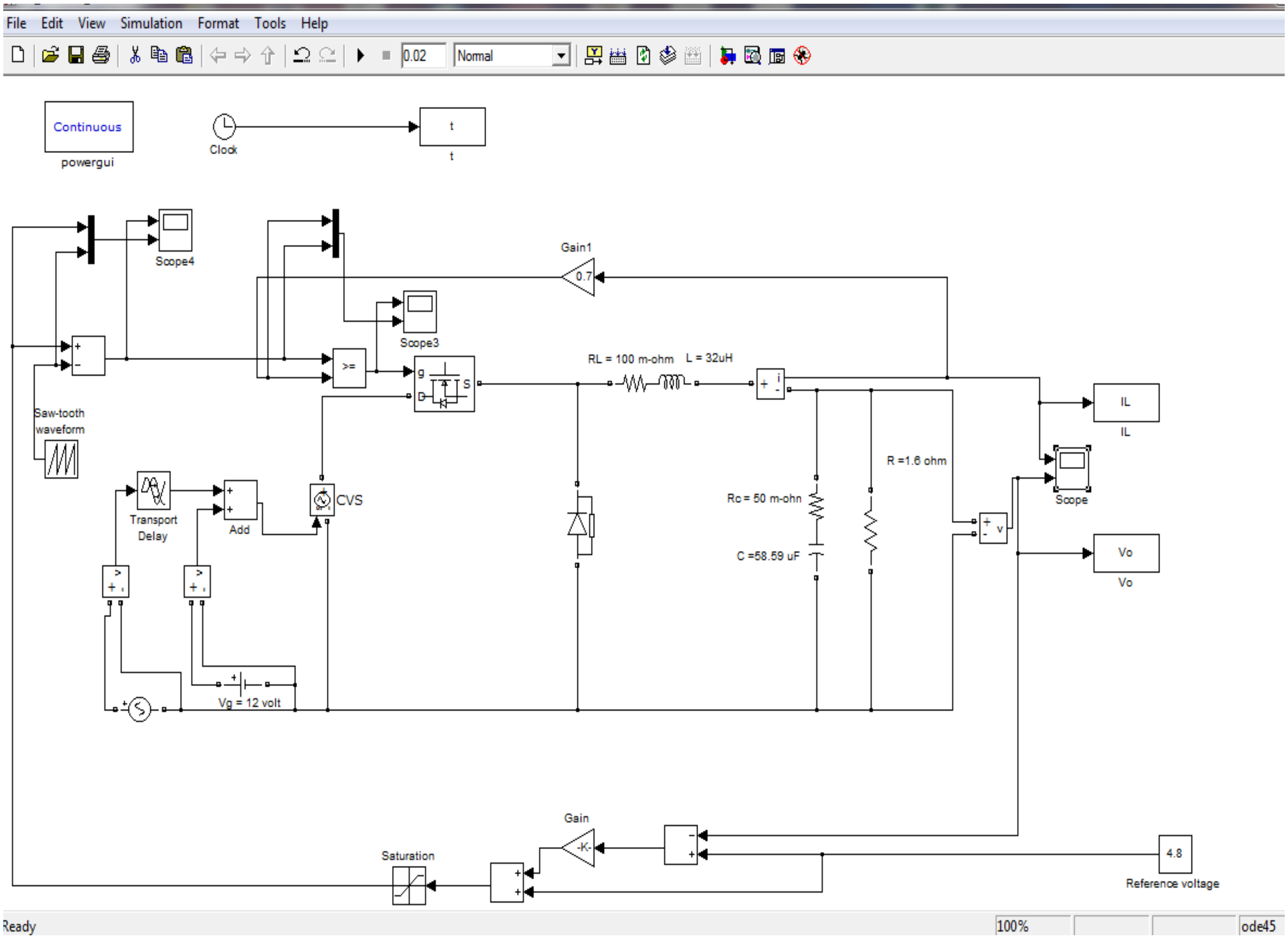

Fig 5.1

COMPARATOR OUTPUT (GATE PULSE)

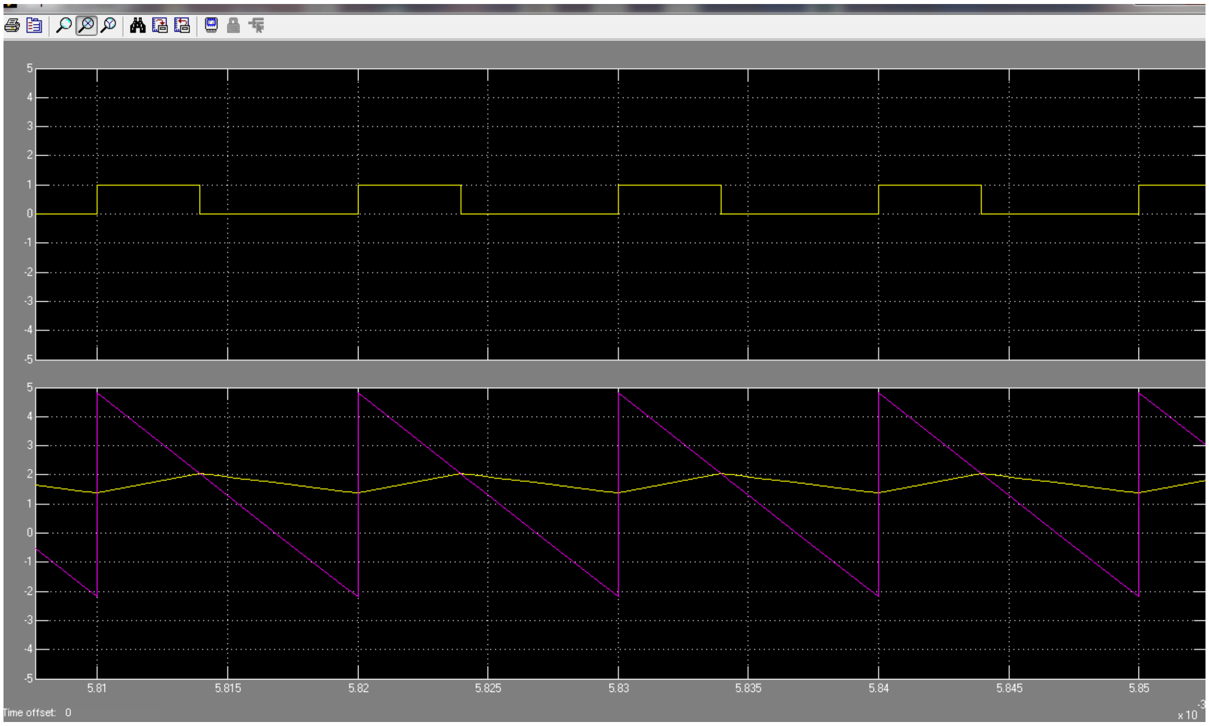

Fig 5.2

WAVEFORM OF INDUCTOR CURRENT AND OUTPUT VOLTAGE

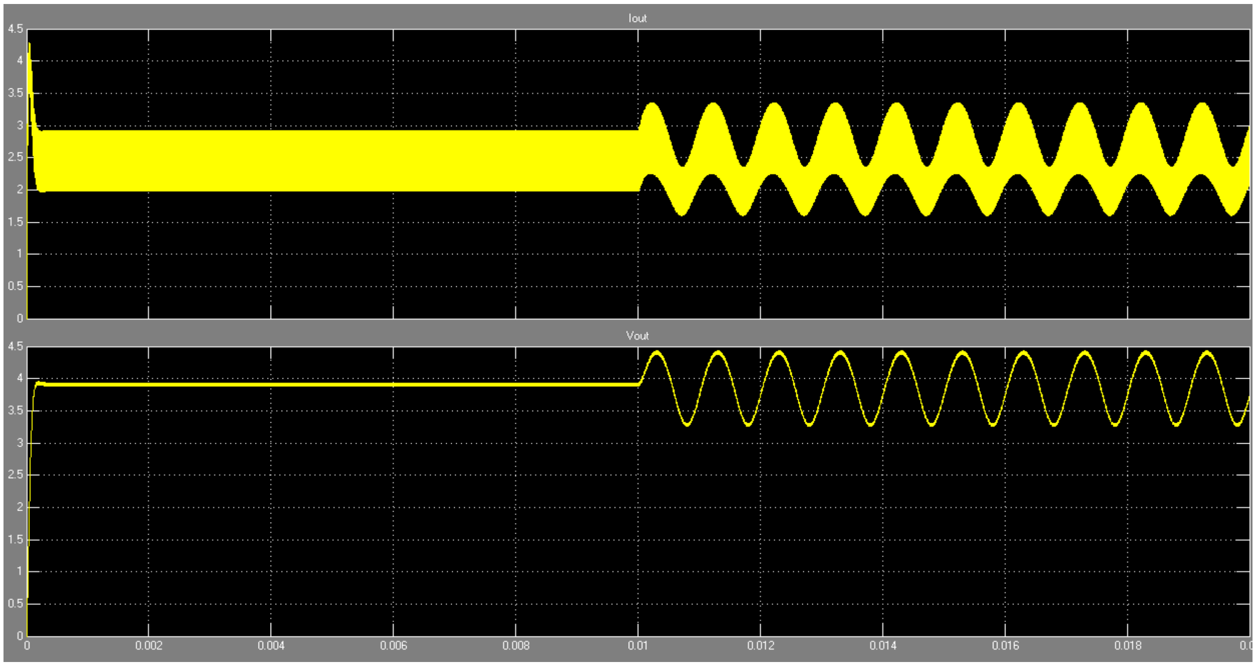

Fig 5.3

5.3 SIMULINK MODEL FOR PCM-CONTROLLED BUCK CONVERTER WITH INPUT FILTER

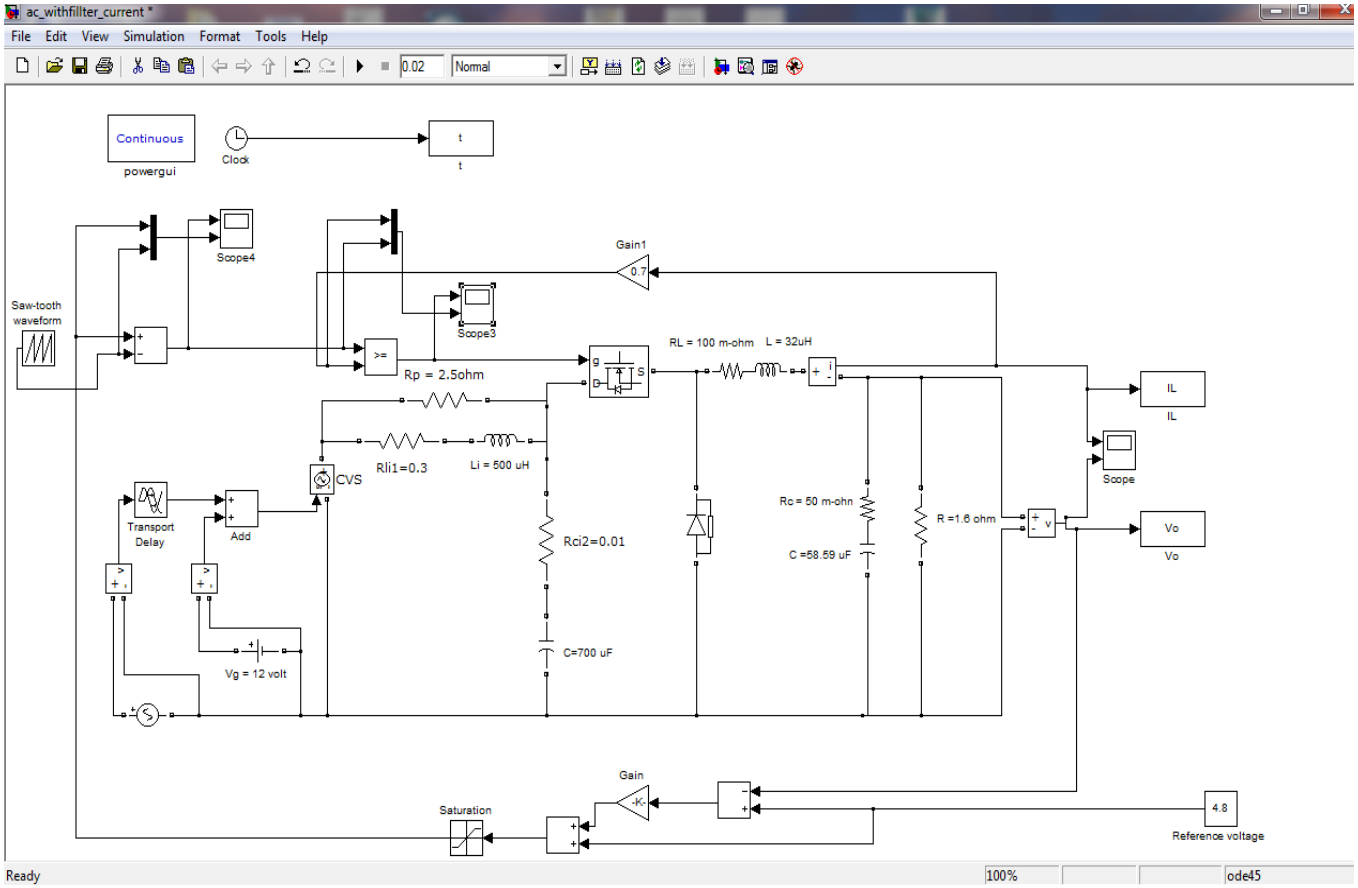

Fig 5.4

COMPARATOR OUTPUT (GATE PULSE)

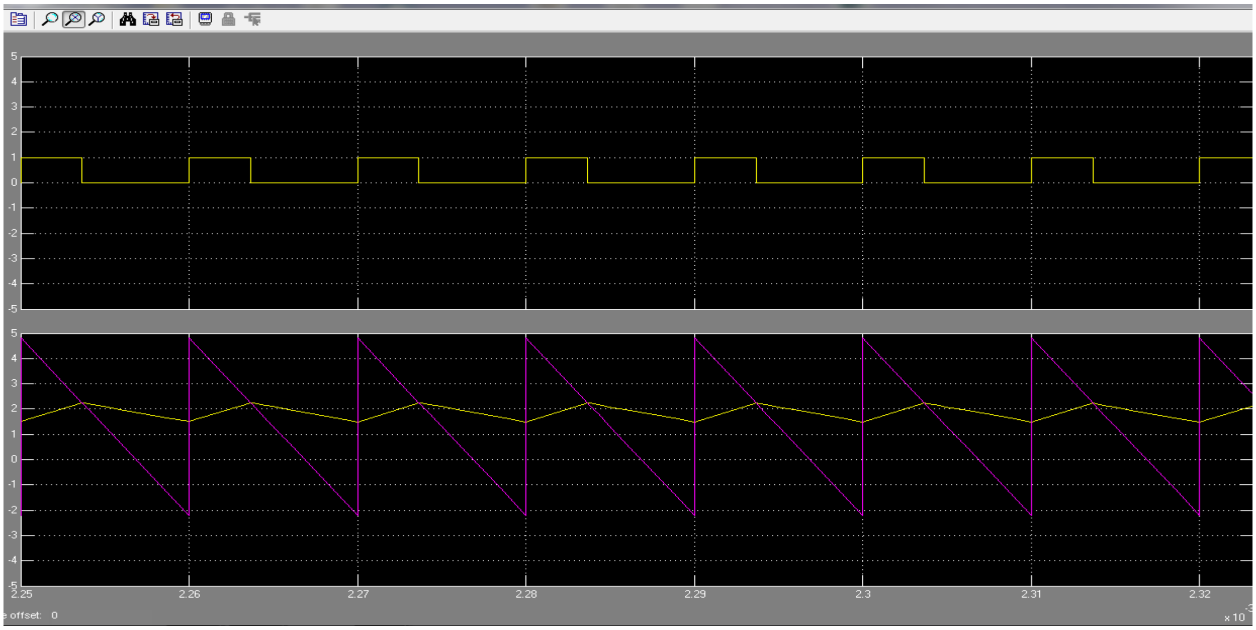

Fig 5.5

WAVEFORM OF INDUCTOR CURRENT AND OUTPUT VOLTAGE

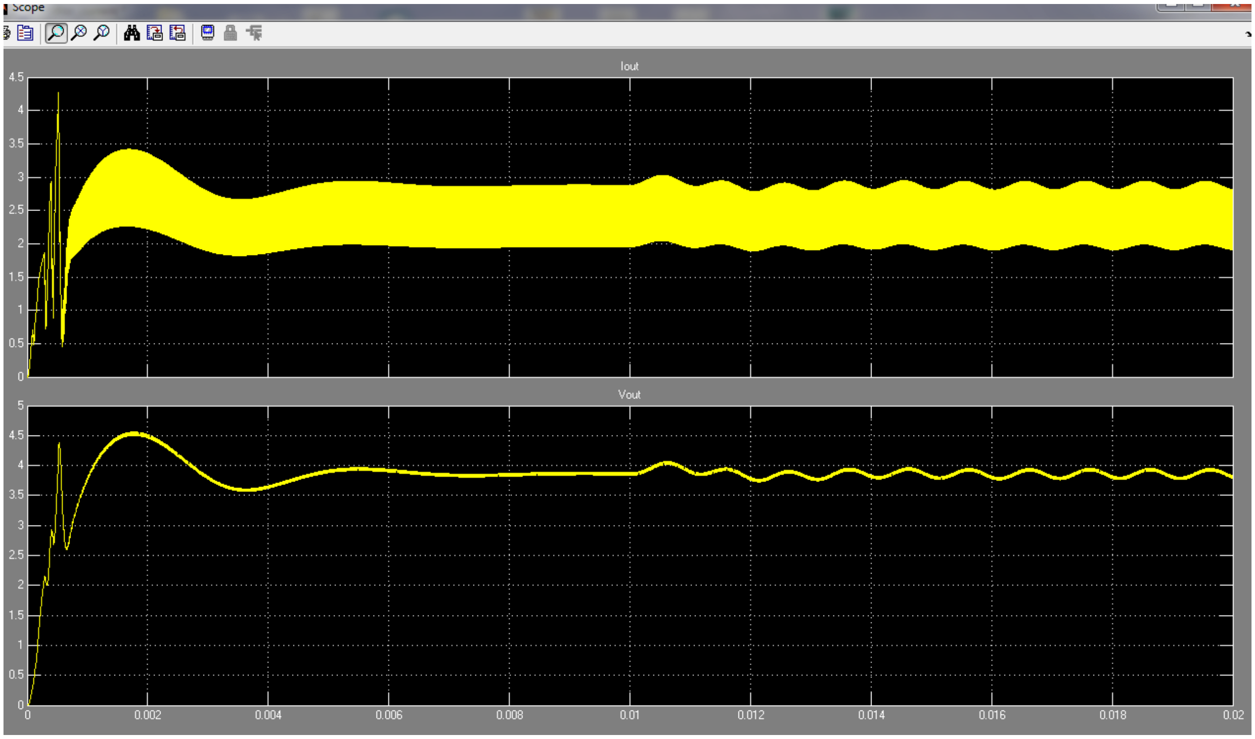

Fig 5.6

SIMULINK MODEL FOR PCM-CONTROLLED BUCK CONVERTER WITH INPUT FILTER(instability, ref to inequality (34),(35))

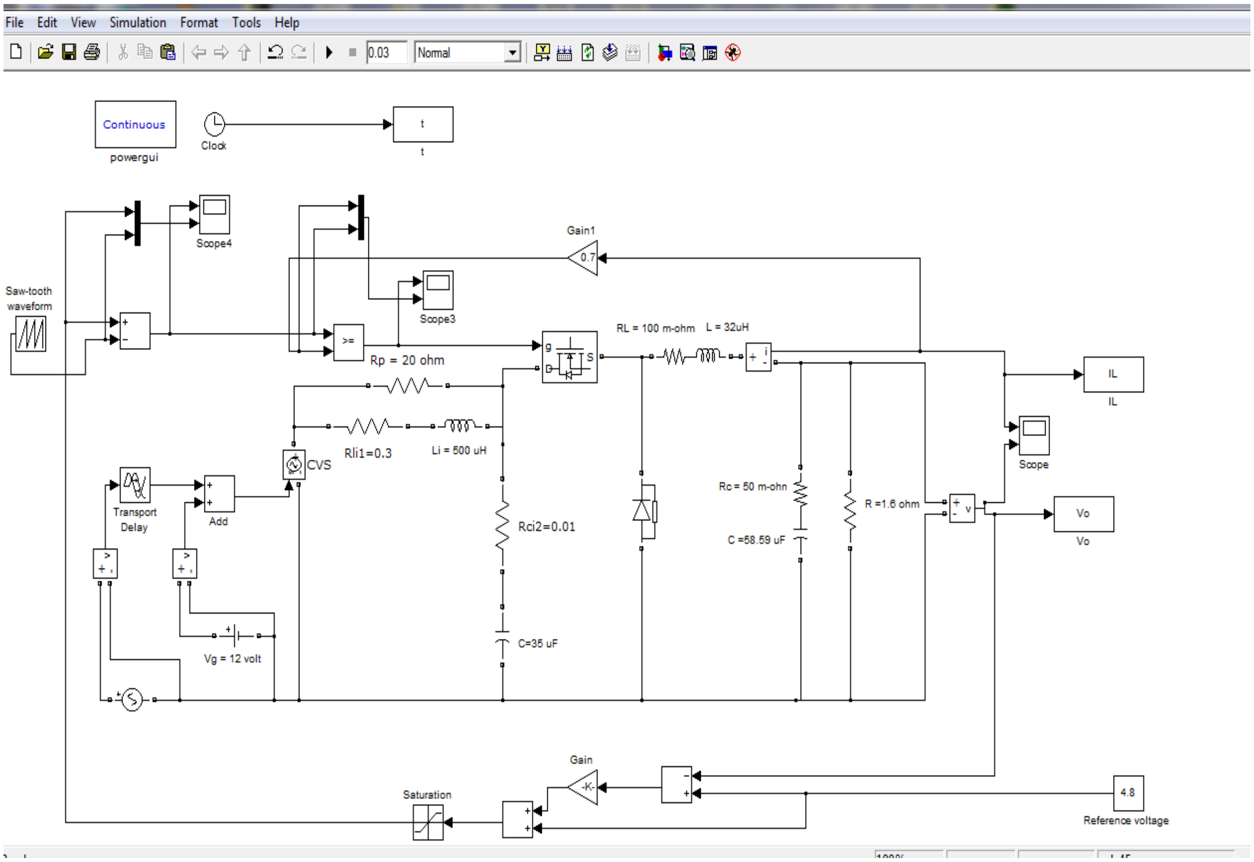

Fig 5.7

COMPARATOR OUTPUT

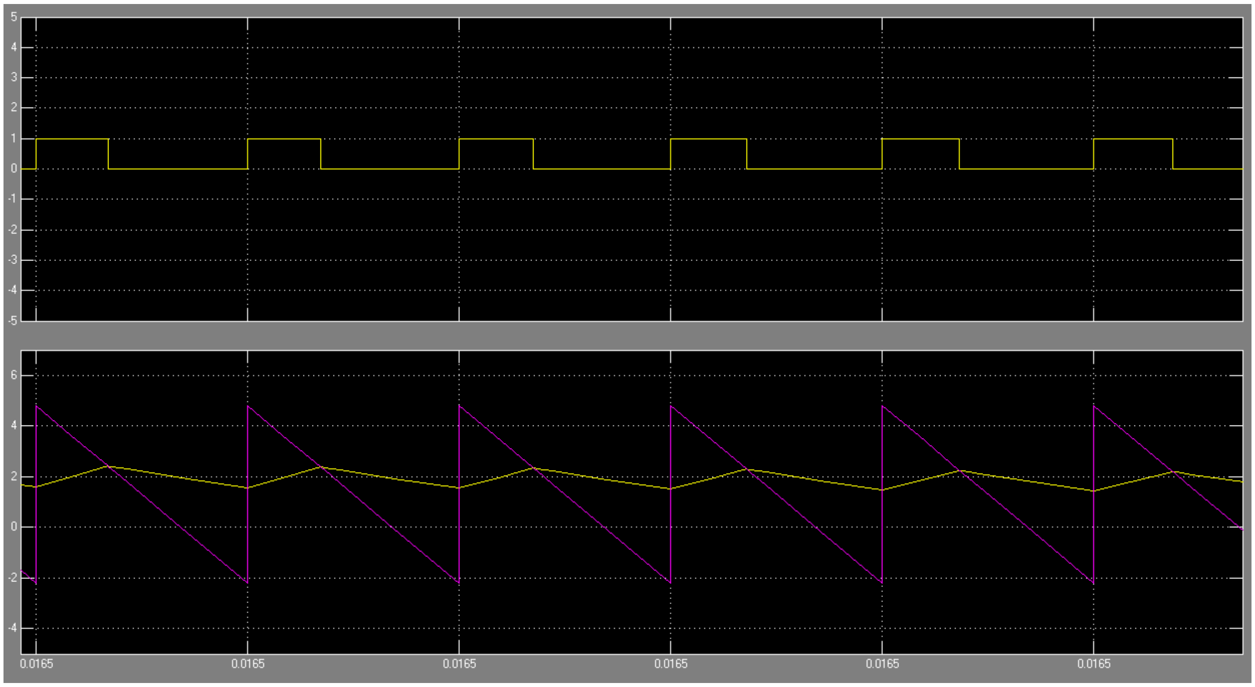

Fig 5.8

WAVEFORM OF INDUCTOR CURRENT AND OUTPUT VOLTAGE

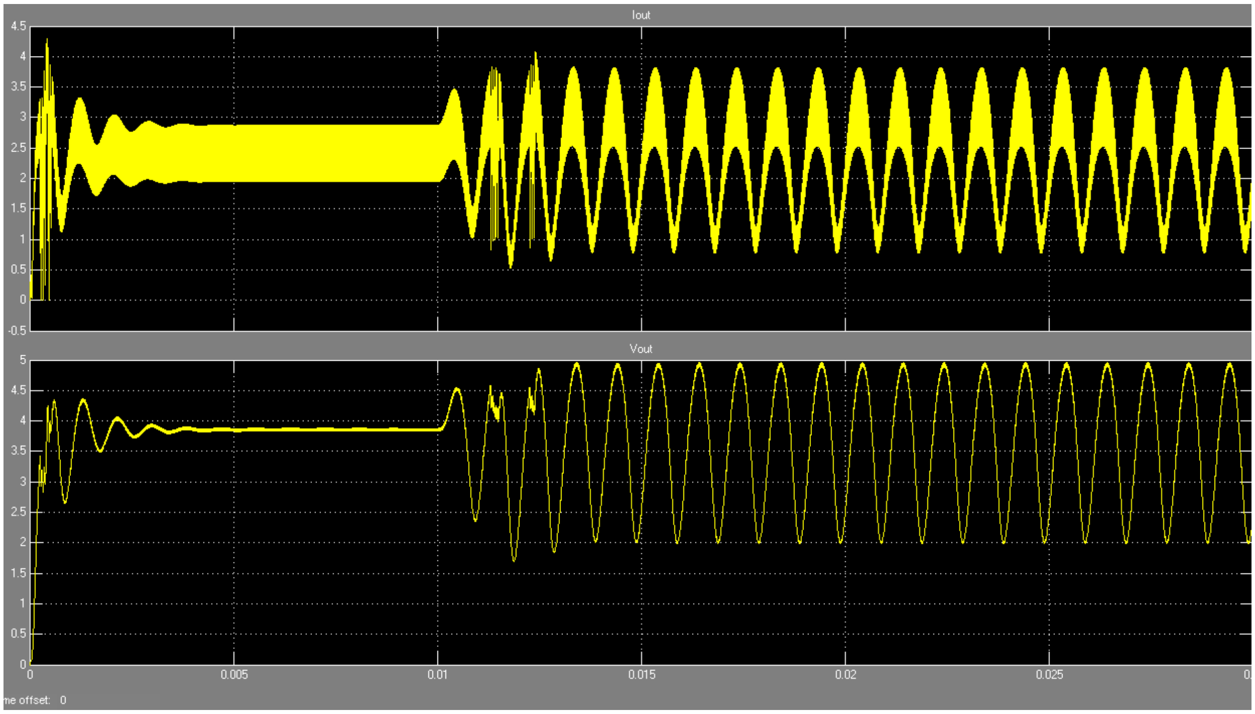

Fig 5.9

CHAPTER 6

6.1 CONCLUSION

6.2 REFERENCES

6.1 CONCLUSION

DC-DC converters are used in many applications, such as battery charger, computer and electrical drives in industry for controlling the DC voltage. However electromagnetic interference present in power signal affects the performance of DC-DC converter. So generally an input filter is added to converter to reduce the electromagnetic interference. Here effect of input filter in current controlled DC-DC buck converter is studied. The design criteria for input filter without considering k_f and k_r are derived. Output of buck converter with and without input filter is examined in stable and unstable condition of PCM controlled buck converter using MATLAB. It reduces the EMI significantly.

6.2 REFERENCES

[1] Shen-Yaur chen and Jin-Jia Chen, “study of the effect and design criteria of the input filter for buck converters with peak current-mode control using a novel system block diagram,” IEEE transactions on industrial electronics, vol.55, No.8, august 2008.

[2] R.W. Erickson and D Maksimovi**,** “Fundamentals of Power Electronics, second edition.” Kluwer Academic Publishers, 2001.

[3] Vatche Vorperian, “simplified analysis of PWM converters using model of PWM switch part I: continuous conduction mode,” IEEE transactions on aerospace and electronic systems, vol.26, no.3, may 1990.

[4] jingquan chen, robort Erickson, and dragan maksimovic**,** “IECON’01: the 27th annual conference of the IEEE industrial electronics society”2001.

[5] www.engr.colostate.edu/ECE562/98 lectures/142.pdf

[6] C. R. Kohut, “Input filter design criteria for switching regulators using Current-mode programming,” IEEE transactions on Power Electronics., vol. 7, no. 3,pp. 469–479, Jul. 1992.

[7] S. Y. Erich and W. M. Polivka, “Input filter design criteria for current programmed Regulators,” IEEE Transactions on Power Electronics, vol. 7, no. 1,pp. 781–791, Jan. 1992.

[8] B. Choi, D. Kim, D. Lee, S. Choi, and J. Sun, “Analysis of input filter Interactions in switching power converters,” IEEE Transactions on Power Electronics,vol. 22, no. 2, pp. 452–460, Mar. 2007.

[9] R. B. Ridley, a New Small-Signal Model for Current-Mode Control.Roswell, GA: Ridley Eng., Inc., 1999.

[10] R.B. Ridley, “A New Small-Signal Model for Current-Mode Control”, PhD Dissertation, Virginia Polytechnic Institute and State University, November, 1990.

[11] V. Vorpérian, “Analysis of Current-Mode Controlled PWM Converters Using the Model of the Current-Controlled PWM Switch.” Power Conversion and Intelligent Motion, October 1990.

[12] http://encon.fke.utm.my/nikd/latest/jul_01_designer.pdf

[13] www.national.com/vcm/national3/en_US/resources/power_designer/powerdesigner_106.pdf

[14] S. Wang, J. D. van Wyk, and F.C. Lee, “Effects of interactions between filter parasitic and power interconnects on EMI filter performance,” IEEE transactions on Industrial Electronics, vol.54, no.6, pp.3344-3352, Dec. 2007

[15] R. D. Middle brook, “Modeling a current-programmed buck regulator,” in Proc. IEEE Application Power Electronics, Conf., Rec., 1987, pp. 3–13.

[16] Patrick L. Chapman, Senior Member, IEEE“Numerical Dynamic Characterization of Peak Current-Mode-Controlled DC–DC Converters” IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 56, NO. 12, DECEMBER 2009.

[17]Edwin van Dijk, Herman J. N. Spruijt, Dermot M. O’Sullivan, and J. Ben Klaassens “PWM-Switch Modeling of DC-DC Converters”IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 10, NO. 6, NOVEMBER 1995