DEVELOPMENT OF EFFICIENT POWER SUPPLY FOR LOW VOLTAGE HIGH CURRENT APPLICATIONS

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DEVELOPMENT OF EFFICIENT POWER SUPPLY FOR LOW VOLTAGE HIGH CURRENT APPLICATIONS

A Thesis submitted in partial fulfillment of the requirements for the degree of

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in
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By

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CERTIFICATE

This is to certify that the thesis titled "**Development of Efficient Power Supply for Low Voltage High Current Applications**", submitted to the National Institute of Technology, Rourkela by **Mr. Aroul K.**, Roll No. **60502002** for the award of Master of Technology (Research) in Electrical Engineering, is a bona fide record of research work carried out by him under my supervision and guidance.

The candidate has fulfilled all the prescribed requirements.

The Thesis which is based on candidate's own work, has not submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a Master of Technology (Research) degree in Electrical Engineering.

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CITATIONS

- Received two citations for an IEEE research paper.

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CONTENTS

ABBREVIATIONS

VRM	- Voltage Regulator Module
VR	- Voltage Regulator
VLSI	- Very-Large-Scale Integration
ZVT	- Zero Voltage Transition
ZCT	- Zero Current Transition
ZVS	- Zero Voltage Switching
ZCS	- Zero Current Switching
SBC	- Synchronous Buck Converter
MSBC	- Multiphase Synchronous Buck Converter
QRC	- Quasi Resonant Converter
MRC	- Multi Resonant Converter
PWM	- Pulse Width Modulation
EMI	- Electromagnetic Interference
DCR	- DC Resistance

NOTATIONS

D	- Schottky Diode
S	- Main Switch/ High Side Switch
S_1	- Auxiliary Switch
S_2	- Synchronous Switch
$i_{gs,}$ $i_{gs1,}$ i_{gs2}	- Gate pulses of Main, Auxiliary and Synchronous switches
$i_{s,}$ $i_{s1}(i_{Lr),}$ i_{s2}	- Main, Auxiliary and Synchronous switch Currents
V_s, V_{s1}, V_{s2}	- Main, Auxiliary and Synchronous switch Voltages
$R_{ds\ (on)}$	- on state Resistance
V_{DS}	- Drain Source Voltage
V_{GS}	- Gate Source Voltage
I_D	- Drain Current
t_{on}	- on time delay
t_{off}	- off time delay
$t_{S\ (L-H)}$	- rising switching time
$t_{S\ (H-L)}$	- falling switching time
Q_G	- Gate Charge
Q_{GD}	- Gate Drain Charge
$Q_{G\ (SW)}$	- Switching Gate Charge
C_{GD}	- Gate drain Capacitance
C_{oss}	- Output Capacitance
C_{DS}	- Drain source Capacitance

V_{TH} - Threshold Voltage

V_{SP} - Switching Point Voltage

f_S - Switching Frequency

V_S - Source Voltage

V_0 - Output Voltage

I_0 - Output Current

L_0 - Output Inductor

C_0 - Output Capacitor

C_r - Resonant Capacitor

L_r - Resonant Inductor

I_p - Resonant Inductor's Peak Current

t_p - The time at peak resonant inductor current for each switching cycle

V_{Cr} - Resonant Capacitor Voltage

i_{L0} - Output Inductor Current

Δi_L - Output Inductor ripple Current

Δv_C - Output Capacitor ripple Voltage

P_{HS}, P_{LS} - Power loss on the high and low side MOSFET

P_{SW} - Switching Power loss

P_{COND} - Conduction Power loss

I_{driver} - Gate Driver Current

$I_{driver\ (L\text{-}H)}$ - The rising Driver Current

$I_{driver\ (H\text{-}L)}$ - The falling Driver Current

V_{DD} - Gate Drive Voltage

$R_{driver\ (pull\text{-}up)}$ - Gate Driver pull up Resistance

$R_{driver\ (pull\text{-}down)}$ - Gate driver pull down Resistance

R_{gate} - Internal Gate Driver Resistance

$P_{DR\ (L\text{-}H)}$ - Dissipation in gate driver for the rising edge

$P_{DR\ (H\text{-}L)}$ - Dissipation in the gate driver for the falling edge

P_{DRIVER} - Gate Driver Loss

d - Duty cycle

ABSTRACT

In order to meet demands for faster and more efficient data processing, modern microprocessors are being designed with lower voltage implementations. The continuous packing of more devices on a single processor chip is increasing its current demands calling for an aggressive power management. These demands, in turn require special power supplies to provide lower voltages with higher currents capabilities for microprocessors.

This work presents a modified low voltage high current Voltage Regulator Module (VRM) technology for desktop computers, and portable applications. The developed advanced VRM has advantages over conventional ones in power efficiency and reliability.

The SMPS outputs of desktop computers are mainly $\pm 5V, \pm 12V$. Considering the factor of distribution loss for today's processors +12V input supply is used instead of +5V and then it is step down to 1.2V. To make this dc/dc conversion efficient at lower voltages, synchronous converter is an obvious choice because of lower conduction loss in the diode.

Primarily the various losses occurring in Synchronous Buck Converter (SBC) is analyzed mathematically. The results conclude the dominance of the switching loss on the high side MOSFET. ZVT, the most efficient among the soft switching techniques is employed to the SBC.

The suggested Zero Voltage Transition (ZVT) Single Phase SBC is simulated using PSIM for design values of 3.3V, 12A output and switching frequency 200 kHz. The proposed converter exhibits an efficient performance in comparison with the conventional converter. Additionally, the resonant auxiliary circuit in ZVT, which conducts for a short period of time, is also devoid of the switching loss. The simulation results are then verified

experimentally by developing a prototype of the proposed converter for a switching frequency of 200 kHz.

With this satisfactory result, a ZVT MSBC (Multiphase Synchronous Buck Converter) is designed for 1.2V, 90A output switching at 500 kHz. The simulated results present a much better performance than the conventional MSBC. ZVT Techniques are only employed mostly for high power converters. A very few work in the literatures has applied them in the low powers. The increase in the efficiency of low power circuits (such as SBC) by applying ZVT technique is realized in this dissertation.

KEYWORDS – dc/dc converter, Synchronous Buck Converter, Voltage Regulator Module, Zero Voltage Transition, Multiphase Synchronous Buck Converter, PSIM, Switching Loss, Microprocessor, Desktop Computers, Portable Applications.

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INTRODUCTION

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Dissertation Outline

The portable products, desktop computers, laptops need the use of SBCs for delivering efficient power to the microprocessors. It demands a high current and low voltage input for its various objectives. This work provides a solution to design an efficient power supply for the computer microprocessors. This design concept can be applied for the portable products also.

1.1 Research Background

Complying with Moore's Law, which states that "transistor density of integrated circuits doubles every eighteen months," the transistors per die in the microprocessors have been steadily increasing in the past decades, as shown in fig.1.1 [1]. The more the transistors are integrated into a single die, the more functions that die can perform [2]. It is predicted that in 2015, there will be tens of billions of transistors in a single chip [3].

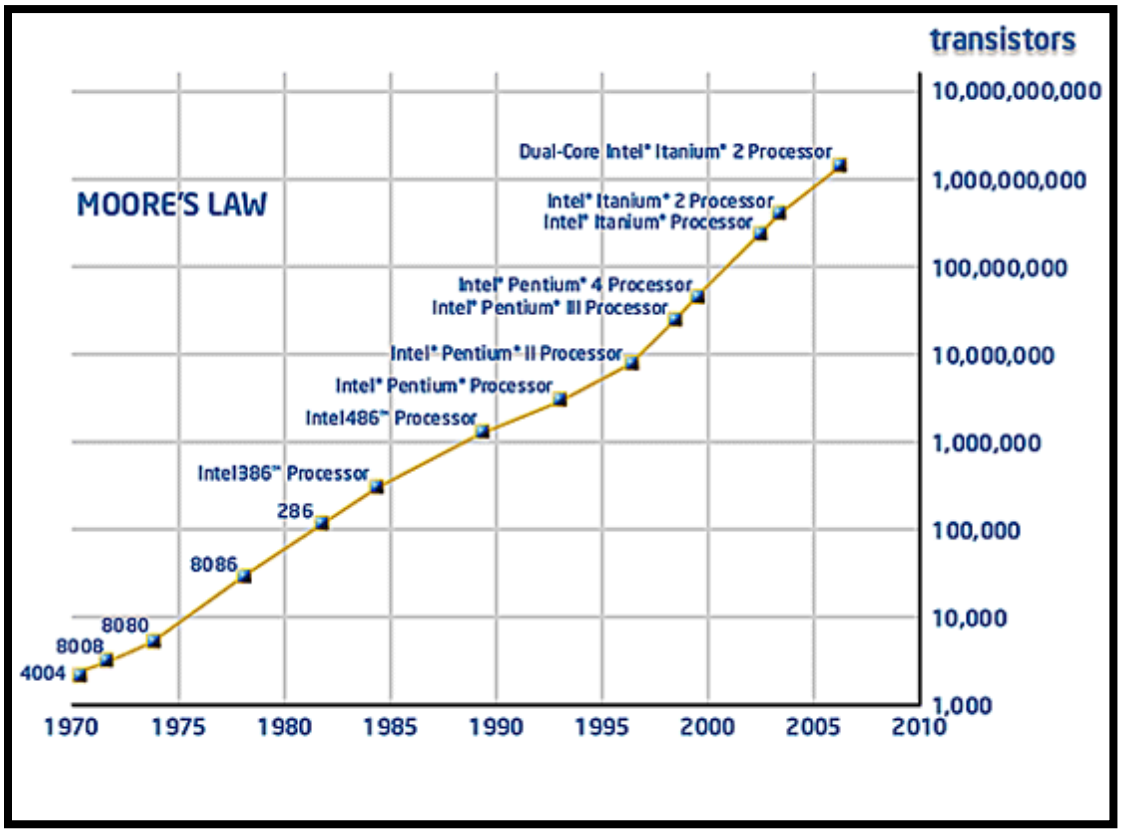

Fig.1.1. Intel's roadmap of the number of integrated transistors in one processor

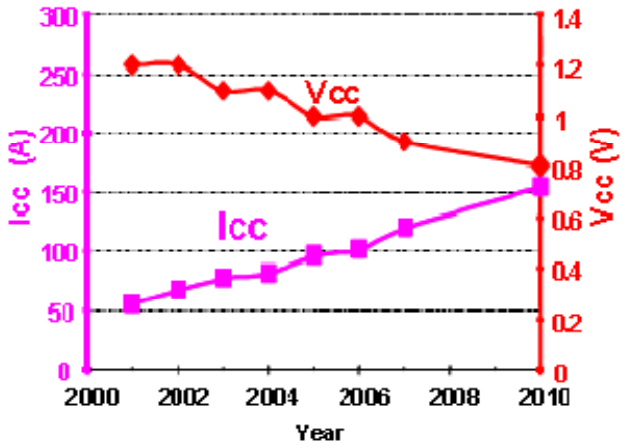

Fig.1.2. Microprocessors voltage and current roadmap

The increasing number of transistors in the microprocessors results in continuous increase of the microprocessor Current demands and hence, the power consumption. In order to reduce the power consumption of the microprocessors, the supply voltages have been decreased as shown in fig.1.2. Moreover, due to the high frequencies, the microprocessors load transition speeds also increase. The low voltage, high current and fast load transition speeds are the challenges imposed on microprocessors power supplies [4].

For a 386 or 486 processor, a traditional centralized power supply (silver box) is sufficient to deliver all the power needed. The silver box also supports power to the memory chip, video card and other parts in the computer. When the Pentium processors emerged in the late 1990s, the centralized power systems no longer met their power requirements. Because of the microprocessors low voltage and high current demands, the parasitic resistors and inductors of the connections between the centralized silver boxes and the microprocessors had a severe, negative impact on power quality. It was no longer practical for the bulky silver box to provide energy directly to the microprocessor. To power the microprocessors of computer systems with dedicated converters, VRs, was then used. The point-of-load regulation system was used to deliver a highly accurate supply voltage to the

microprocessor, where a dedicated dc/dc converter, the VR, was placed in close proximity to the microprocessor in order to minimize the parasitic impedance between the VRM and the microprocessor. In the beginning, a 5V was used as the input of the VRM. As the power consumption of the microprocessor increased, the distribution loss of the 5V bus also dramatically increased. The input voltage from the silver box is now 12V and the supply voltage to the processors have been and will continuously be decreasing [5] - [7].

1.2 Converter Topology for VR

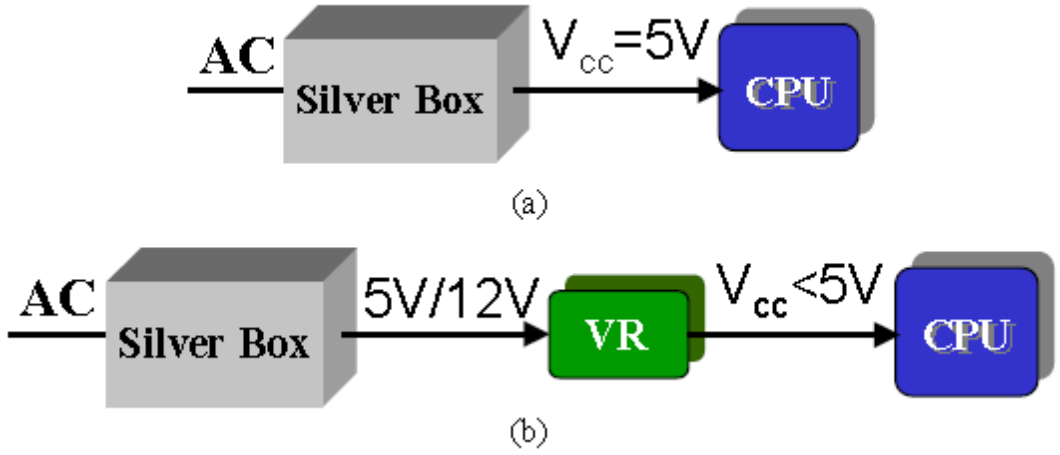

Fig.1.3. Power delivery structures: (a) The initial power delivery architecture for CPUs (b) Current power delivery structure for CPUs

The simplest known dc/dc step down converter is the buck topology. Designing buck converters for low voltages typically 5V and under provides a number of challenges. The main disadvantage is the significant power loss during the diode/Schottky diode D conduction period, which is the product of the forward voltage drop and its current [8].

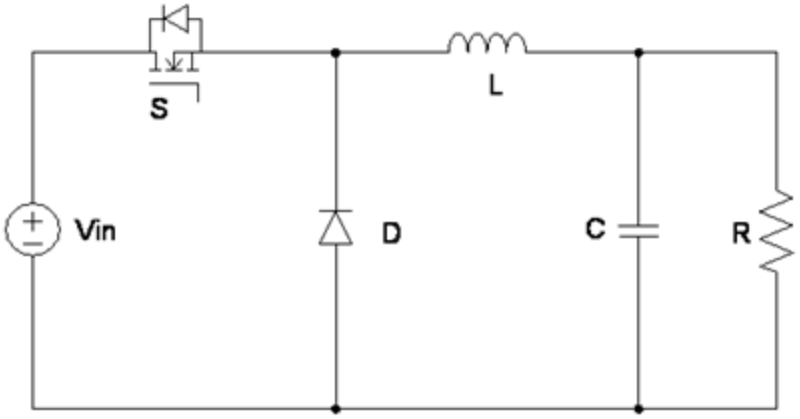

Fig.1.4. Conventional Buck Converter

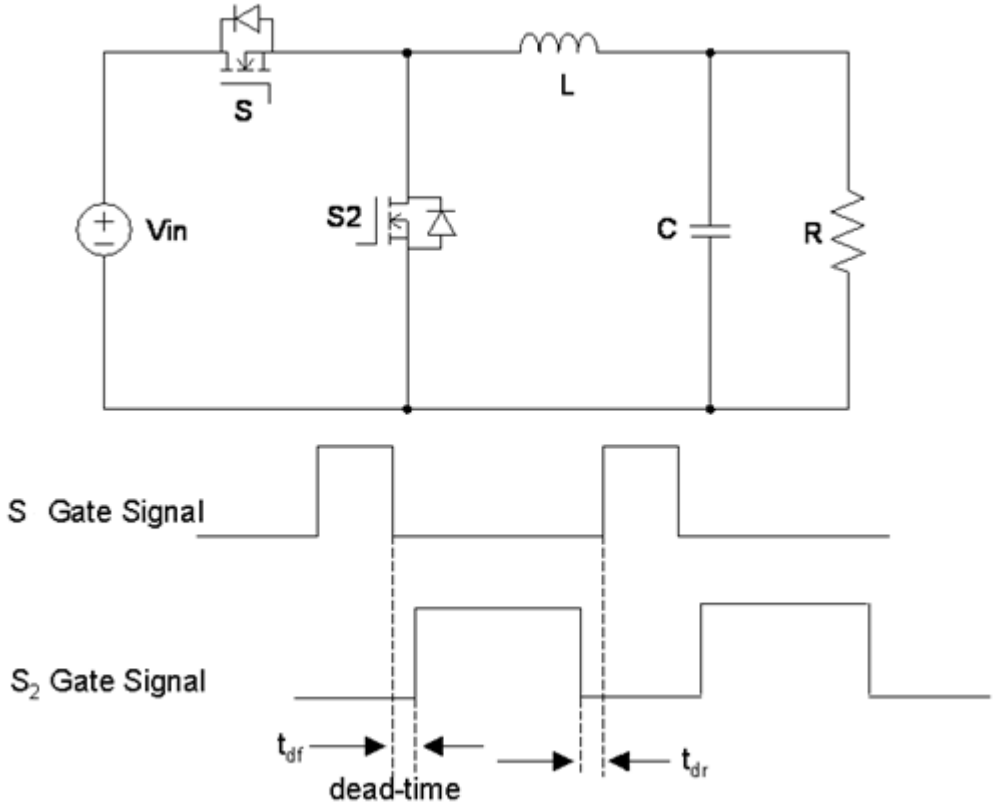

Fig.1.5. SBC and Gate Signal Waveforms

As shown in fig.1.4, by replacing D with S_2, the conventional buck is converted to synchronous buck topology. The ideal gate signal waveforms of S and S_2 are also shown in fig.1.5. The dead times between S and S_2 are used to prevent the shoot through [9], [10]. During the dead time, the inductor current continues flowing through internal body diode of S_2. When the gate signal of S_2 is high, the inductor current flows through S_2. Synchronous buck topology provides better efficiency than standard buck converter because the on-resistance $R_{ds(on)}$ of S_2 is in the milliohm range during S_2 on time interval [8].

The synchronous buck circuit is in widespread use to provide high current, low voltage power for CPU's, chipsets, peripherals etc. Typically used to convert from a 12V or 5V supply, they provide outputs as low as 1.2V for low voltage CPUs made in sub micron technologies [4].

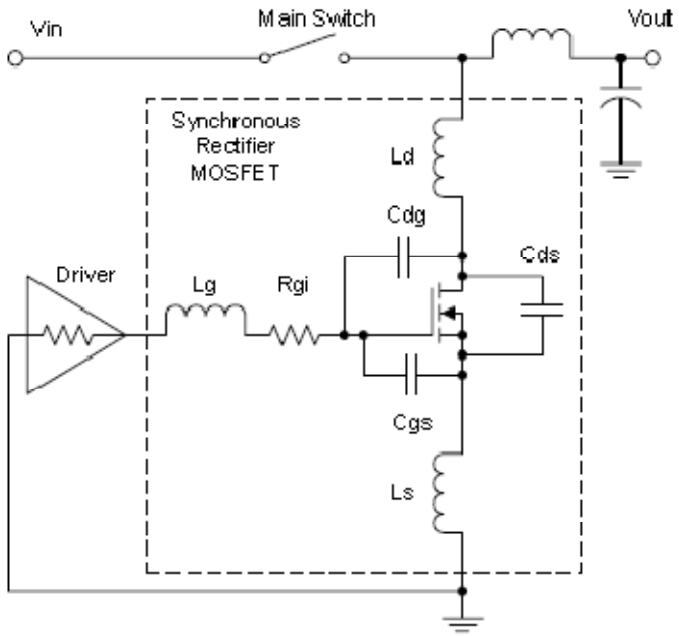

Fig.1.6. Synchronous Rectifier Parasitic Components

As shown in fig.1.6, high dv/dt on the low side switch node when it is turned off can raise the voltage on its gate through capacitive coupling from the drain-to-gate to the point and the switch is momentarily turned ON causing a shoot through [11], [12]. Many resonant drivers were proposed to provide lossless gate drives [13]-[15] and the control techniques [16]-[19] were proposed to improve the slew rates of the microprocessor loads.

As microprocessor power consumption increases, a single phase SBC can no longer deliver the required current. Handling the high current in a single phase converter would place high thermal demands on the components in the system such as the inductors and MOSFETs (metal-oxide semiconductor field-effect transistors). Therefore the VR topology adopts the MSBC.

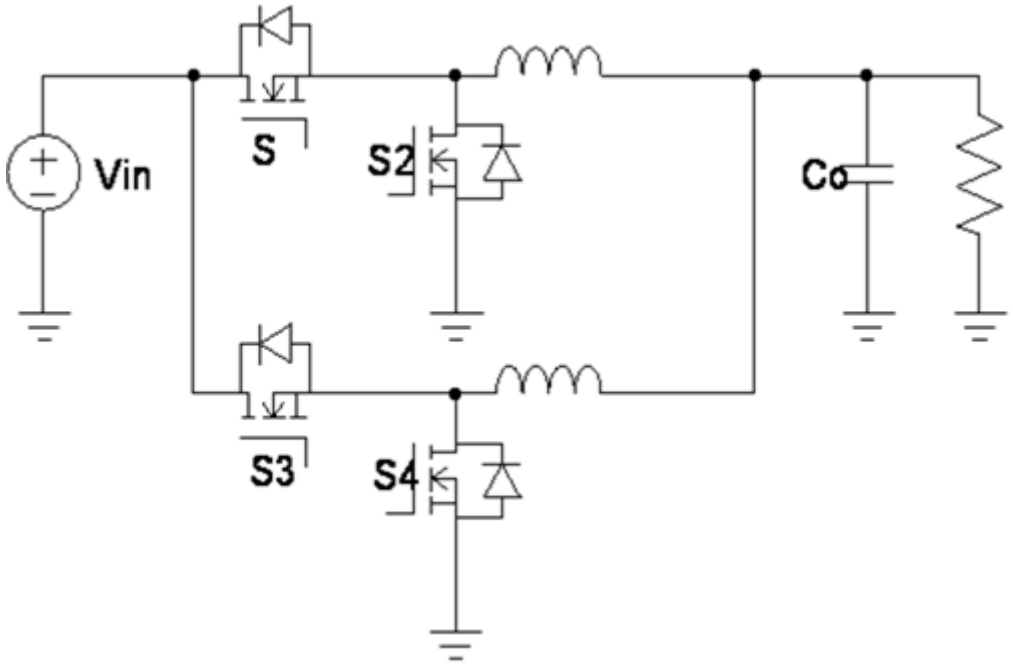

Fig.1.7. Two Phase MSBC

Multiphase operation is important for producing the high currents and low voltages demanded by today's CPUs, as it reduces current ripple by interleaving phases and provides better thermal management due to the distributed structure [20] – [22].

1.3 Switching Loss

In SBCs, switching of semiconductor devices normally occurs at high current levels. Therefore, when switching at high frequencies these converters are associated with high power dissipation in their switching devices. Also, the higher input and lower output voltages bring about very low duty cycles. Hence, the high side MOSFET S/S_3 should turn on and off in a very short period of time, which also brings switching losses into picture [23], [24]. The losses due to switching produce three considerable effects [25] on the converters in general,

1. Achievable f_S and efficiency limited
2. EMI at high frequencies due to high di/dt, dv/dt and induces noise
3. Switching locus may sometimes exceed safe operating area

Switching loss of a MOSFET can be represented mathematically as,

$$P_{SW} = \frac{V_{DS}.I_D.f_S}{2}(t_{on} + t_{off}) \qquad 1.1$$

From equation (1.1) some important result can be deduced that switching losses can be reduced by two methods:

(i) By reducing the turn-on and turn-off delay times. This is done by using faster and more efficient switches in the converter.

(ii) By making the current or voltage across the switch zero before turning it on or off. Soft switching resonant converters are based on this concept.

Also it is inferred from the equation that the switching loss in any semiconductor switch varies linearly with f_S and the delay times [26], [27].

Hard switching is the predominant loss mechanism in the high side MOSFET followed by the conduction losses of the low side MOSFET [28], [29]. Some 60% to 70% of the total losses are in the MOSFET for a 60W power converter (Step – Down). Thus, more efficient power MOSFETs is needed that offer both reduced conduction and switching losses at higher frequencies [30]. The switching losses at higher frequencies can be eliminated by the soft switching techniques available.

1.4 Solution

There are mainly two techniques to eliminate the switching losses namely ZVS and ZCS. QRCs were introduced to overcome the disadvantages of conventional PWM converters operating at high switching frequency by achieving ZVS for the active switch and ZCS for the rectifier diode [31]-[34]. ZVS MRCs technique utilizes all major parasitic of the power stages and all semiconductor devices in MRC operate with ZVS, which substantially reduces the switching losses and noise [35].

In both techniques, the switching losses in the semiconductor devices are eliminated due to the fact that current through or voltage across the switching device at switching point is equal to or near zero. This reduction in the switching loss allows the designer to attain a higher operating frequency without sacrificing converter efficiency. By doing so, the resonant converters show promise of achieving what could not be achieved by the PWM converter that is the design of small size and weight converters. Currently, resonant power converters operating in the range of a few megahertz are available. Another advantage of resonant converters over PWM converters is the decrease of harmonic content in the converter voltage and current waveforms. Therefore, when the resonant and PWM converters

are operated at the same power level and frequency, it is expected that the resonant converter will have lower harmonic emission [36].

The Resonant converters operate with sinusoidal current through the power switches which results in high peak and RMS currents for the power transistors and high voltage stresses on the rectifier diodes. Furthermore, when the line voltage or load current varies over a wide range, QRCs are modulated with a wide switching frequency range, making the circuit design difficult to optimize [37]. As a compromise between the PWM and resonant techniques, various soft switching PWM converter techniques has been proposed to aim at combining desirable features of both the conventional PWM and Quasi Resonant techniques without a significant increase in circulating energy.

1.5 ZVT and ZCT

Such a solution has been achieved by ZVT and ZCT. The choice between the two depends on the semiconductor device technology that will be used. In the case of majority carrier semiconductors, the best choice would be ZVS, where the capacitive turn-on losses can be eliminated. On the other hand, in the case of minority carrier semiconductors, the ZCS technique can avoid the turn off losses caused by the current tail [38].

The voltage-mode soft-switching method that has attracted most interest in recent years is the ZVT. This is because of its low additional conduction losses and because its operation is closest to the PWM converters. Instead of using a series resonant network across the power switch, an alternative way is to use a shunt resonant network across the power switch. The auxiliary circuit of the ZVT converters is activated just before the main switch is turned on and ceases after it is accomplished. The auxiliary circuit components in this circuit have lower ratings than those in the main power circuit because the auxiliary circuit is active

for only a fraction of the switching cycle. A partial resonance is created by the shunt resonant network to achieve ZCS or ZVS during the switching transition. And it will still keep the advantages of a PWM converter because after the switching transition is over, the circuit reverts back to PWM operation mode [39 -42].

Previously proposed ZVT-PWM converters have at least one of the following key drawbacks.

1. The auxiliary switch is turned off while it is conducting current. This causes switching losses and EMI to appear that offsets the benefits of the using the auxiliary circuit. In converters such as the ones proposed in [43], [44] the turn off is very hard.
2. The auxiliary circuit components have high voltage and/or current stresses. Such as converters proposed in [45], [46]. The converter proposed in [42] reduces the current stress on the main switch, but circuit is very complex.

Reducing switching losses for High side MOSFETs operating at low powers is not clearly dealt in literatures. Hence, this work presents a new class of ZVT SBC. By using a simple resonant auxiliary network in parallel with the main switch, the proposed converters achieve ZVS for the main switch and synchronous switch, ZCS for the auxiliary switch.

1.6 Dissertation Outline

This chapter has discussed the problems occurring in SBC and has given an outline solution to its switching loss. Chapter 2 analysis the various losses occurring in SBC mathematically and validates the domination of switching loss on the high side switch. Chapter 3 introduces the new ZVT SBC and analysis its various modes of operation, thereby

designing its various parameters for experimentation. Chapter 4 discusses the results on the designed converter verifying its superior performance over the conventional one by both simulation and experimental work. Chapter 5 introduces the ZVT MSBC and presents its simulation results, where it is shown to be much more efficient than the existing MSBC. Chapter 6 presents a summary of the dissertation and points out the limitation in ZVT MSBC proposing the future work.

Chapter 2

LOSS ANALYSIS

The High Side Losses

The Low Side Losses

The Gate Driver Loss

Conclusion

As this work concentrates on reducing switching losses in Synchronous Buck Converters (SBCs), it is essential to elucidate briefly on this loss. It was concluded from literatures in the previous chapter that the high side switching loss is highly dominant compared to the low side switching loss. In this chapter the need for eliminating the high side switching loss is validated by mathematical analysis.

A SBC having the following values is considered for the analysis:-

V_S = 12V

V_0 = 3.3V

I_0 =12A

f_S = 200 kHz

S_1 and S_2 =IRF1312. It has $R_{ds\,(on)}$ of 10 mΩ.

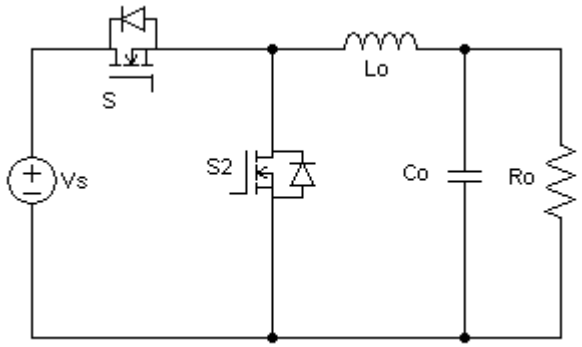

Fig.2.1. Synchronous Buck Converter

2.1 The High Side Losses

The power loss in any MOSFET is the combination of the MOSFET's switching loss and the conduction loss.

$$P_{HS} = P_{SW} + P_{COND} \qquad 2.1$$

2.1.1 Conduction Loss

Calculating high side conduction loss is straightforward as the conduction losses are just the I^2R losses in the MOSFET times the MOSFET's duty cycle:

$$P_{COND} = {I_0}^2 . R_{ds(on)} . \frac{V_0}{V_S} \qquad 2.2$$

$$P_{COND} = 12A^2 . 10m\Omega . \frac{3.3V}{12V} = 0.396W$$

2.1.2 Switching Loss

The switching time is broken up into 5 periods (t_1-t_5) as illustrated in fig. 2.2. The top drawing in fig.2.2 shows the voltage across the MOSFET and the current through it. The bottom timing graph represents V_{GS} as a function of time. The shape of this graph is identical to the shape of the Q_G curve contained in the datasheets, shown in fig.2.3, which assumes the gate is being driven with a constant current. The Q_G notations in fig.2.2 indicate which Q_G is being charged during the corresponding time period.

The switching interval begins when the high-side MOSFET driver turns on and begins to supply current to S's gate to charge its input capacitance. There are no switching losses until V_{GS} reaches the MOSFET's V_{TH}, therefore the power loss during the time period t_1 (Pt_1) = 0. When V_{GS} reaches V_{TH}, the input capacitance is being charged and I_D is rising linearly until it reaches the current in L_0 which is presumed to be I_0. During the period t_2 the MOSFET is sustaining the entire input voltage across it, therefore, the energy in the MOSFET during t_2 is:

$$E_{t_2} = t_2 . \left(\frac{V_S . I_0}{2} \right) \qquad 2.3$$

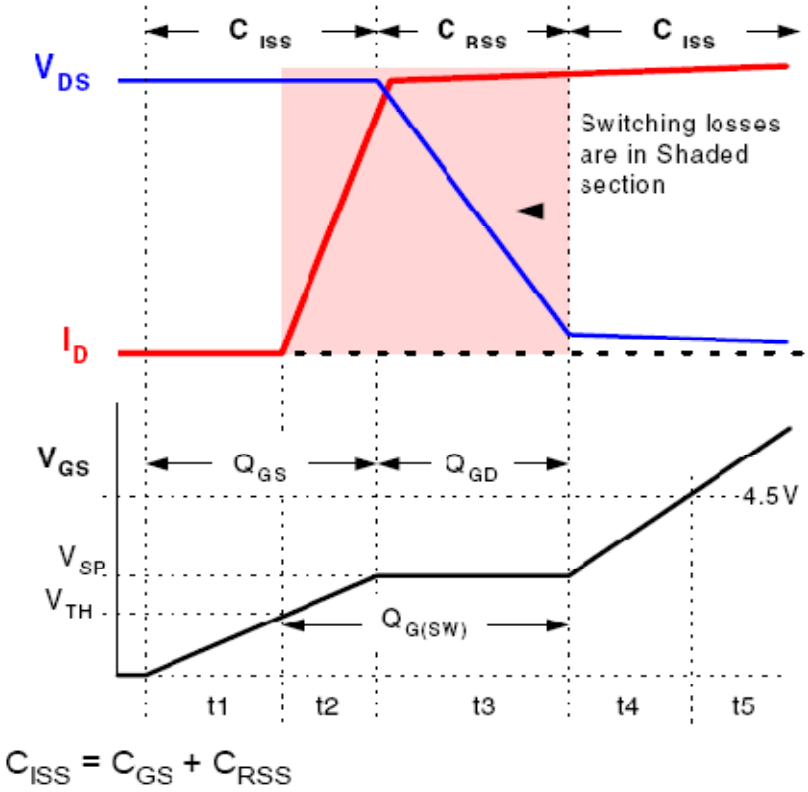

Fig.2.2. High Side Switching Losses and Q_G

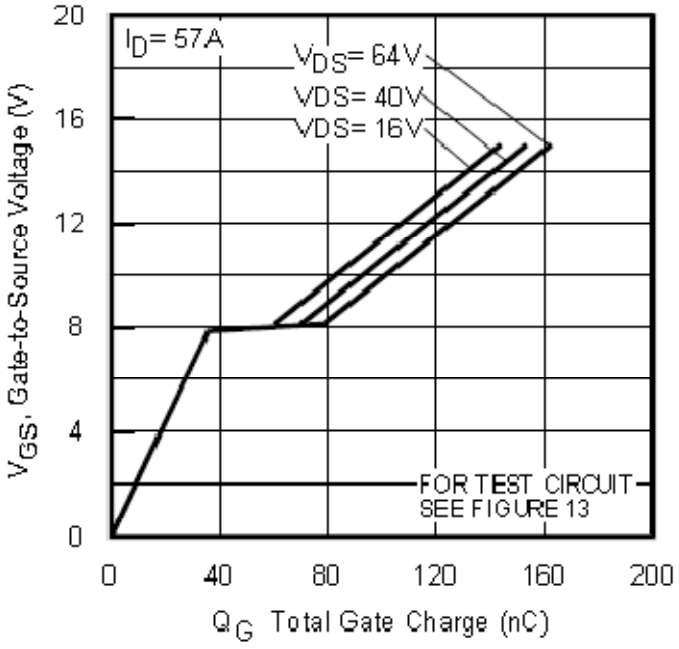

Fig.2.3. Gate Charge vs. Gate Source Voltage of IRF1312

During the period t_3, I_0 is flowing through S, and V_{DS} begins to fall. The entire gate current starts to recharge C_{GD}. During this time the current is constant at I_0 and the voltage is falling fairly linearly from V_S to zero, therefore:

$$E_{t_3} = t_3.\left(\frac{V_S.I_0}{2}\right) \qquad 2.4$$

During t_4 and t_5, the MOSFET is just fully enhancing the channel to obtain its rated $R_{ds\,(on)}$ at a rated V_{GS}. The losses during this time are very small compared to t_2 and t_3, when the MOSFET is simultaneously sustaining voltage and conducting current, so it can be safely ignored in the analysis. The switching loss for any given edge is just the power that occurs in each switching interval, multiplied by the duty cycle of the switching interval:

$$P_{SW} = \left(\frac{V_S.I_0}{2}\right).(t_2 + t_3).(f_S) \qquad 2.5$$

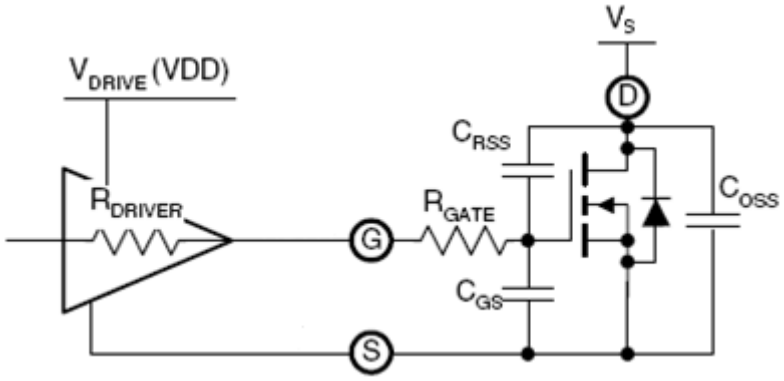

Fig.2.4. Drive Equivalent Circuit

Each period, t_2 and t_3 is determined by how long it takes the gate driver to deliver all of the charge required to move through a time period,

$$t_x = \frac{Q_{G(x)}}{I_{driver}} \qquad 2.6$$

Most of the switching interval is spent in t_3, which occurs at a voltage V_{SP}. This is not specified in most MOSFET datasheets, which can be read from the gate charge graph. Gate

charge values only vary slightly with drain current and drain-source voltage. Hence V_{SP} read from fig.2.3 is 8V.

The following values for the gate driver circuit are assumed for the analysis:

V_{DD} = 10V

$R_{driver\ (pull\text{-}up)}$ = 5Ω

$R_{driver\ (pull\text{-}down)}$ = 2Ω

R_{gate} = 1.5Ω

With V_{SP} known, the gate current can be determined by Ohm's law on the circuit in fig.2.3.

$$I_{driver(L-H)} = \frac{V_{DD}-V_{SP}}{R_{driver(pull-up)}+R_{gate}} \qquad 2.7$$

$$I_{driver(L-H)} = \frac{10V-8V}{5\Omega+1.5\Omega} = 0.31A$$

$$I_{driver(H-L)} = \frac{V_{SP}}{R_{driver(pull-down)}+R_{gate}} \qquad 2.8$$

$$I_{driver(H-L)} = \frac{8V}{2\Omega+1.5\Omega} = 2.28A$$

The rising time (L-H) and falling times (H-L) are treated separately, since I_{driver} can be different for each edge. The V_{GS} excursion during t_2 is from V_{TH} to V_{SP}. Approximating this as V_{SP} simplifies the calculation considerably and introduces no significant error. This approximation also allows to use the $Q_{G(SW)}$ term to represent the gate charge for a MOSFET to move through the switching interval.

$$Q_{G(SW)} \approx Q_{GD} + \frac{Q_{GS}}{2} \qquad 2.9$$

Taking the values of Q_{GD} and Q_{GS} from IRF1312 datasheet,

$$Q_{G(SW)} \approx 35nC$$

So, the switching times therefore are:

$$t_{S(L-H)} = \frac{Q_{G(SW)}}{I_{driver(L-H)}} \qquad 2.10$$

$$t_{S(L-H)} = \frac{35nC}{0.31A} = 112.9ns$$

$$t_{S(H-L)} = \frac{Q_{G(SW)}}{I_{driver(H-L)}} \qquad 2.11$$

$$t_{S(H-L)} = \frac{35nC}{2.28A} = 15.35ns$$

The switching loss discussion above can be summarized as:

$$P_{SW} = \left(\frac{V_{in}.I_0}{2}\right).(f_S).(t_{S(L-H)} + t_{S(H-L)}) \qquad 2.12$$

$$P_{SW} = \left(\frac{12V.12A}{2}\right).(200kHz).(112.9ns + 15.35ns) = 1.847W$$

2.2 The Low Side Losses

The Low side Loss (P_{LS}) also comprises of conduction and switching loss.

$$P_{LS} = P_{SW} + P_{COND} \qquad 2.13$$

2.2.1 Conduction Loss

$$P_{COND} = {I_0}^2.R_{ds(on)}.(1 - \frac{V_O}{V_S}) \qquad 2.14$$

$$P_{COND} = 12^2.10m\Omega.\left(1 - \frac{3.3V}{12V}\right) = 1.044W$$

2.2.2 Switching Loss

Since the switch S_2 turns on and off with only a diode drop across it, switching loss of the low side MOSFET is negligible.

2.3 The Gate Driver Loss

The power to charge the gate:

$$P_{GATE} = (Q_G).(f_S).(V_{DD}) \quad 2.15$$

Taking the value of Q_G from datasheet

$$P_{GATE} = (140nC).(500kHz).(10V) = 0.7W$$

P_{GATE} is the power from the V_{DD} supply required to drive a MOSFET gate. It is independent of the driver's output resistance and includes both the rising and falling edges. It is distributed between R_{driver}, R_{gate} proportional to their resistances.

Dissipation in the driver for the rising edge is:

$$P_{DR(L-H)} = \frac{P_{gate}.R_{driver(pull-up)}}{2(R_{total})} \quad 2.16$$

Where,

$$R_{total} = R_{driver} + R_{gate}$$

$$P_{DR(L-H)} = \frac{0.7W.5\Omega}{2(6.5)} = 0.27W \quad 2.17$$

Similarly, dissipation in the driver for the falling edge is:

$$P_{DR(H-L)} = \frac{P_{gate}.R_{driver(pull-down)}}{2(R_{total})} \quad 2.18$$

$$P_{DR(H-L)} = \frac{0.7W.2}{2(3.5)} = 0.2W$$

$$P_{DRIVER} = P_{DR(L-H)} + P_{DR(H-L)} = 0.47W$$

The Losses discussed are summarized in the table given below.

Table.2.1. Summary of the Loss Analysis

	High Side	**Low Side**
$\mathbf{P_{SW}}$	1.847W	Negligible
$\mathbf{P_{COND}}$	0.396W	1.044W
$\mathbf{P_{DRIVER}}$	0.47W	0.47W

2.4 Conclusion

The Converter designed for an output power of 39.6W suffers from the losses calculated as above mathematically. It is found that the switching loss of the high side alone swallows 4.62% of the converters output. Hence, it is of serious importance to minimize this loss for a better performance of the SBC.

Chapter 3

CONVERTER OPERATION AND DESIGN

The Proposed Converter

Modes of Operation

Converter Design Procedure

Selection of Devices

Conclusion

This chapter first introduces the proposed circuit of single phase ZVT synchronous buck converter and explores its various modes of operation with suitable waveforms and circuit diagrams. After this detailed study, design values for the converter are fixed. The criteria for selection of devices are also discussed.

3.1 The Proposed Converter

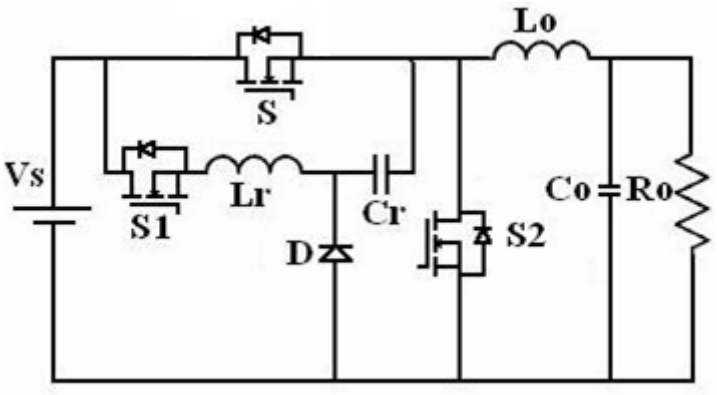

Fig.3.1. Proposed ZVT SBC

The circuit scheme of the proposed new ZVT SBC is shown in Fig.3.1. An auxiliary circuit added in parallel to S is the modification made to SBC. The auxiliary circuit consists of an S_1, C_r and L_r. It operates only during a short switching transition time to create ZVS condition for S. A high frequency Schottky diode D is used for discharging C_r to the load, which happens before the turn on of S_2.

During one switching cycle, the following assumptions are made in order to simplify the steady state analysis of the circuit shown in fig.3.1.

1. V_S is constant.

2. V_0 is constant or C_0 is large enough.

3. I_0 is constant or L_0 is large enough.

4. L_0 is much larger L_r.

5. Reverse recovery time of all diodes is ignored.

Considering the above assumptions, the converter is simplified as:

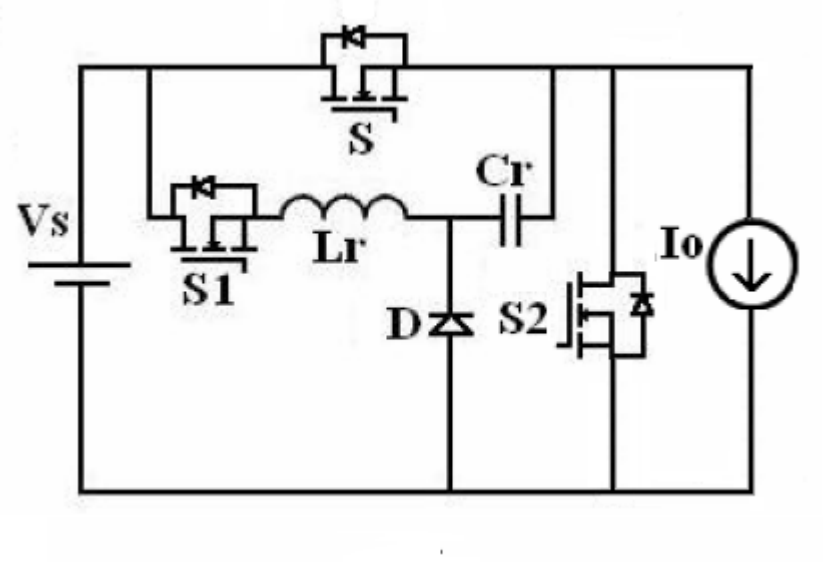

Fig.3.2. Simplified ZVT SBC

3.2 Modes of Operation

Seven stages take place in the steady state operation during one switching cycle in the proposed converter. The key waveforms of these stages are given in fig.3.3. The detailed analysis of every stage is presented below:

Mode 1 (t_0, t_1): Prior to $t = t_0$, S_2 was conducting. S and S_1 were in off-state. At t_0, S_1 is turned on which realizes zero-current turn-on as it is in series with L_r. The current through L_r and C_r rise at the same rate as the rate of fall of current through S_2. Resonance occurs between L_r and C_r during this mode. The mode ends at $t = t_1$, when i_{Lr} reaches I_0 and when S_2 turns off.

$$i_{S_2} = I_0 - i_{L_r} \qquad 3.1$$

$$i_{L_r}(t - t_0) = \frac{V_s}{Z} \sin \omega (t - t_0) \qquad 3.2$$

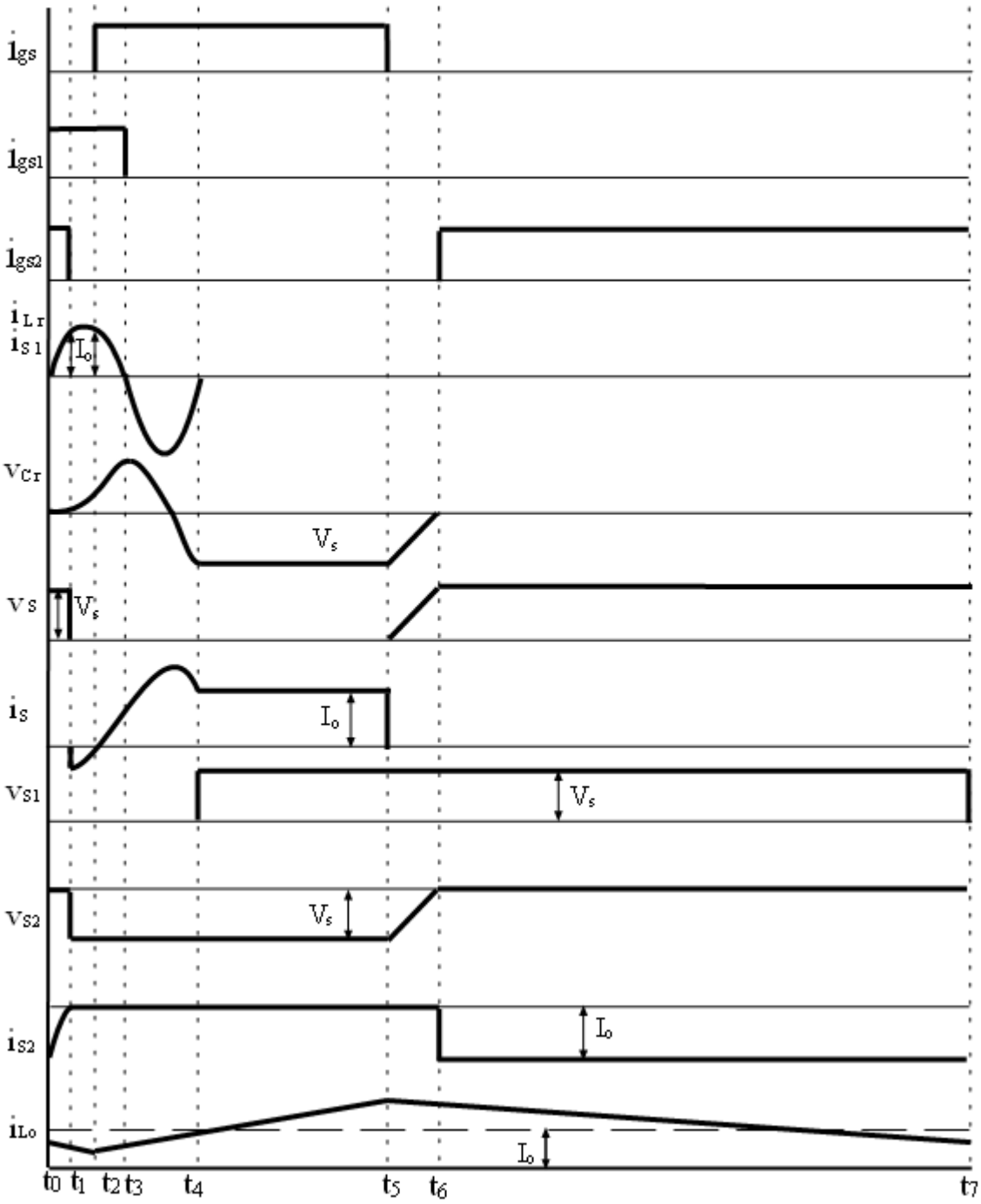

Fig.3.3. Theoretical Waveforms

$$\omega = \frac{1}{\sqrt{L_r C_r}} = \text{Resonant Frequency}$$

$$Z = \sqrt{\frac{L_r}{C_r}} = \text{Characteristic Impedance}$$

At $t=t_1$,

$$V_{C_r}(t_1 - t_0) = V_{C_{r1}} \qquad 3.3$$

$$i_{L_r}(t_1 - t_0) = I_0 \qquad 3.4$$

$$t_{01} = t_1 - t_0 = \frac{1}{\omega}\sin^{-1}\left(\frac{I_0 Z}{V_s}\right) \qquad 3.5$$

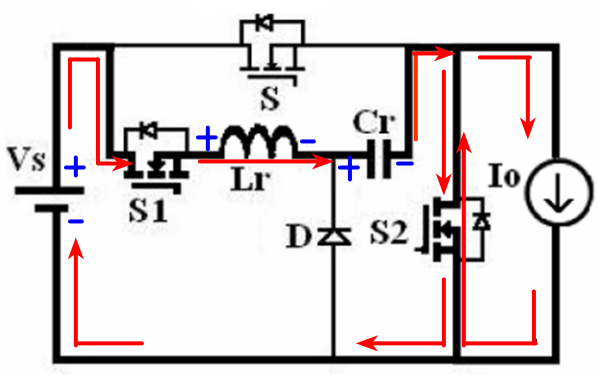

Fig.3.4. Converter Operation in Mode 1

Mode 2 (t_1, t_2): As L_r and C_r continue to resonate in this mode too, the current in excess to I_0 flows through the body diode of S, which is responsible for its zero voltage turn on. The conduction of the body diode discharges C_{DS} across S. As the auxiliary circuit is providing the required load, the body diode of S_2 does not conduct here as in the conventional converters, which causes a drop in output voltage during the dead time period. This mode ends when the C_{DS} is depleted of charges and when the inductor current again reaches I_0.

$$i_{S2} = 0 \qquad 3.6$$

$$i_{L_r}(t - t_1) = \frac{V_S - V_{C_{r1}}}{Z}\sin\omega(t - t_1) + I_0\cos\omega(t - t_1) \qquad 3.7$$

At $t=t_2$,

$$i_{L_r}(t_2 - t_1) = I_0 \qquad 3.8$$

$$t_{12} = \frac{2}{\omega}\left(\tan^{-1}\left(\frac{V_S - V_{C_r}}{I_0 Z}\right)\right) \qquad 3.9$$

$$V_{C_r}(t_2 - t_1) = V_{C_{r2}} \qquad 3.10$$

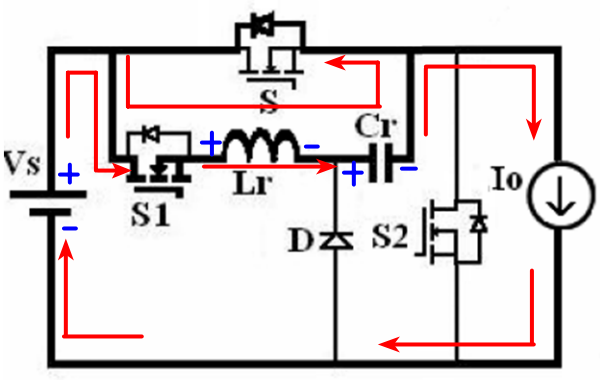

Fig.3.5. Converter Operation in Mode 2

Mode 3 (t_2, t_3): At t_2, S is turned-on with ZVS. During this stage the growth rate of i_s, is determined by the resonance between L_r and C_r. The resonant process continues in this mode too where the current i_{Lr} continue to decrease. Again in this mode, since S is turned on at the instant $i_{Lr}=I_0$, the body diode of the S_2 does not conduct here too because S_1 starts supplying the required output. At the end of this mode i_{Lr} equals zero and resonant capacitor voltage equals $v_{Cr(max)}$.

$$i_{L_r}(t - t_2) = \frac{-V_{C_{r2}}}{Z}\sin\omega(t - t_2) + I_0\cos\omega(t - t_2) \qquad 3.11$$

At $t=t_3$,

$$i_{L_r} = 0 \qquad 3.12$$

$$t_{23} = \tan^{-1}\left(\frac{I_0 Z}{V_{C_{r2}}}\right) \qquad 3.13$$

$$V_{C_r}(t_3) = V_{C_{r(max)}} \qquad 3.14$$

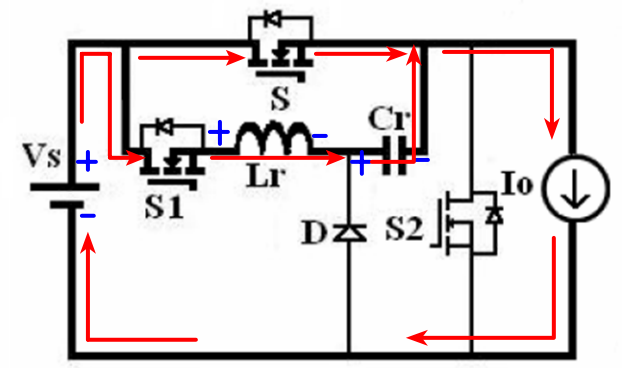

Fig.3.6. Converter Operation in Mode 3

Mode 4 (t_3, t_4): At t_3, S_1 is turned-off with ZCS. The resonant capacitor starts to discharge through the body diode of the switch S_1, which causes the resonant current i_{Lr} to rise in the reverse direction. It reaches a maximum negative and increases to zero. At the end of this mode, body diode of S_1 is turned off and the resonant peak current flowing through the main switch is zero. C_r is charged to $-v_{Cr\,(max)}$.

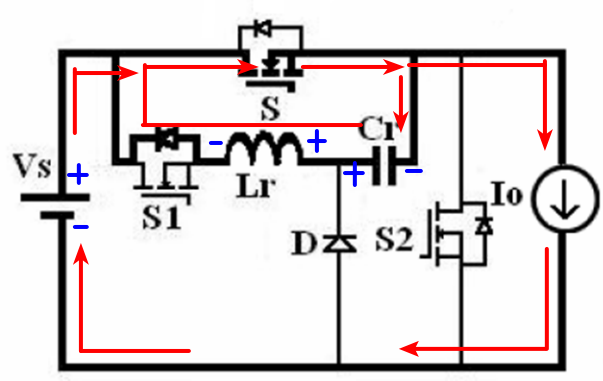

Fig.3.7. Converter Operation in Mode 4

$$i_{L_r}(t - t_3) = \frac{V_{C_{r(max)}}}{Z} . \sin \omega (t - t_4) \quad 3.15$$

At $t = t_4$,

$$i_{L_r}(t_4) = 0 \quad 3.16$$

$$t_{34} = \frac{\pi}{\omega} \quad 3.17$$

$$V_{C_r}(t_4) = -V_{C_{r3}} \quad 3.18$$

Mode 5 (t_4, t_5): Since the body diode of S_1 has turned off at t_4, now only the S carries the load current. There is no resonance in this mode and the circuit operation is identical to a conventional PWM buck converter.

$$i_S = i_0 \qquad 3.19$$

$$V_{C_r}(t_5) = -V_{C_{r3}} \qquad 3.20$$

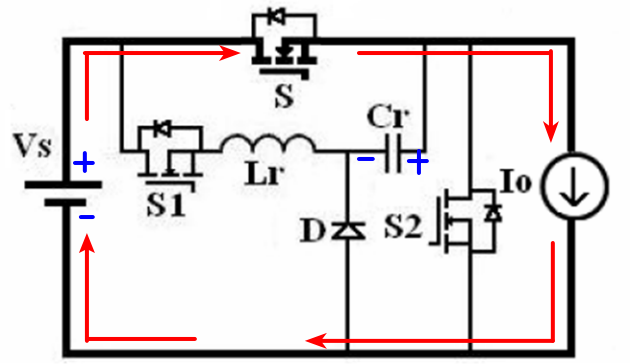

Fig.3.8. Converter Operation in Mode 5

Mode 6 (t_5, t_6): At t_5, S is turned off with ZVS and D starts conducting. The resonant energy stored in C_r is transferred to the load through D. This mode finishes when Cr is fully discharged.

$$V_{C_r}(t - t_5) = -V_{C_{r3}} + \frac{I_0}{C_r}(t - t_5) \qquad 3.21$$

At $t=t_6$,

$$V_{C_r}(t_6) = 0 \qquad 3.22$$

$$t_{56} = \frac{C_r V_{C_{r3}}}{I_0} \qquad 3.23$$

Mode 7 (t_6, t_7): During this mode, the converter operates like a conventional PWM buck converter until the switch S_1 is turned on in the next switching cycle.

$$i_{S2} = I_0 \qquad 3.24$$

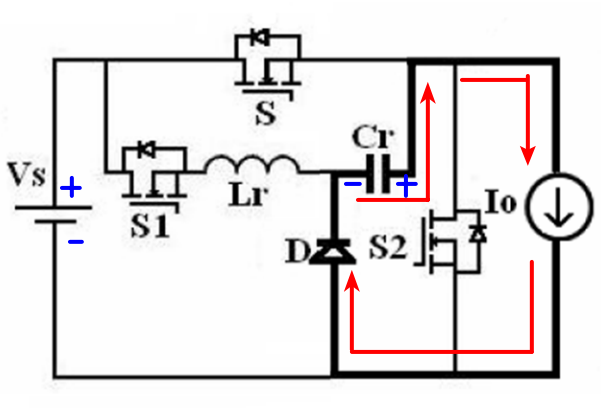

Fig.3.9. Converter Operation in Mode 6

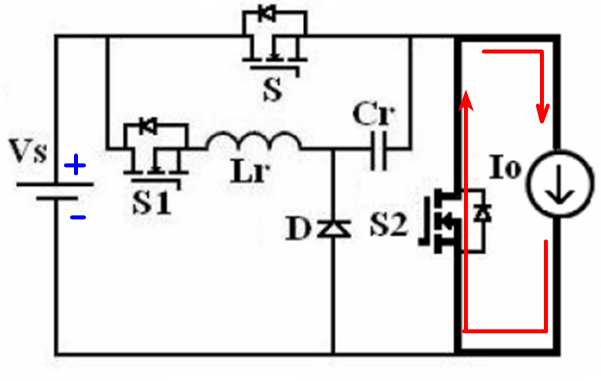

Fig.3.10. Converter Operation in Mode 7

3.3 Converter Design Procedure

The inductor current waveform I(L_0) in a conventional synchronous buck converter contains a dc component I_0 and a linear ripple of peak magnitude dI as shown in fig.3.11. In a well designed converter, the dc component I_0 entirely flows through the load resistance R_0 and the entire inductor current ripple flows through C_0 as it is chosen large enough such that its impedance at the switching frequency is much smaller than load [8]. Hence using a high value of L_0 and C_0 gives a ripple free constant output current and voltage at a constant load.

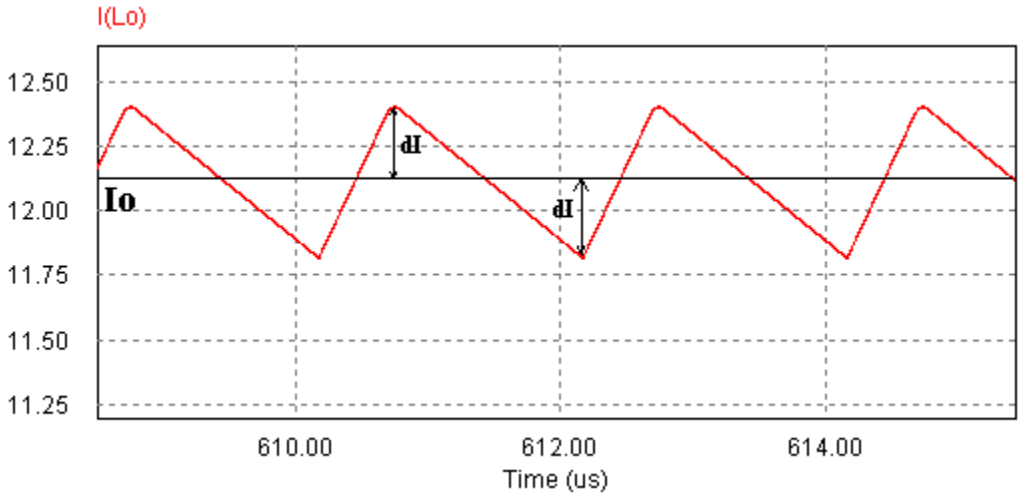

Fig.3.11. Inductor Current Waveform in SBC

The auxiliary circuit in this proposed converter operates only for a short period of time. Hence for most of the switching time, it resembles a conventional SBC. Hence the value of L_0 and C_0 can be computed by the established equations used for the conventional converter.

The converter is to be designed for V_S = 12V, V_0 = 3.3V, I_0=12A and f_s = 200 kHz.

$$L_0 = \frac{(V_s - V_0)(d.T_s)}{2.\Delta i_L} \qquad 3.25$$

$$L_0 = \frac{(12V - 3.3V)(0.275\ X\ 5\mu s)}{2X12\ X\ 5\%} = 9.969\mu H$$

$$C_0 = \frac{\Delta i_L.T_s}{8.\Delta V_c} \qquad 3.26$$

$$C_0 = \frac{0.6A\ X\ 5\mu}{8\ X\ 3.3V\ X\ 0.1\%} = 113.64\ \mu F$$

The auxiliary circuits in ZVT turns on before the main switch and turns off after the main switch is turned on. During the period between auxiliary and main switch turn-on, the resonant inductor is charged to I_p, which is designed for a very few amperes more than I_0.

V_S entirely flow only to charge L_r and C_r up to the time period t_2 i.e. up to the charging of inductor current to I_p. Hence a series LC resonant circuit solution as in equation 3.2 is applicable here to find the values of L_r and C_r.

The resonant inductor current in a series LC resonant circuit from 3.2 is given by

$$i_{L_r}(t) = I_P . \sin \omega t \qquad 3.27$$

$$I_P = V_S . \sqrt{\frac{C_r}{L_r}} \qquad 3.28$$

For I_p= 12.2A, V_S = 12V

$$C_r = 1.0336\, L_r \qquad 3.29$$

$$t_p = \frac{\pi}{2\omega} = \frac{\pi\sqrt{L_r C_r}}{2} \qquad 3.30$$

The converter is designed for f_S of 200 kHz. Hence, T_S = 5µs. It is considered for simplification that S is turned on at 0.4166µs (i.e. at 30° of the 360°, which is one switching cycle). The body diode of S is designed to operate for 5°s from 25° to 30°. Hence, the peak value occurs approximately at 27° i.e. at,

$$t_p = 0.375\mu s \qquad 3.31$$

Thus referring to equations 3.29, 3.30, 3.31,

$$L_r = \frac{2 \text{ X } 0.375\mu s}{1.0336 \text{ X } 3.14} = 231.09 \text{ nH}$$

$$C_r = 1.0336\, L_r = 238.85 \text{ nF}$$

These designed values are summarized below:

Table.3.1. Designed Values for the converter

Parameter	Value
L_0	10μH
C_0	120μF
L_r	230nH
C_r	240nF

3.4 Selection of Devices

3.4.1 MOSFET Selection

When selecting the MOSFETs, there is a fundamental choice of whether to use an N channel or P channel device for the upper switch. N channel MOSFETs have the advantage of lower on resistance for a given die size and often have lower gate charge. They also tend to be relatively inexpensive. Their chief drawback is that they need a bootstrapped drive circuit or a special bias supply for the driver to work, since the gate drive must be several volts above the input voltage to the converter to enhance the MOSFET fully.

Conversely, P channel MOSFETs has simpler gate drive requirements. They require that their gate be pulled a few volts below the input voltage for them to be turned on. Their disadvantage is that their cost is higher as compared to their N channel counterpart for an equivalent $R_{ds(on)}$, and they generally have slower switching times. For a lower side switch S_2, an N channel MOSFET with a very low on-state resistance is usually preferred. For soft switching applications, C_{oss} is important because it can affect the resonance of the circuit.

3.4.2 Inductor and Capacitor Selection

The optimum inductor value for a particular supply is dependent on the switching frequency, transient performance, and the conduction losses in the inductor and other components. Some of the merits for selecting a low vs. high inductor value for a given core size and geometry are summarized below:

A. Benefits of Lower Inductor Values

1. Low DCR: lower DC inductor losses in windings
2. Fewer turns: higher DC saturation current
3. High di/dt: faster response to load step / dump
4. High di/dt: fewer output capacitors required for good load transient recovery

B. Benefits of Higher Inductor Values

1. Low ripple: lower AC inductor losses in core (flux) and windings (skin effect)
2. Low ripple: lower conduction losses in MOSFETs
3. Low ripple: lower RMS ripple current for capacitors
4. Low ripple: continuous inductor current flow over wider load range

In general, lower inductor values are best for higher frequency converters, since the peak-to peak ripple current decreases linearly with switching frequency. A good rule of thumb is to select an inductor that produces a ripple current of 10% to 30% of full load DC current. Too large an inductance value leads to poor loop response, and too small an inductance value leads to high AC losses. The capacitor value is chosen based on L_0. A high value of C_0 gives fewer ripples and vice-versa.

3.5 Conclusion

A few assumptions were made to ZVT SBC for steady state analysis of the circuit. The various modes of its operation are presented neatly, thereby designing the converter parameters. Using these values the performance of the converter is examined by both simulation and experiment in the next chapter. Various criteria in selecting the devices for experimental set up are discussed briefly.

Chapter 4

RESULTS AND DISCUSSION

The Simulation Results

The Experimental Results

Conclusion

The parameters of SBC considered for the loss analysis and design in chapter 2 and chapter 3 is adopted here for simulation and experimental validation. The simulation results are validated with experimental observations.

The simulation is carried out in PSIM pro 7.1.2 by assigning the appropriate designed value for each element. PSIM is a simulation package specifically designed for power electronics and motor control. With its user-friendly interface, its simulation speed, its capability of simulating any type of power converters and control circuits, PSIM is ideal for system-level simulation, control loop design, and motor drive system studies.

4.1 The Simulation Results

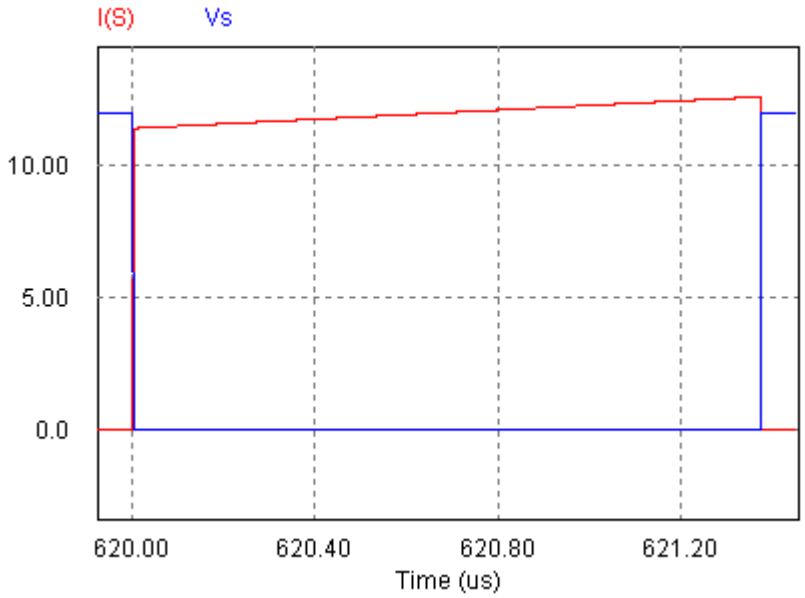

Fig.4.1. Switching Waveform of S in SBC

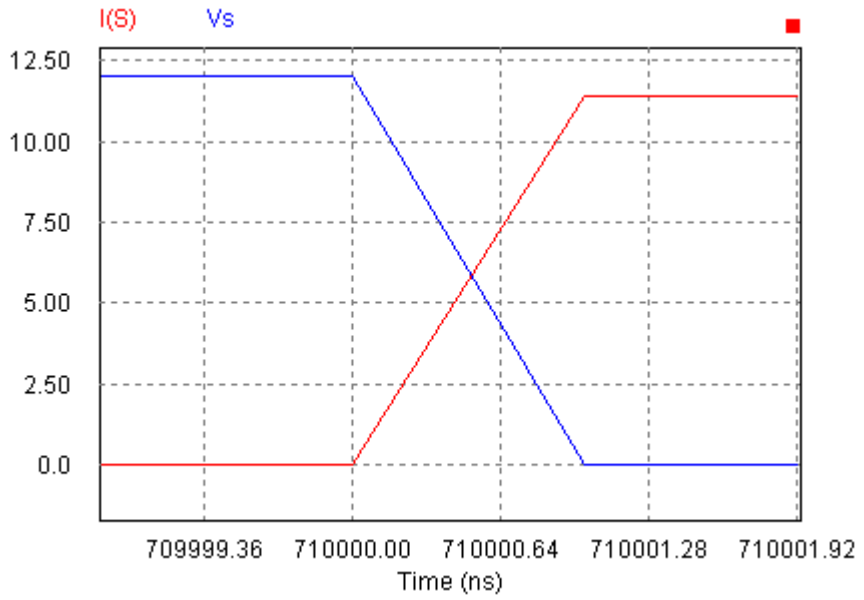

Fig.4.2. Enlarged Switching Waveform of S in SBC

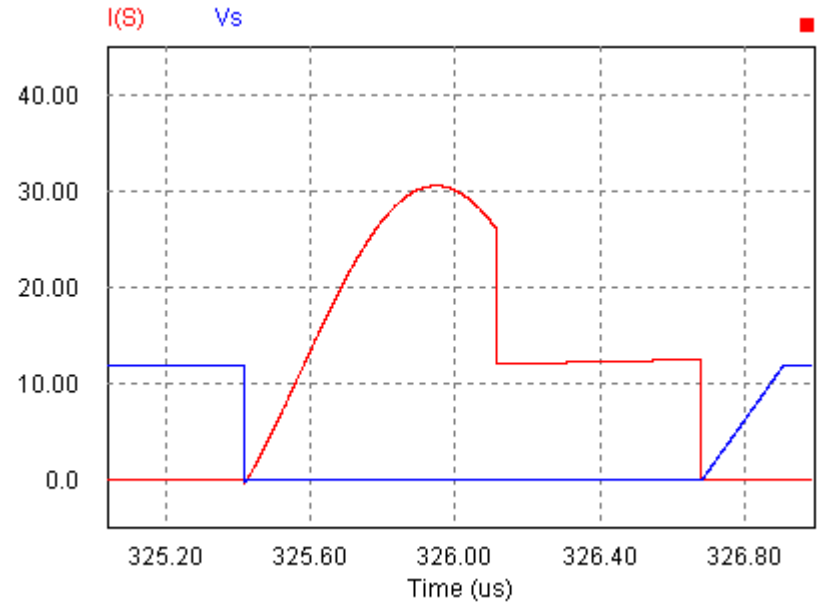

Fig.4.3. Switching Waveform of S in ZVT SBC

Fig. 4.1 and Fig. 4.2 show the switching action of S in SBC which suffers from the switching loss. The Fig. 4.3 presents the switching action of S in the proposed converter, which is devoid of the switching loss but the peak current raises an issue on the conduction

loss. From the equation 2.2 it is recalled that the conduction loss of switch S for the same design in SBC is 0.396W. The average current flowing through switch S from fig. 4.3 is measured as 17.067A and the conduction loss is,

$$P_{COND} = 17.067A^2.10m\Omega.\frac{3.3V}{12V} = 0.801W$$

Whereas, switching loss for SBC from 2.12 is 1.847W at f_S = 200 kHz but from the same equation it is inferred that switching loss varies linearly with f_S .S_1 also conducts only for a short duty cycle, hence negligibly less conduction loss arising from it. As seen from fig. 4.4, S_1 is also devoid of the switching loss. Taking all these into account, the proposed converter is efficient than the conventional converter.

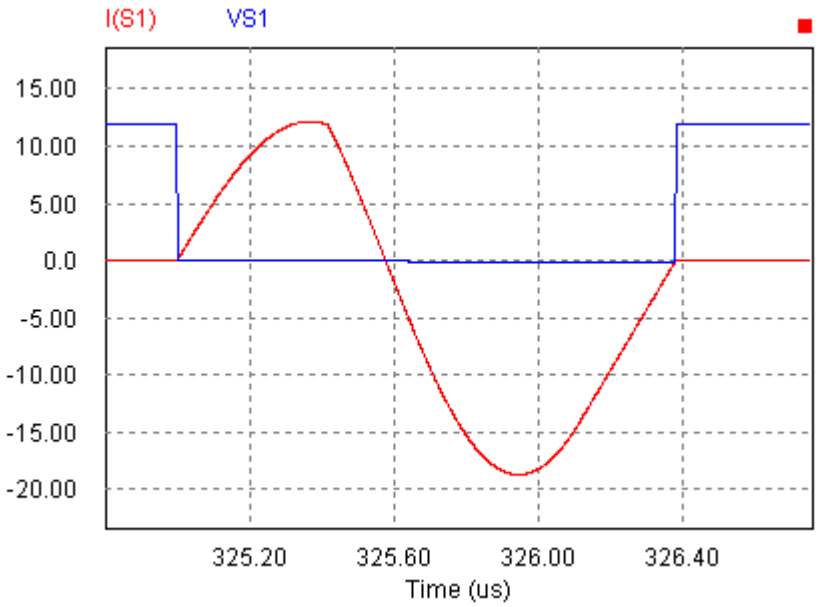

Fig.4.4. Switching Waveform of S_1 IN ZVT SBC

The ripple in the output inductor current L_0 shown in fig.4.7 almost entirely flows through the output capacitor C_0 shown in fig.4.7. This provides a good tolerant output voltage. Output Voltage and current match the designed values of 3.3V, 12A as shown in fig. 4.9 and 4.10.

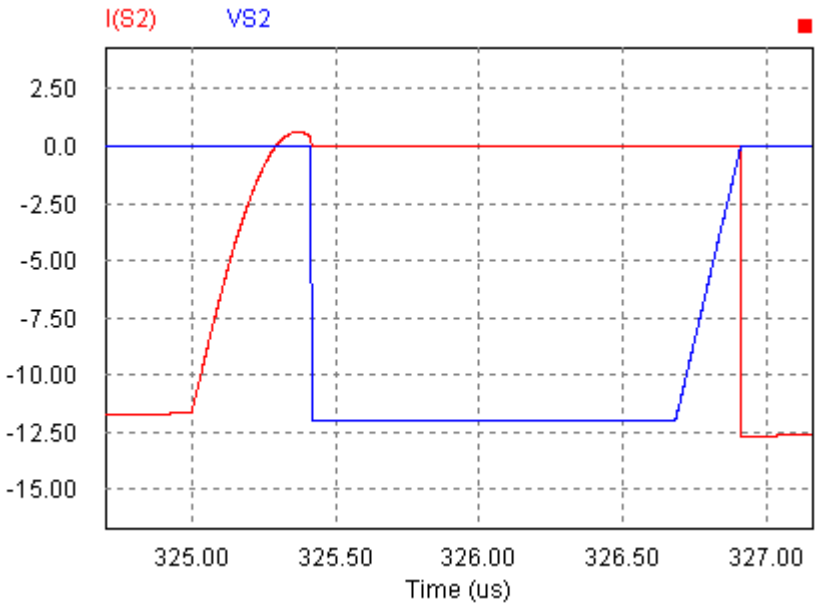

Fig.4.5. Switching Waveform of S_2 in ZVT SBC

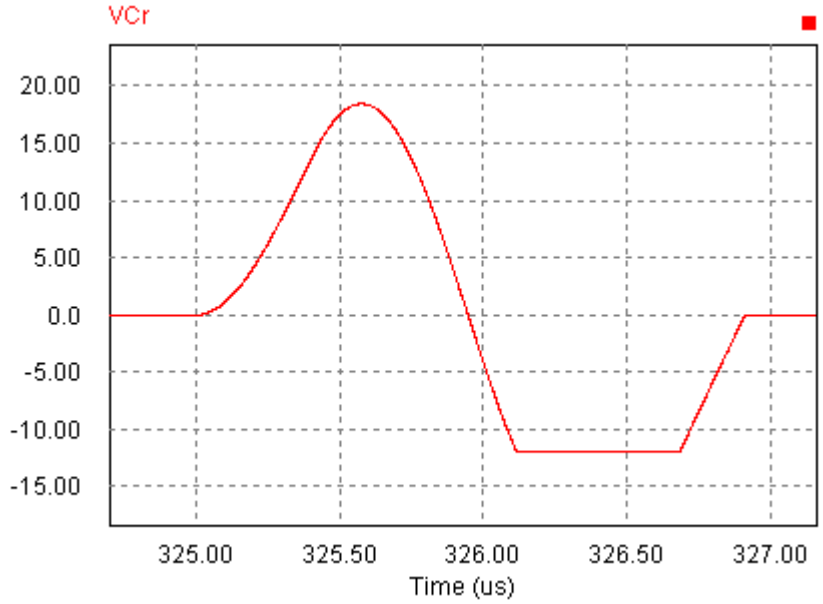

Fig.4.6. Resonant Capacitor Voltage

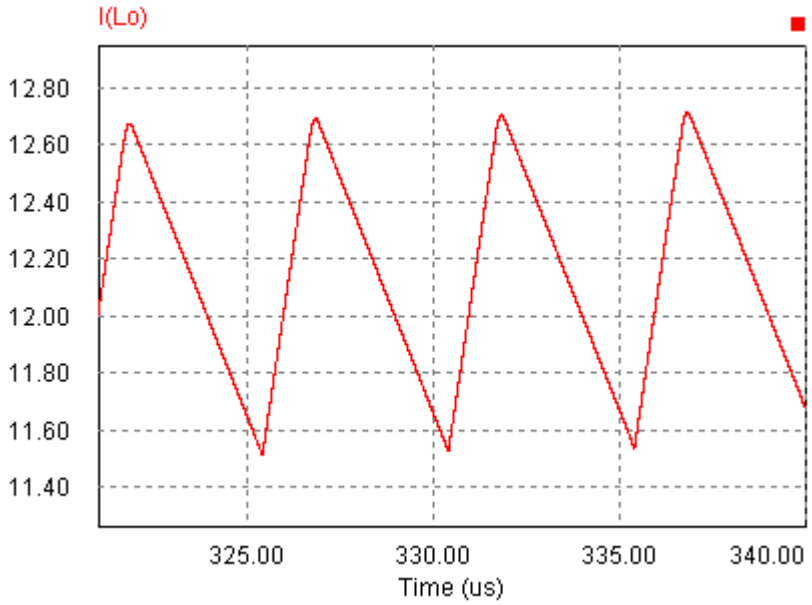

Fig.4.7. Output Inductor Current

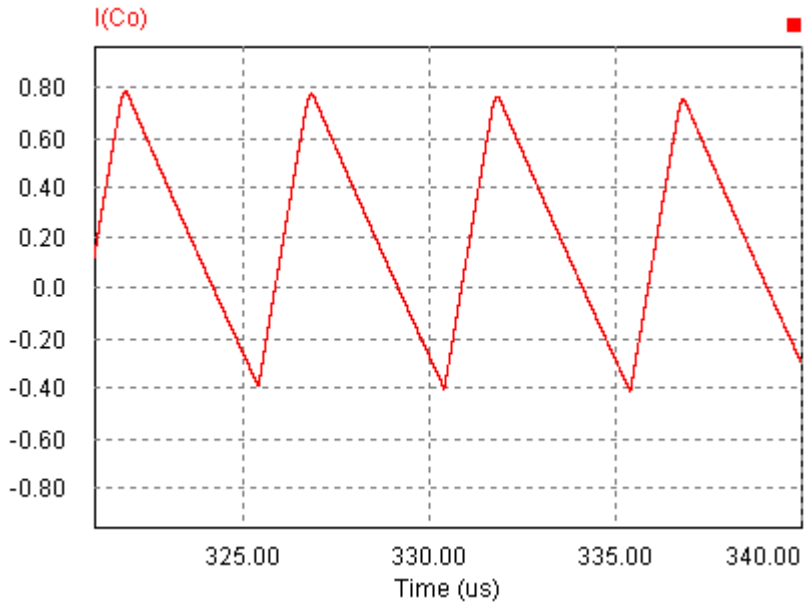

Fig.4.8. Output Capacitor Ripple Current

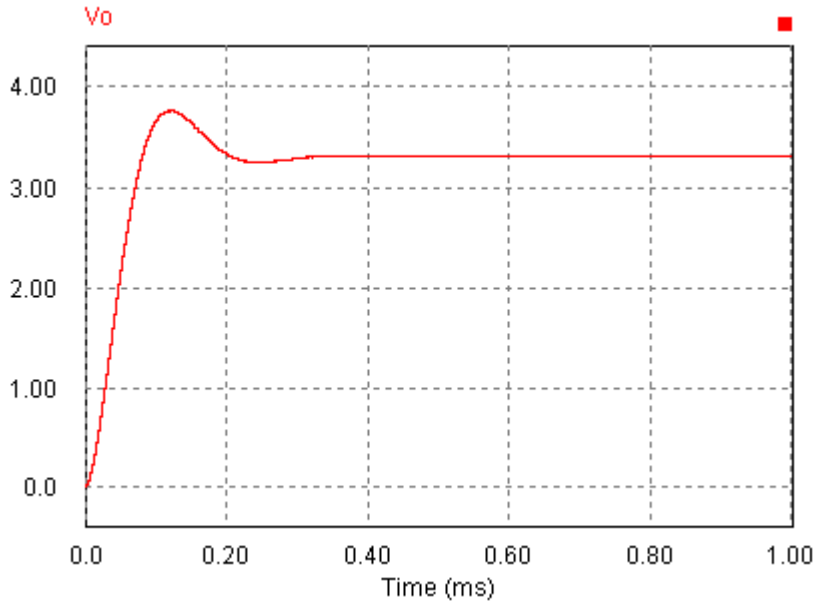

Fig.4.9. Output Voltage

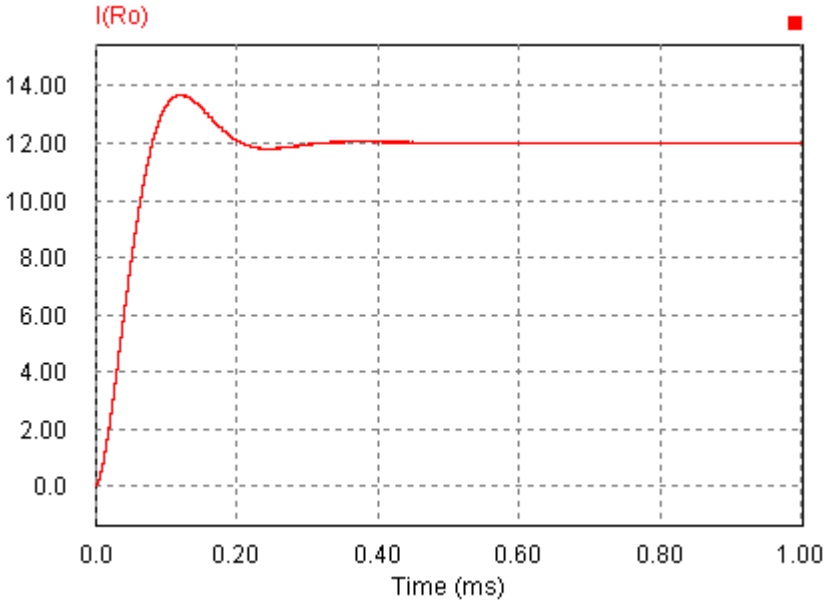

Fig.4.10. Output Current

4.2 The Experimental Results

A prototype of the circuit is developed at 200 kHz. MOSFET IRF1312 is used for the high-side switch S, auxiliary switch S_1 and for the low side switch S_2 as well owing to its excellent feature of having low gate charge and on-state resistance. ELHC300, an APLAB Programmable electronic DC load of voltage rating 0-120V DC and current rating 0-60A is used to vary the load and quantify efficiency.

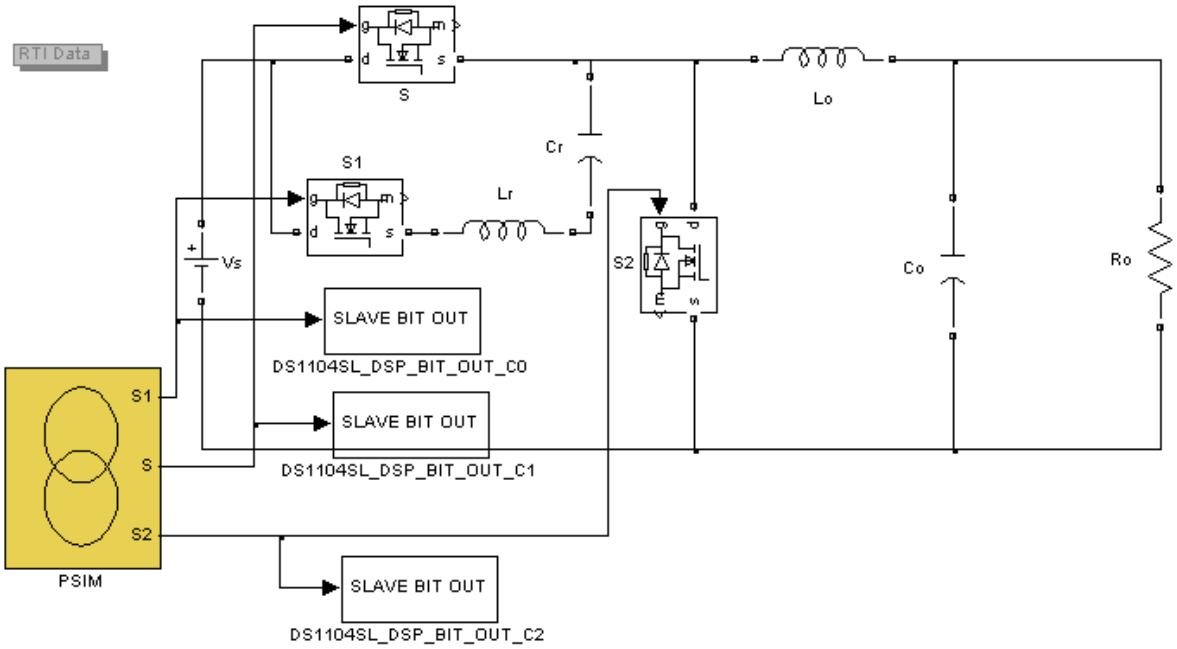

Fig.4.11. SIMULINK – dSPACE interface

The PWM signals are generated using dSPACE DS1104 as shown in fig. 4.11. The yellow color block built in PSIM defines the conduction period of the switches. The "SLAVE BIT OUT" is dSPACE's slave DSP block. The signals from PSIM are taken to the experimental set up through this slave DSP I/O block. More information on dSPACE is given in the appendix.

Schottky diode D_S is used anti-parallel to the S_1 to avoid the conduction of its body diode. However, a small amount of current flows through the body diode. Adding one more Schottky diode in series to S_1 will fully block the reverse current through the body diode but it may increase the forward voltage drop.

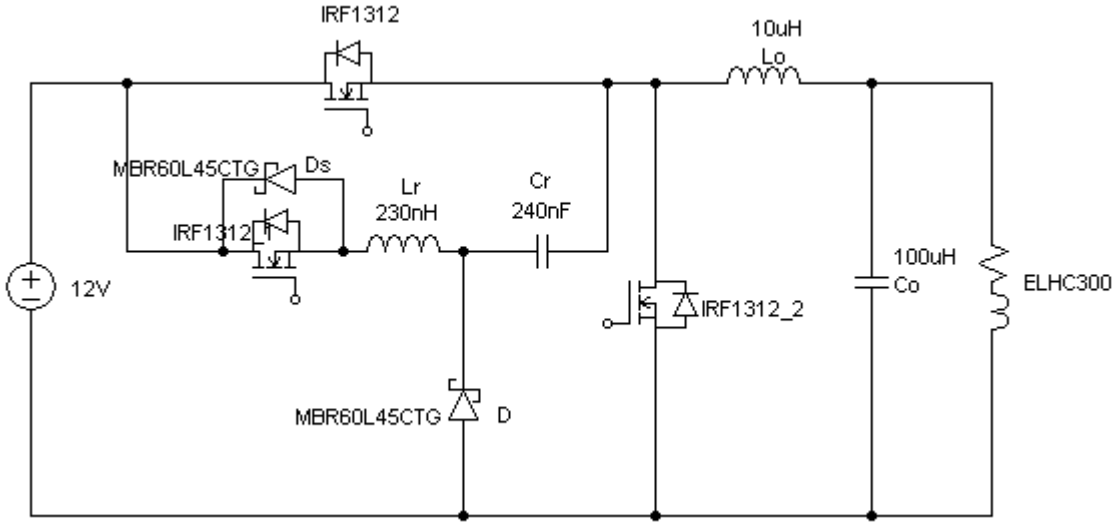

Fig.4.12. Schematic of Experimental circuit

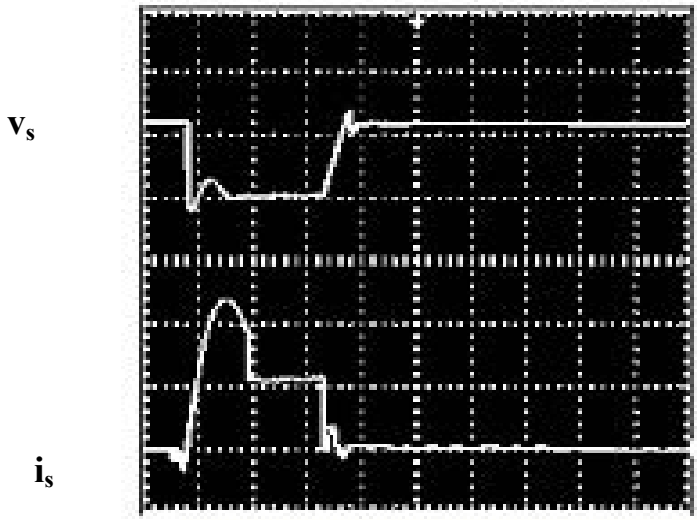

Fig.4.13. Main Switch S: v_S; i_S: (V: 10 V/div, I: 10 A/div, time: 0. 5 µs/div)

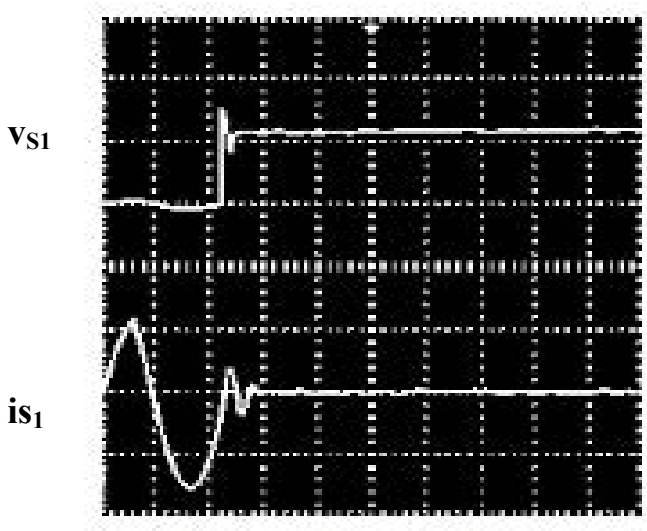

Fig.4.14. Auxiliary Switch S_1: v_{S1}; i_{S1}: (V: 10 V/div, I: 10 A/div, time: 0. 5 µs/div)

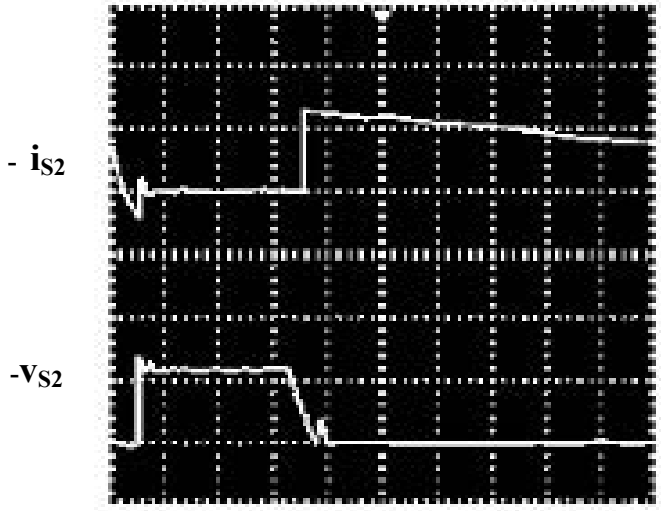

Fig.4.15. Synchronous Switch S_2: v_{S2}; i_{S2}: (V: 10 V/div, I: 10 A/div, time: 0. 5 µs/div)

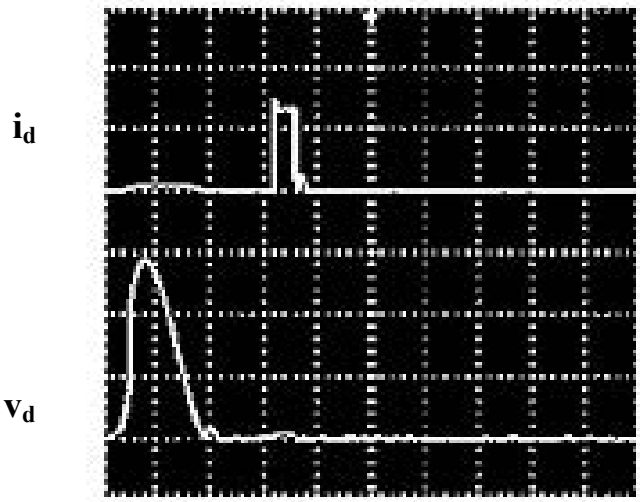

Fig.4.16. Schottky Diode D: v_d; i_d: (V: 10 V/div, I: 10 A/div, time: 0. 5 µs/div)

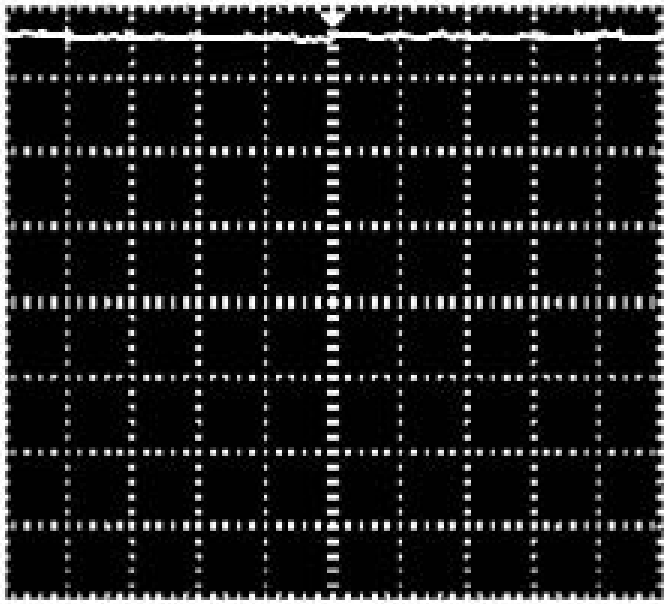

Fig.4.17. Output Voltage: v_o (V: 1 V/div, time: 2.5 µs/div)

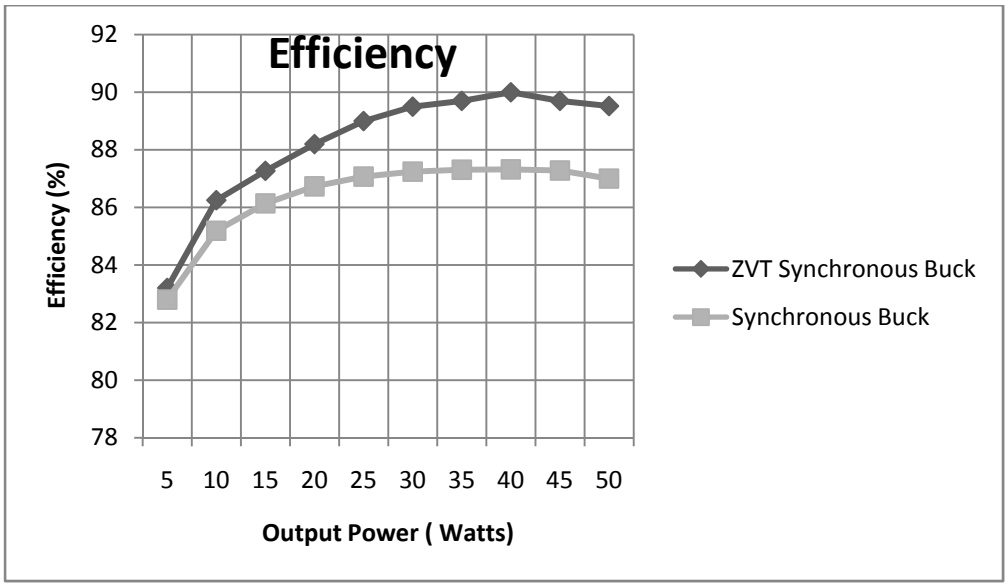

Fig.4.18. Efficiency plot between ZVT SBC and SBC

Fig. 4.12, 4.13 and 4.14 is seen to switch on and off with zero current and voltage. They match exactly with the simulation results in fig. 4.3, 4.4 and 4.5. The output voltage presented in fig. 4.16 has a small ripple and it is seen to remain constant at 3.3V. Finally, the fig. 4.17 clearly verifies the improved performance of the proposed converter.

4.3 Conclusion

The simulation and experimental results obtained were in accordance to the design aspects. With this satisfactory output, the auxiliary circuit is added to MSBC, which is widely used nowadays in the computer processors power supplies. The portable power mostly use single phase SBC for their power supplies.

Chapter 5

MULTIPHASE ZVT SYNCHRONOUS BUCK CONVERTER

Schematic of ZVT MSBC

Design Considerations

Simulation Results

Conclusion

High performance Voltage Regulator Modules (VRMs) for the new generation of microprocessors have many strict and challenging specifications that include high power density, high output current capability, low output voltage deviation and fast transient-response. According to Intel's roadmap, over tens of billions of transistors will be integrated into one processor by 2015 [3]. The consumption current will be increased to 200A while the voltage is down to 0.8V by 2010 [47]. Such high current low voltage converter implementation with improved performance is possible by multiphase circuits. In this chapter MSBC with the proposed resonant auxiliary circuit has been simulated and results are presented.

5.1 Schematic of ZVT MSBC

Fig. 5.1 shows the schematic circuit of ZVT 2 phase MSBC. Each phase is built up with identical structure for equal sharing of current between the phases.

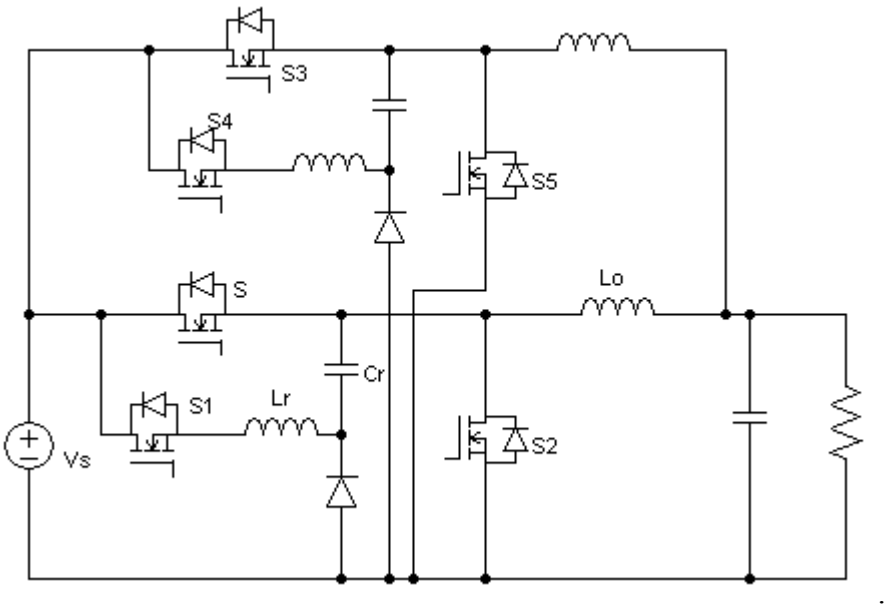

Fig.5.1. Schematic of a 2-Phase ZVT MSBC

5.2 Design Considerations

A 4 Phase ZVT MSBC is designed for V_S = 12V, V_0 = 1.2V, I_0 = 90A, and f_s= 500 kHz. These values of Pentium IV are taken from [4]. The design procedure, operation of this converter is the same as the single phase ZVT SBC. The circuit parameters L_0 = 960nH, L_r = 26nH, C_r = 95nF are same for all the phases and the output capacitance is C_0 = 20µF.

Compared to the single phase SBC, a low inductor value is obtained from the design equations. Interleaving VRs with small inductances reduces both the steady state voltage ripples and the transient voltage spikes, so that a much smaller output capacitance can be used to meet the steady state and transient voltage requirements. Thus, power density can be significantly improved. Moreover, interleaving makes the thermal dissipation more evenly distributed.

5.3 Simulation Results

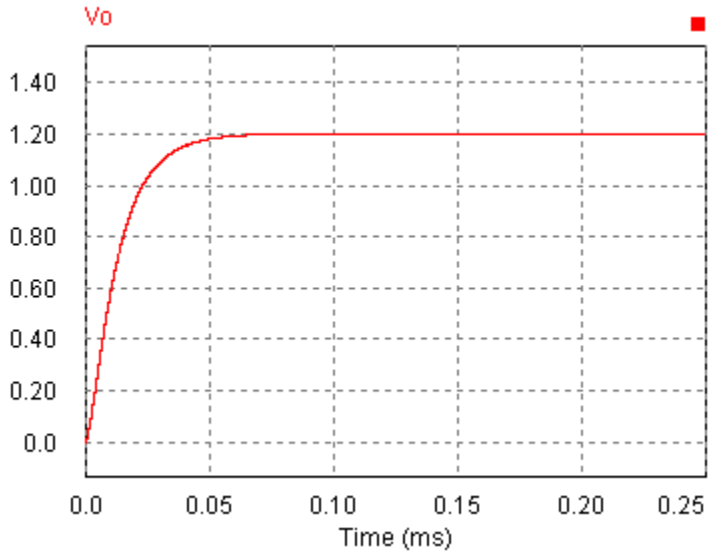

Fig.5.2. Output Voltage

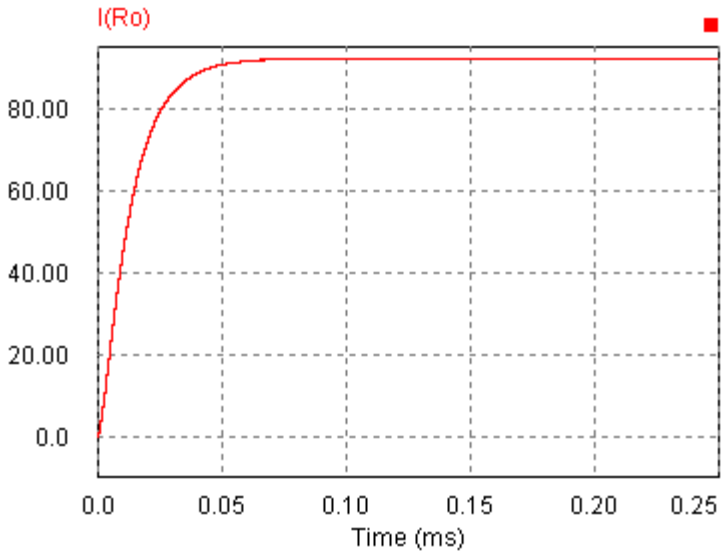

Fig.5.3. Output Current

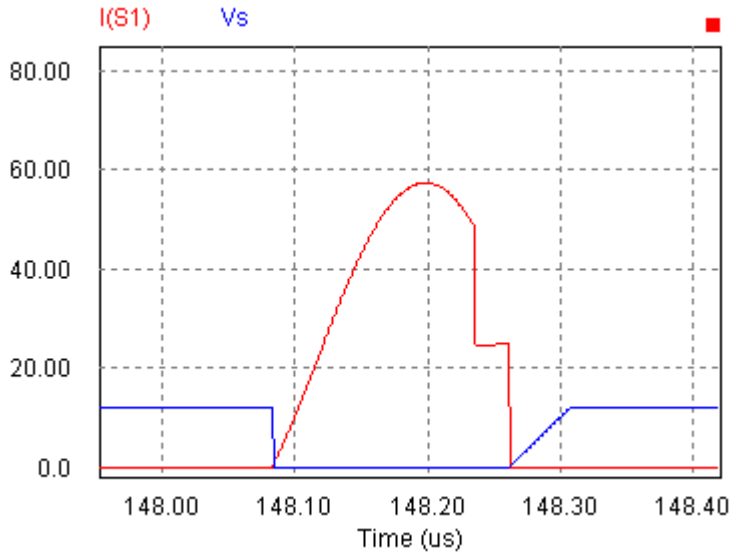

Fig.5.4. Switching action of S

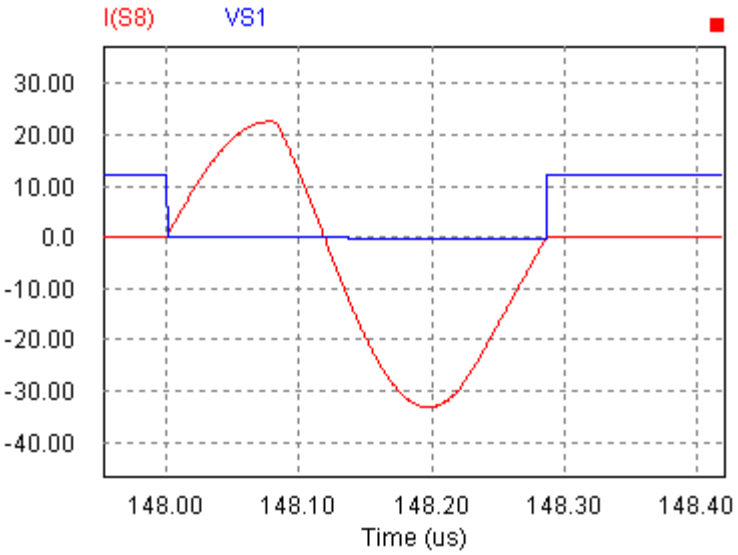

Fig.5.5. Switching action of S_1

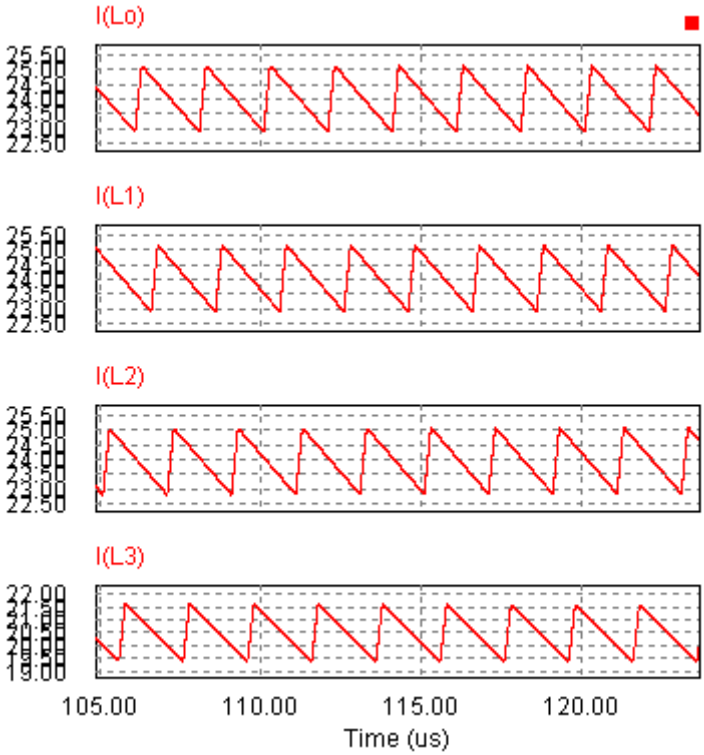

Fig.5.6. Inductor Current in the Different Phases

Fig.5.2 and Fig.5.3 shows the output voltage and current matching with the design value of 1.2V and 90A. Fig. 5.4 and Fig. 5.5 show the switching action of S and S_1, which are devoid of the switching loss. Fig. 5.6 shows the sharing of inductor current in all the four phases. Almost equal current is flowing in all the phases, which provides an equal amount of stress on all the high side switches. Fig. 5.7 shows the efficiency calculation, where the ZVT MSBC has an edge over the MSBC.

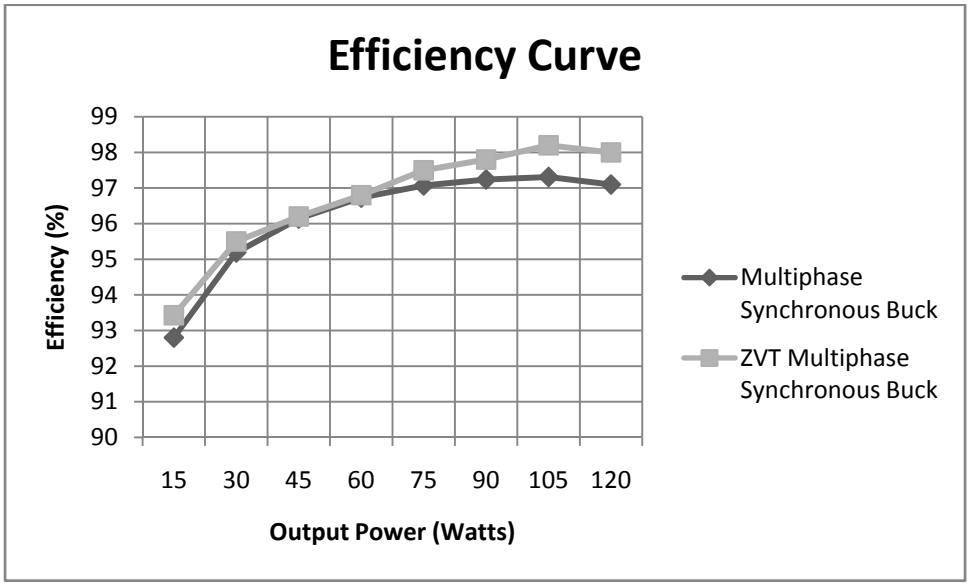

Fig.5.7. Efficiency plot between MSBC and ZVT MSBC

5.4 Conclusion

A new ZVT MSBC is presented in this chapter. An auxiliary switch is added in each of the phases to eliminate the switching losses by creating a partial resonance. It is concluded from simulation that none of the switches used in this converter suffers from the switching loss. This proposed converter is efficient in the active mode but during the sleep mode or at low powers, its performance is on par with the conventional one. It is hence concluded that eliminating switching losses in ZVT MSBC delivers power efficiently to the computer processors.

Chapter 6

CONCLUSION

Summary

Future Work

6.1 Summary

Nano technology is driving VLSI (very-large-scale integrated) circuits in a path of greater transistor integration and faster clock frequencies. This has imposed a challenge for delivering high current and low voltages at greater switching frequencies to modern processors. Increase in the switching frequency cause the switches to turn on and off in a very short period. This forms the basis for the switching loss, which increases linearly with switching frequency. Furthermore, the Moore's Law is perceived to prevail at least for the next decade, with continuous advancements of processing technologies for VLSI circuits. Hence, eliminating the switching loss for an efficient power supply becomes the need of the hour.

It is the purpose of this work to develop high-efficiency, high-power density VRs (Voltage Regulators) to power present and future generations of processors. This dissertation has focused on the following:

1. Analysis of various losses occurring in Synchronous Buck Converters (SBCs)
2. Modeling of a new Zero Voltage Transition (ZVT) SBC for portable applications
3. A VR structure for powering today and future's microprocessors those are used in desktop, laptop.

In order to build an efficient converter, it is necessary to identify and quantify the losses occurring in it. Hence, a mathematical analysis of the SBC is carried out. The results prove the domination of high side switching loss over the rest of the losses. Moreover, it consumes a major share in the converters output.

Following the vision of eliminating high side switching loss, SBC is modeled with the very attractive ZVT soft switching technique. In comparison to the other methods, the current and voltage stress on the switches is very low in ZVT.

The new designed ZVT SBC is then simulated for 12V input, 12A/3.3V output at switching frequency of 200 kHz. None of the switches is found to suffer from the switching losses. It is also experimentally proved that ZVT SBC is able to achieve a higher efficiency than the conventional converter, not only at full load condition but also at light load condition by the soft switching technique. This unique feature makes the approach even more attractive for the portable applications.

However, for desktop processor power supplies multiphase synchronous buck converters (MSBC) are employed as its current demand is much more in comparison to the portable application devices. The concept of removing switching loss by ZVT technique is also extended to MSBC. Simulation is performed to analyze its performance. Alike the single phase, ZVT MSBC is also found to deliver an efficient performance.

As a conclusion, eliminating the semiconductor devices switching losses is a promising solution for powering future processors. It is widely effective in computer and communication systems. Far beyond that, it provides a feasible platform for new architectures to power the future microprocessors.

6.2 Future Work

The ZVT MSBC is not implemented practically. It has an auxiliary circuit present in each phase, which may increase the cost and size of the converter. The immediate idea is to employ a single auxiliary circuit for any number of phases used. Designing the converter as mentioned brings in a few more problems. They are mainly:

1. Current flows through the body diode of all the non-conducting switches, when the auxiliary circuit is in operation.
2. Employing a few more switches in avoiding the above problem makes the converter circuit complex.

Imparting the above suggested change to it arrives as a challenge to the power supply design engineers. Applying the above suggestion to the converter may provide much better efficiency at low powers also, which is not achieved in this work.

Appendix

dSPACE DS1104

The Matlab Simulink, by use of the Real Time Interface (RTI) is capable to link the simulation files to the real world, namely is possible to connect the variables of simulation structure to physical input-output units, (analog to digital and digital to analog inverters, digital in/outs etc). Using appropriate hardware it is possible to generate code, (executed on the target processor) based on simulation structure. In this way the time-consuming programming can be avoided and results a very powerful and efficient development procedure. This approach was used by dSPACE in design of its DS series of controller cards, dedicated for real time control of fast processes like electrical drives. The DS1104 card contains all necessary peripherals and computing power (offered by a PowerPC master-processor and TMS320F240 slave-DSP) for implementation of complex drives structures. The software associated to the card provides the control for the implementation process from simulation up to real time experiment.

The dSPACE systems used for Motor/Control labs is an embedded or self contained system. The PCI controller card DS1104 installed in the computers is its own entity. None of the processing for a system implemented on the DS1104 dSPACE board is done by the host PC. As a result the board requires that software be created and downloaded to the board for the system to function. The MPC8240 PowerPC 603e processor and TMS320F240 DSP on the card provide the computing power necessary for real time control tasks.

The Control Desk software, which comes along with the installation, is used to design the system implementation and interface with the DS1104 dSPACE board. It is used to download software to the board, start and stop the function of the DS1104 as well as create a layout for interfacing with global variables in C/C++ programs used for implementation.

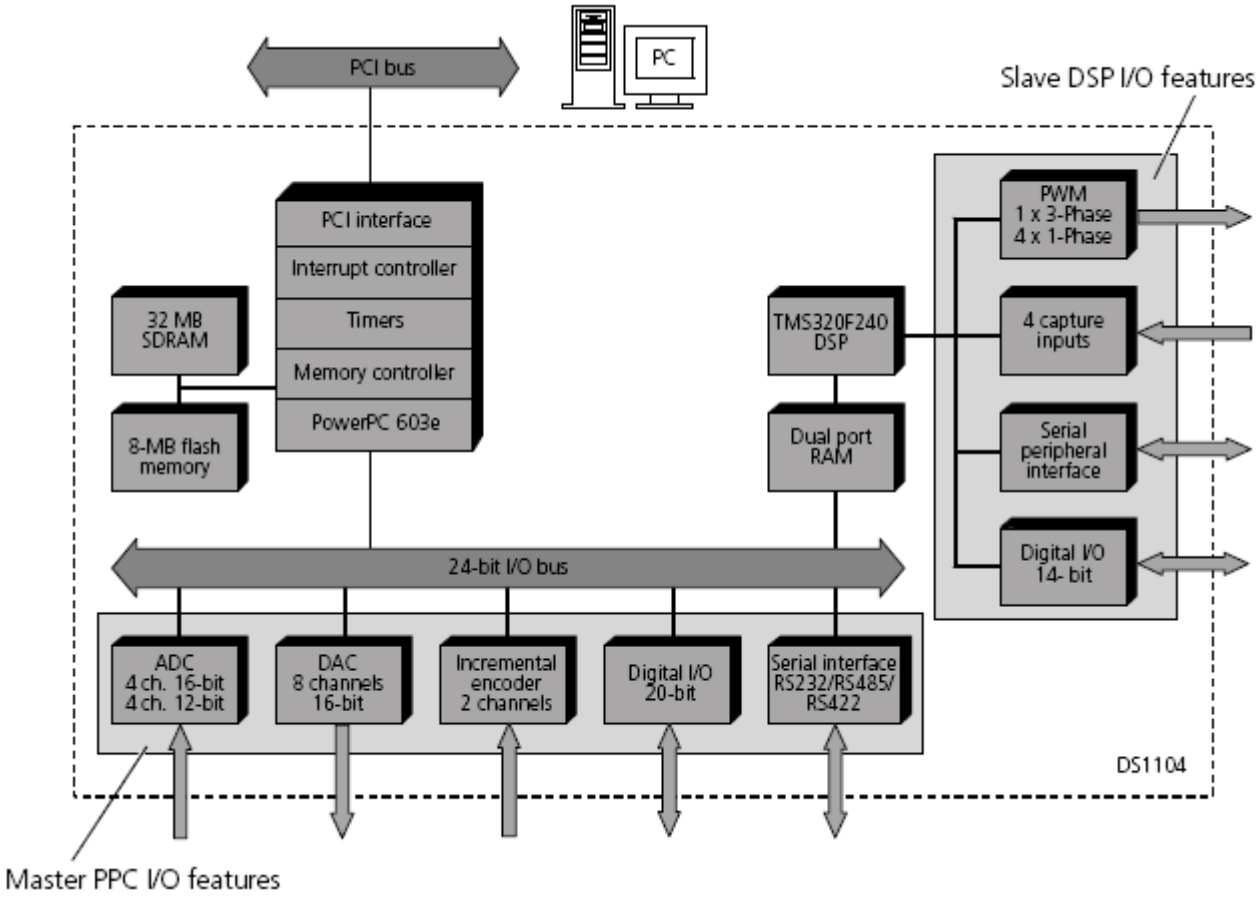

Fig.1. Architecture of DS1104

Fig.2. Picture of DS1104

An overview of the pertinent system specification includes:

- Four multiplexed inputs to 16-bit analog to digital converter (ADC), Four inputs with independent 12-bit ADCs, and an 8-output digital to analog converter (DAC).
- 2 incremental Encoders
- Onboard independent 64-bit floating point processor
- Onboard Slave DSP
- Onboard memory
- Other digital I/O capabilities

The system includes three main components:

- PCI development Board
- I/O breakout box
- Control Desk software and software protection dongle

The eight, 16 bit, D/A converters each with an output range of ±10V operates as voltage sources as their output impedance is close to zero, and each D/A channel can source or sink up to 5mA. The resolution, which represents the smallest difference between two output levels of the converter, is $20V/2^{16} = 0.305mV$. That is, the output voltage of the D/A converter can be varied from -10V to +10V in 0.305 mV steps.

The first four A/D channels share a single 16 bit A/D converter through an analog multiplexer. As a result, it is not possible to simultaneously sample analog signal on these four channels. The remaining four channels each have dedicated 12 bit A/D converters, allowing the simultaneous sampling of four analog input signals. The input range for all eight channels is ±10 V. The resolution of the 16 bit channels is 0.305mV, while the resolution for

the 12 bit A/D converters is 20 V/2^{12} = 4.9mV. The input impedance of each A/D channel is approximately 1 MΩ.

The 37 pin, 20 bit digital I/O can provide a maximum of ±5mA and +5V output while the slave DSP can provide a maximum of ±13mA and +5V output. The slave DSP can generate four 1-Φ PWM signals with variable duty cycle, frequencies and polarity. Also 3-Φ signal generation is possible. It is not simultaneously possible to generate both the 1-Φ and 3-Φ signals due to the pin conflicts. Slave DSP was used to generate signals from pins 5, 10, 11 in the ZVT SBC experiment.

Fig. 2 shows the dSPACE DS1104 Board. The D/A channels are located at the left hand side of the breakout panel, and are labeled DACH1 through DACH8. Immediately to the right of the D/A are ADCH1 through ADCH8 for the A/D converters, digital I/O and slave I/O PWM.

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1. A. K. Panda, Aroul K., "A Novel Technique to Reduce the Switching Losses in a Synchronous Buck Converter," *International Conference on Power Electronics, Drives and Energy Systems, IEEE PEDES,* pp. 1-5, 12 – 15 Dec. 2006.

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CITATIONS

For Publication No. 1

1. A Master's Thesis on "Analysis and Simulation of a 19V to 3.3V Synchronous Step-Down Controller Design", Zhou Jie, Department of Electrical Engineering, Datong University, Shanxi, China.

2. A Doctoral Thesis on "Power Management Schemes for Ultra Low Power Biomedical Devices", David Fitrio, School of Electrical Engineering, Victoria University, Melbourne City, Australia.