PHYSICAL DESIGN OF LOW POWER OPERATIONAL AMPLIFIER

A THESIS SUBMITTED IN PARTIAL FULFILLMENT

OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

VLSI Design and Embedded System

By

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ROLL No: 209EC2122

Department of Electronics and Communication Engineering

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Under the Guidance of

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CERTIFICATE

This is to certify that the thesis entitled, **"PHYSICAL DESIGN OF LOW POWER OPERATIONAL AMPLIFIER"** submitted by **Dipanjan Bhadra** in partial fulfillment of the requirements for the award of Master of Technology Degree in **Electronics & Communication Engineering** with specialization in **"VLSI Design and Embedded System"** at the National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

Date:

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Dedicated to:

My parents.

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ABSTRACT

A CMOS single output two stage operational amplifier is presented which operates at 3 V power supply at 0.18 micron (i.e., 180 nm) technology. It is designed to meet a set of provided specifications. The unique behavior of the MOS transistors in sub- threshold region not only allows a designer to work at low input bias current but also at low voltage. This op-amp has very low standby power consumption with a high driving capability and operates at low voltage so that the circuit operates at low power. The op-amp provides a gain of 20.4dB and a -3db bandwidth of 202 kHz and a unity gain bandwidth of 2.15MHz for a load of 5 pF capacitor. This op-amp has a $PSRR_{(+)}$ of 85.0 dB and a $PSRR_{(-)}$ of 60.0 dB. It has a CMRR (dc) of -64.4 dB, and an output slew rate of 12.465 v/μs. The power consumption for the op-amp is 1.18mW. The presented op-amp has a Input Common Mode Range(ICMR) of -1V to 2.4V. The op-amp is designed in the 180 nm technology using the umc 180 nm technology library. The layout for the above op-amp had been designed and the post layout simulations are compared with the schematic simulations.

The proposed op-amp is a simple two stage single ended op-amp. The input stage of the op-amp is a differential amplifier with an NMOS pair. The second stage of the op-amp is a simple PMOS common source amplifier. The second stage is used to increase the voltage swing at the output. The op-amp uses a -3v Vdd and a -3v Vss and consumes a power of around 0.6mW (as per post layout simulations).

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ABBREVIATIONS USED

Op-Amp	Operational Amplifier
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
CMR	Common Mode Range
CM	Common Mode
OTA	Operational transconductance amplifier

OPERATIONAL AMPLIFIER SPECIFICATIONS

- GAIN = 10 v/v.
- BANDWIDTH = 20 KHz.
- LOAD CAPACITANCE = 5pF.
- SLEW RATE = 10 v/μs.
- INPUT COMMON MODE RANGE = 1.2 v to 2.4 v.
- INPUT RANGE = 10 mv to 30 mv differential mode.
- MAXIMUM POWER DISSIPATION = 1 mw.
- CMRR = 50 dB.
- V_{dd} = 3 v.

Chapter 1

INTRODUCTION

1.1 MOTIVATION

The operational amplifier is undoubtedly one of the most useful devices in analog electronic circuitry. Op-amps are built with vastly different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Operational Amplifiers, more commonly known as Op-amps, are among the most widely used building blocks in Analog Electronic Circuits. Op-amps are used equally in both analog and digital circuits. [1,2]

Op-amps are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performing mathematical operations such as addition, subtraction, integration, differentiation etc . Generally an Operational Amplifier is a 3-terminal device. It consists mainly of an **Inverting input** denoted by a negative sign, **("-")** and the other a **Non-inverting input** denoted by a positive sign **("+")** in the symbol for op-amp. Both these inputs are very high impedance. The output signal of an Operational Amplifier is the magnified difference between the two input signals or in other words the amplified differential input. Generally the input stage of an Operational Amplifier is often a differential amplifier.[3]

Our aim is to create the physical design and fabricate a low power Op-amp .An ideal op-amp having a single- ended out is characterized by a differential input, infinite voltage gain, infinite input resistance and zero output resistance. In a real op-amp however these characters cannot be generated but their performance has to be sufficiently good for the circuit behavior to closely approximate the characters of an ideal op-amp in most applications. With the introduction of each new generation of CMOS technologies design of op-amps continues to pose further challenges as the supply voltages and transistor channel lengths scale down.[4-6,35]

1.2 SYSTEM OVERVIEW

For Op-amps used in many useful applications, rather a surprisingly large number of applications, the actual amplifier performance is closely approximated by an idealized amplifier model. Indeed quite frequently circuits are designed explicitly to insure acceptability of this approximation. And in other cases where the idealization is not a sufficiently accurate approximation nevertheless it often provides a starting point for an iterative process

towards a final design. Consider the 741 amplifier, an older but proven industry-standard device, which has a voltage gain exceeding 105 in normal operation. To cause an output voltage change between representative saturation voltage limits of ±15 volts, i.e., a full thirty-volt output change, the input voltage change involved is less than 0.3millivolt. Such a small voltage difference often may be neglected, i.e., approximated as zero, when compared to other circuit voltages with which it is associated in a KVL loop equation. [7-9]

This section briefly discusses the basic concept of op-amp. An amplifier with the general characteristics of very high voltage gain, very high input resistance, and very low output resistance generally is referred to as an op-amp. Most analog applications use an Op-Amp that has some amount of negative feedback. The Negative feedback is used to tell the Op-Amp how much to amplify a signal. And since op-amps are so extensively used to implement a feedback system, the required precision of the closed loop circuit determines the open loop gain of the system.[10]

A basic op-amp consists of 4 main blocks

a. Current Mirror
b. Differential Amplifier
c. Level shift, differential to single ended gain stage
d. Output buffer

The general structure of op-amp is as shown in figure 1 below:-

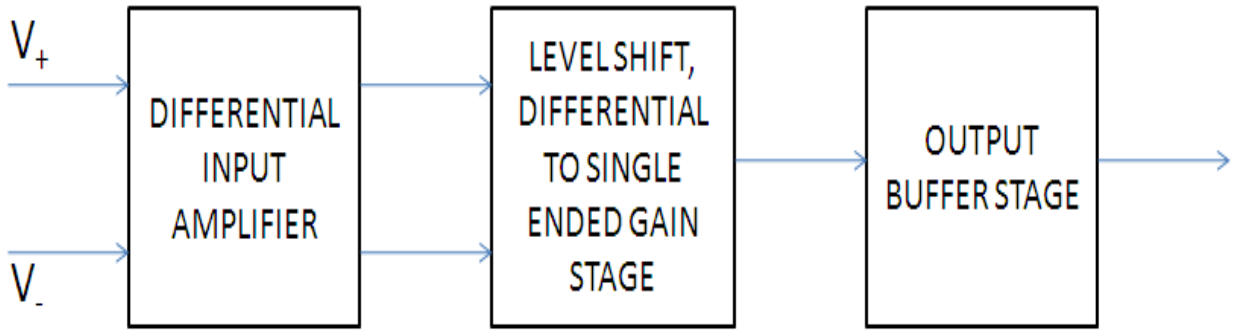

Figure 1 General Structure of op-amp

The first block is input differential amplifier, which is designed so that it provides very high input impedance, a large CMRR and PSRR, a low offset voltage, low noise and high gain. The

second stage performs Level shifting, added gain and differential to single ended converter. The third block is the output buffer. The output buffer may sometimes be omitted to form a high output resistance un-buffered op-amp often referred to as Operational transconductance amplifier or an OTA. Those which have the final output buffer stage have a low output resistance (Voltage operational amplifiers).[11-12]

1.3 APPLICATIONS

Operational amplifiers are used in so many different ways that it is not possible to describe all of the applications. However we may look into the use of op-amps for some simple yet widely used applications to form an idea of its mode of employment for various applications:

a. Summing Amplifier (Adder): The summing amplifier is a handy circuit enabling to add several signals together. The summing action of the circuit shown in Figure 2 is easy to understand. By keeping the negative terminal close to 0V (virtual ground) the op-amp essentially nails one leg of R1, R2 and R3 to a 0V potential. This makes it easy to write the currents in these resistors.

$I1 = V1 / R1; \quad I2 = V2 / R2; \quad I3 = V3 / R3$ ……... (1)

According to Kirchhoff's law, we get $I = I1 + I2 + I3$ and

$V_0 = - R_F (V1 / R1 + V2 / R2 + V3 / R3)$ ……... (2)

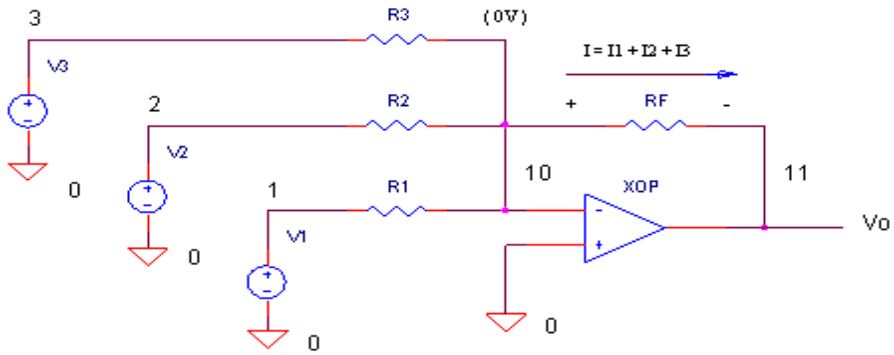

Figure 2: Op-amp summing circuit

b. Differential Amplifier: The difference op-amp produces the algebraic difference between two input voltages, which is shown in Figure 3. When RF=Rin and RA=RB the output of the amplifier can be given as $V_O = \frac{RA}{RF}(V_A - V_B)$. Thus the setup amplifies the difference of two voltages by a constant gain set by the used resistances.

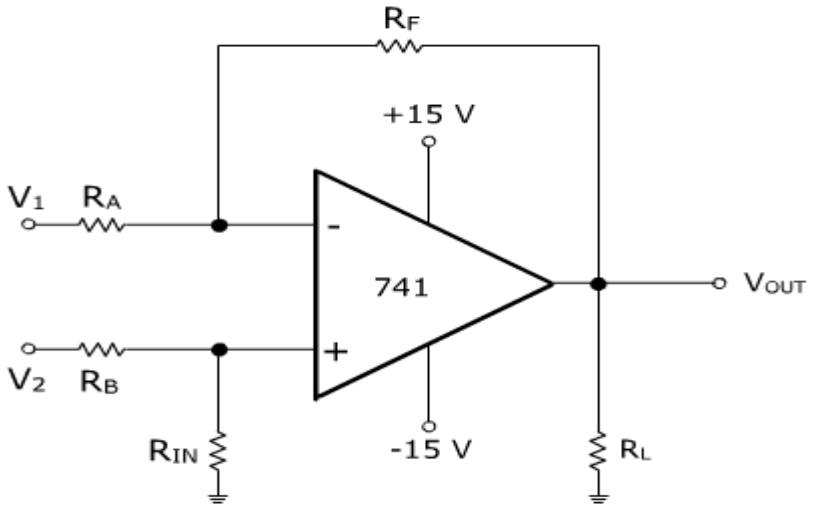

Figure 3: Op-amp differential circuit

Chapter 2

CURRENT MIRROR

2.1 INTRODUCTION

Current mirrors made by using active devices are widely used in analog integrated circuits not only as biasing elements but also as load devices for the amplifier stages. The extensive use of current mirrors for biasing in analog circuits stems from the fact that it provides superior insensitivity of circuit performance to variations in power supple and temperature variations. More over for small bias current requirements often current mirrors are favored over resistors as they are more economical in terms of die area. The high incremental resistance of the current mirror results in high voltage gain at low power-supply voltages. These apart the current mirrors and current sources find other applications in analog design as well.

A current mirror is a electronic circuit designed to regulate and control the current through one active device depending on the current through another active device. It also needs to keep the output current constant irrespective of the output load. The controlling current or the current depending on the value of which the output current is determined is often a varying signal current. Practically, an ideal current mirror can also be considered to be an ideal current amplifier. The current mirror is used in analog circuits to provide bias currents and active loads. A current mirror is characterized by three main specifications. One of them is the current level it produces. The AC output resistance is the second. The AC output resistance determines how much the output current varies with the voltage applied to the mirror. The third specification is the minimum voltage that needs to be maintained across the output terminal of the current mirror for it to work properly. This minimum voltage that is to be applied across the output transistor of the mirror to keep it in active mode dictates the voltage specification for the current mirror. This voltage range in which the mirror works is called the compliance range and the voltage beyond which the current mirror performance is no longer satisfactory is called the compliance voltage. A number of secondary performance issues with mirrors temperature stability also dictates the design procedure.

In case of an ideal current mirror the output current is a product of the input current and a desired voltage gain. A unity gain causes the input current to be reflected at the output. Ideally the current mirror gain has to be independent of input current frequency and the output current has to be independent of the voltage at the output node. In practice though real current mirrors suffer from many deviations from the ideal behavior. For instance neither is the gain independent of the input frequency nor does the current mirror output current stays independent of voltage variations at the output node.[13,14]

2.2 CURRENT MIRROR

The basic current mirror implemented using MOSFET transistors is as shown in Figure 4. In the figure 4 for the proper functioning of the device we make assume that both transistors M1 and M2 operate in saturation or active region. In this circuit, there is a direct relation between I_{REF} and I_{OUT},

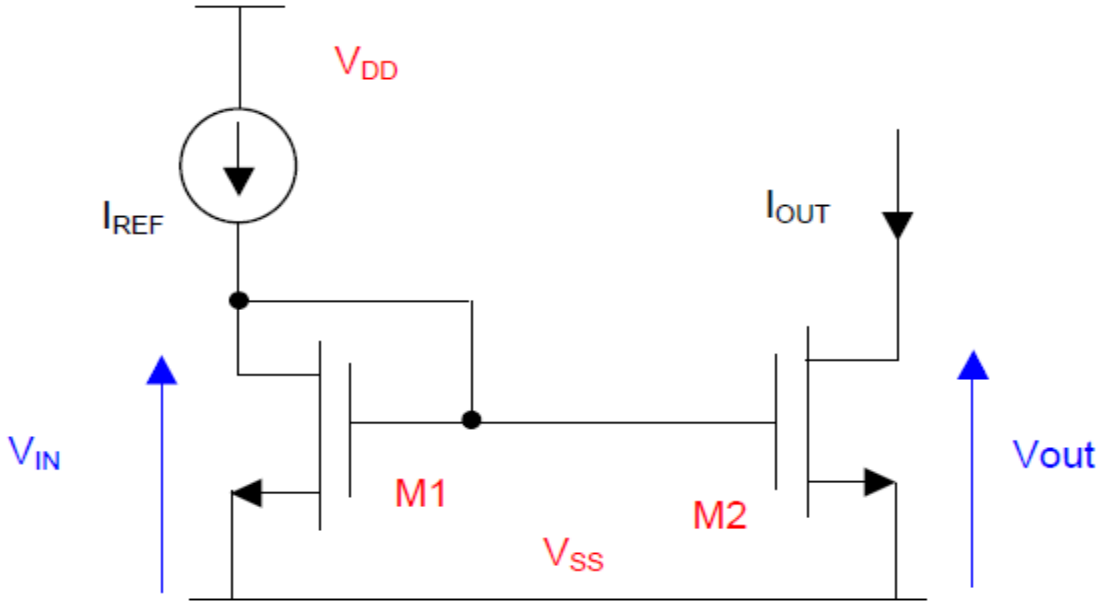

Figure 4: Basic Current Mirror

The drain current of a MOSFET I_{DRAIN} is determined not only by the voltage across the gate and source terminals but also the drain-to-gate voltage of the MOSFET. Thus the drain current can be given by $I_D = f\ (V_{GS},\ V_{DG})$. This relationship can be derived from the functionality of the MOSFET device. The drain-to-source voltage is expressed as: $V_{DS}=V_{DG}+V_{GS}$.

With this substitution, it is an approximate form for function $f\ (V_{GS},\ V_{DG})$:

$$I_d = f(V_{GS},V_{DS}) = \frac{1}{2} K_p(\frac{W}{L}) (V_{GS} - V_{th})2(1 + \lambda V_{DS})$$

$$= \frac{1}{2} K_p(\frac{W}{L}) (V_{GS} - V_{th})2(1 + \lambda(V_{DG}+ V_{GS}))..... (3)$$

Here K_p of the transistors depends on the technology of fabrication, W/L is the ratio of width to length of the transistor, V_{GS}, V_{th}, and V_{DS} is the gate-source voltage, the threshold voltage and the drain source voltage respectively, λ is the channel length modulation constant of the

transistors.

Now for the transistor M_1 of the mirror circuit in figure 4, $I_D = I_{REF}$. Now for the circuit the reference current I_{REF} is a known current of constant value independent of supply voltage variations. We may use a resistor as shown, or even a "threshold-referenced" or "self-biased" current source to provide this constant reference current.

Now as the drain and gate is shorted $V_{DG}=0$ for transistor M_1, so the function for the drain current of M_1 can be given by $I_D = f(V_{GS}, V_{DG}=0)$, thus I_{REF} depends solely on the gate to source voltage, thus the current I_{REF} determines the value of V_{GS}.

Now as evident from the circuit the same VGS is applied to transistor M2. Thus if M1 and M2 are matched that is have identical channel length, width, threshold voltage *etc* and we apply $V_{DG}=0$ to M2 too, then the current I_{OUT} depends only on V_{GS} for M2 too and thus $I_{OUT} = I_{REF}$; that is, the output current and the reference current of a current mirror are equal when $V_{DG}=0$ for the output transistor, and both transistors are matched with identical W/L.

2.3 OUTPUT RESISTANCE

Unlike the ideal current mirror practical current mirrors have finite output resistance that depends on the channel length modulation of the transistors of the output stage:

$$R_N = r_o = \frac{1/\lambda + VDS}{ID} \quad \text{..... (4)}$$

Where λ is the channel-length modulation index and VDS is the drain-to-source voltage.

2.4 COMPLIANCE VOLTAGE

When analyzing the working of the current mirror it was assumed that the transistors are operating in saturation, thus the minimum output voltage required for the current mirror to behave correctly is determined by the minimum drain to source voltage that needs to be applied to the output stage transistors to keep them in saturation thus V_{CV} can be given as:

$$V_{CV} = V_{GS}(\text{for } I_D \text{ at } V_{DG} = 0V) = f^{-1}(I_D) \text{ with } V_{DG} = 0 \quad \text{..... (5)}$$

A current mirror is a electronic circuit designed to regulate and control the current through one active device depending on the current through another active device, keeping the output current constant independent of the load. The controlling current or the current depending on the value of which the output current is determined is often a varying signal current. Practically, an ideal current mirror can also be considered to be an ideal current amplifier. The current mirror is used in analog

circuits to provide bias currents and active loads. M1 has the drain and gate terminals connected together. This forces M1 to operate in the saturation mode in this particular circuit if ID $\neq 0$. In this mode

$$I_{D1} = \frac{1}{2} K_{n1}' \frac{W1}{L1}(V_{GS} - V_{t1})^2 \quad \ldots\ldots (6)$$

With a zero gate current, $I_{REF} = I_{D1}$

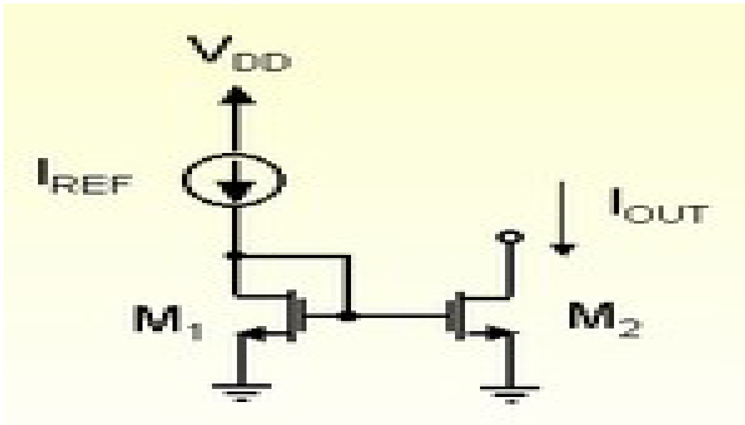

Figure 5:NMOS Current Mirror

Where we can see easily from the below circuit [Figure 6] that

$$I_{REF} = (V_{DD} - V_{GS} - (-V_{SS}))/R_{REF} \quad \ldots\ldots (7)$$

Now we will assume that the two MOSFETS in the circuit have the same V_{GS} .since they are shorted at their gates and their sources are both connected to the V_{SS} or ground terminal(V_{DD} in case of PMOS transistors of Figure 7) Consequently the drain current in the second transistor is

$$I_{D1} = \frac{1}{2} K_{n2}' \frac{W2}{L2}(V_{GS} - V_{t2})^2 \quad \ldots\ldots (8)$$

If these two transistors are perfectly matched but they are perhaps fabricated with different channel dimensions, then $K_{n1}' = K_{n2}'$ and $V_{t1} = V_{t2}$ so that by comparing the above equations we obtain

$$I_{D2} = ((W_2/L_2) / (W_1/L_1))\, I_{D1} = ((W_2/L_2) / (W_1/L_1))\, I_{REF} \quad \ldots\ldots (9)$$

The MOSFET current mirror using resistor R_{REF} is shown in Figure 6 for NMOS. In this NMOS current mirror shown above, M2 acts as a current sink since it pulls current $I_0 = I_{D2}$ from the load, which in our case will be the amplifier circuits of the op-amp.

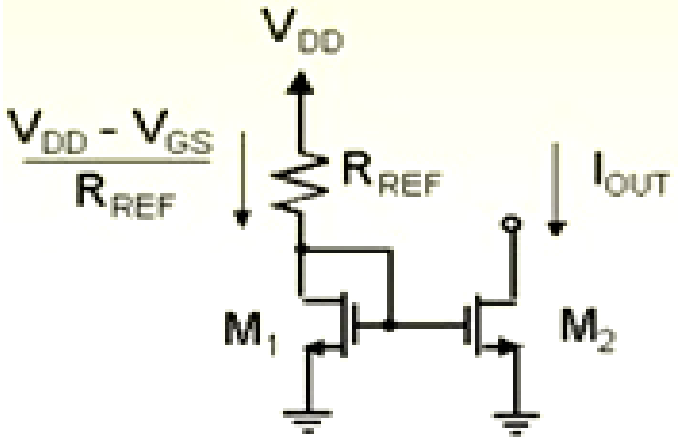

Figure 6: MOSFET Current Mirror using resistor R_{REF}

By using PMOS, this current mirror circuit [Figure 7] is constructed as shown in the figure. The source of the PMOS are connected to VDD

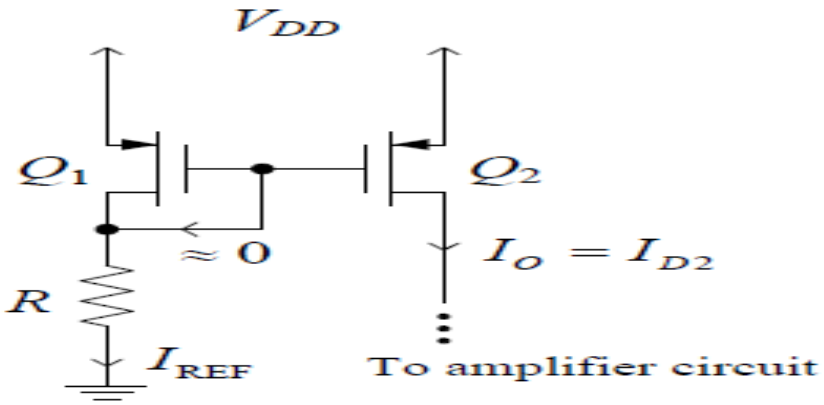

Figure 7: PMOS Current Mirror

Here Q2 acts as a current source since it pushes current $I_0 = I_{D2}$ into the load.

2.4 PRACTICAL APPROXIMATIONS

During small-signal analysis the current mirror is approximated by an equivalent Norton impedance whereas for large signal analysis it is considered to be a simple current source. However, the current mirror deviates from the characteristics of an ideal current source in many ways:

- Unlike the ideal current source which has infinite AC impedance a practical mirror has finite impedance.
- The output current of a current source is constant irrespective of output voltage and there is no minimum compliance voltage requirement for it to function properly. Also

even past the compliance range the current mirror output varies with the variation in voltage at the output terminal. The Norton equivalent circuit of a current mirror output consists of a resistance R_0 in parallel with the current source dependent on the input current. This resistance R_0 for the variation in current due to variation in voltage across output terminals and also affects directly the performance of many circuits that use a current mirror. Though it is not possible to build a real current mirror with infinite R_0 the goal is to make it very large.

- The current source output is independent of frequency whereas the parasitic capacitances of the transistors causes the current mirror output to vary with frequency.
- Unlike the ideal source which has no sensitivity to real-world effects like noise, power-supply voltage variations and component tolerances in real life the gain of the current mirror varies due to variation in these parameters. Variations may be systematic or random: systematic error accounts for the errors that occur even when all components are perfectly matched and has to be calculated for each current mirror. Random error is the error caused by unintended mismatch between matched elements.

The current mirror schematic is as shown in Figure 8 below:-

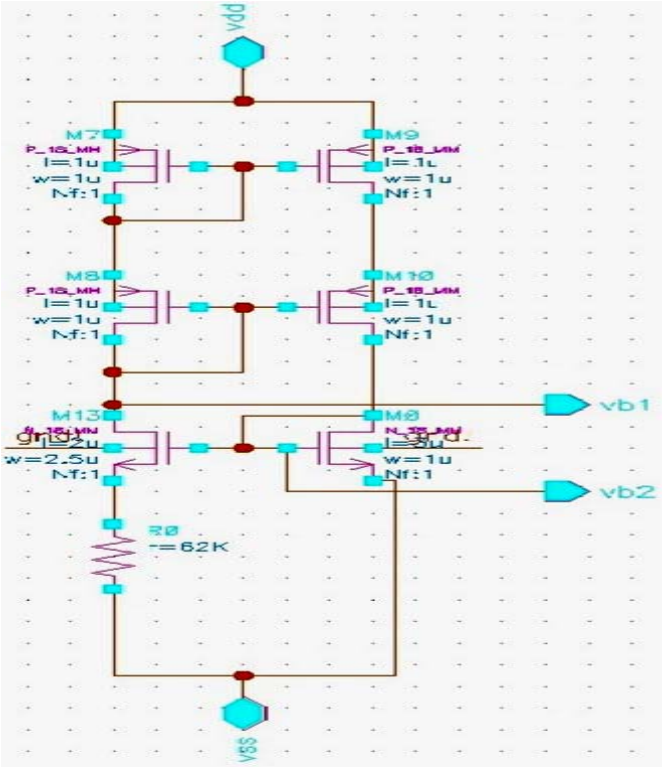

Figure 8: Schematic of a Current bias circuit

Symbol view of the bias circuit and the current mirror circuit :

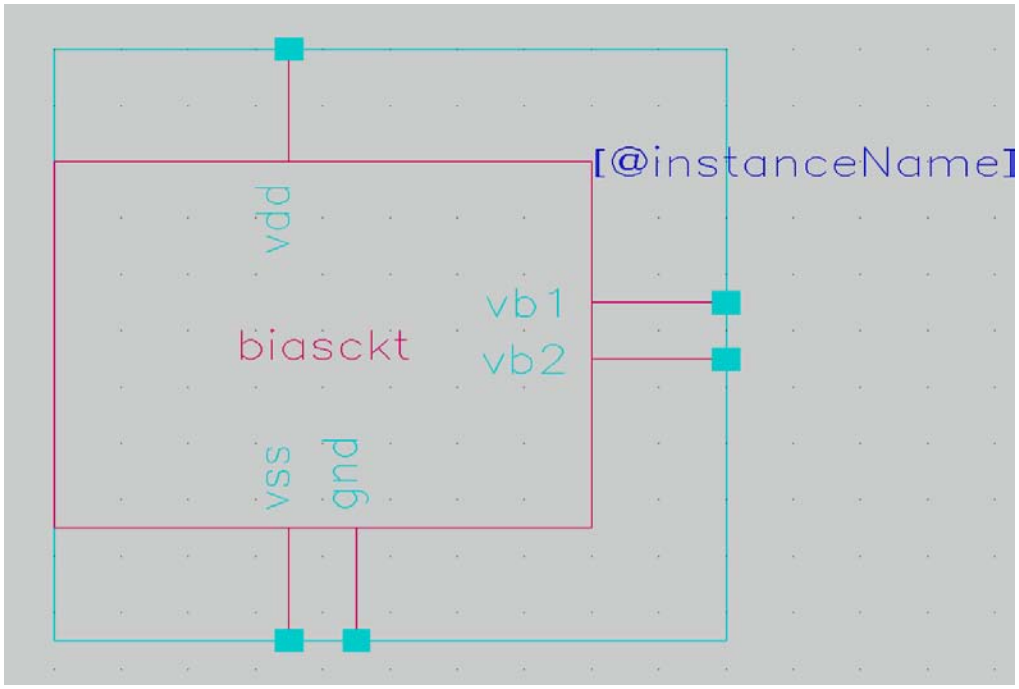

Figure 9: Bias Circuit Symbol View

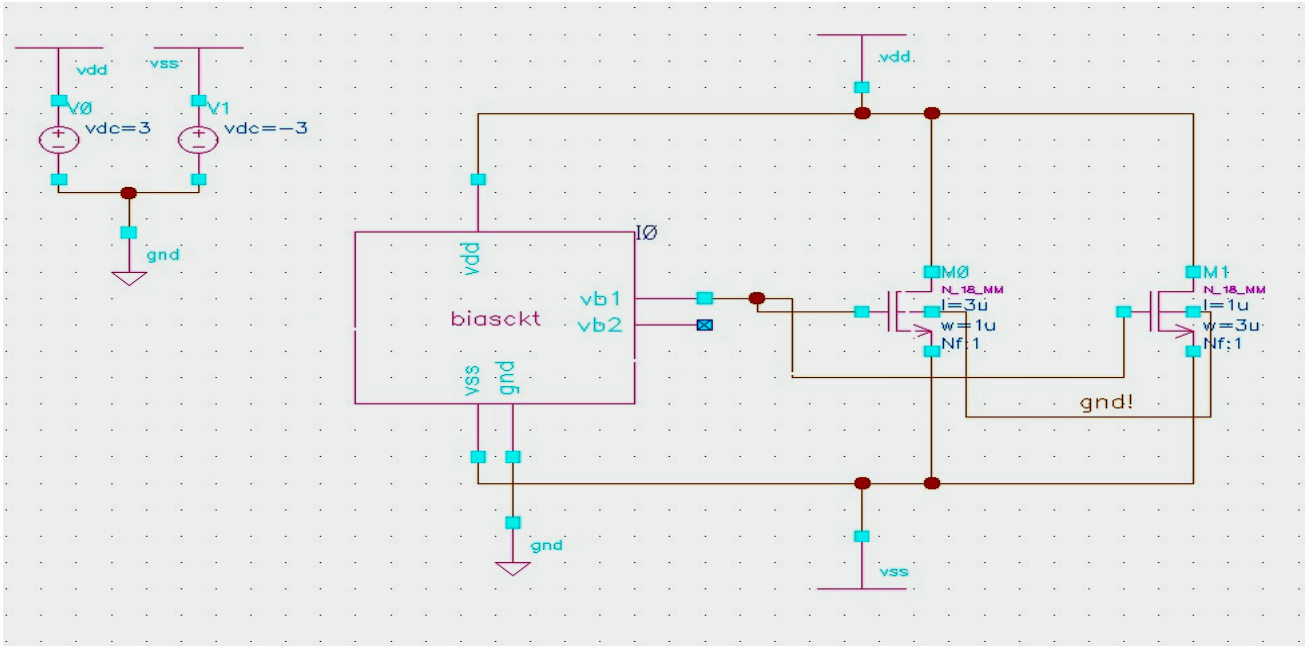

Figure 10: Current Mirror Circuit

Chapter 3

DIFFERENTIAL AMPLIFIER

3.1 INTRODUCTION

The differential amplifier is an essential building block in modern IC amplifiers. Many electronic devices use differential amplifiers internally. A differential amplifier is a type of electronic amplifier that multiplies the difference between two inputs by some constant factor (the differential gain). The output of an ideal differential amplifier is given by:

$$V_{out} = A_d (V_{in}^{+} - V_{in}^{-}) \quad \text{.....(10)}$$

Where V_{in}^{+} and V_{in}^{-} are the input voltages and A_d is the differential gain. In ideal op-amps though the gain is not exactly equal for the two inputs. This means, for an instance, that if V_{in}^{+} and V_{in}^{-} will be equal then the output may not be zero as it should be for the ideal case. Therefore a more practical expression for the output of an amplifier needs to include another term

$$V_{out} = A_d(V_{in}^{+} - V_{in}^{-}) + A_c((V_{in}^{+} + V_{in}^{-})/2) \quad \text{.....(11)}$$

Where A_c is the common mode gain of the amplifier and

A_d is the differential mode gain of the amplifier.

3.2 DIFFERENTIAL AMPLIFIER

When using a differential amplifier it is desirable to null out noise and bias voltages that appear on both inputs so a low common-mode gain is usually considered good. The common-mode rejection ratio is usually defined as the ratio between differential-mode gain and common-mode gain and it characterizes the efficiency of the amplifier in effectively refusing voltages that are common to both inputs from affecting the output. Common-mode rejection ratio (CMRR):

$$CMRR = A_d/A_c \quad \text{..... (12)}$$

In a perfectly symmetrical differential amplifier, Ac is zero and the CMRR is infinite. It might be noted here that a differential amplifier is used more often than the single input one, when one input of the differential amplifier is grounded it acts as a single; by grounding one input of a differential amplifier, a single-ended amplifier results. An operational amplifier is basically a differential amplifier with very high differential-mode gain along with very high input impedances and rather low output impedance. At times some kinds of differential amplifiers are created by connecting smaller differential amplifiers and other components. [15, 16, 37]

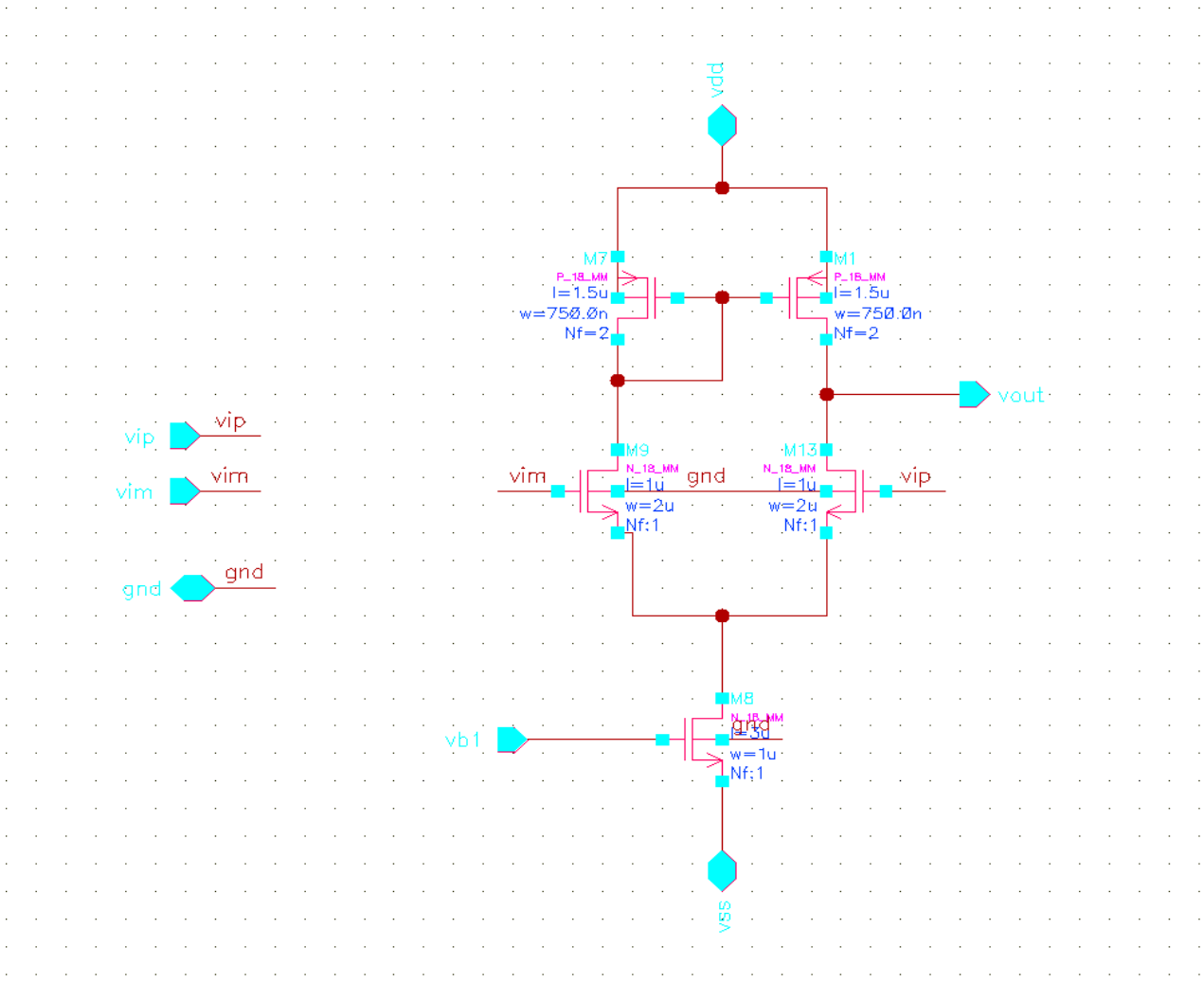

Figure 11: Differential Amplifier Schematic

Many a analog circuits use differential amplifiers as the input amplifier stage. The input amplifier stage is supposed to account for the high input impedance, large common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR), low dc offset voltage and noise and much of the op-amps voltage gain. The output signal of the input stage is much larger than the input one is hence much less sensitive to noise and offset voltage effects in the later stages. Since the circuit operates in a differential mode, it can provide high differential gain along with low common-mode gain and hence a large CMRR. The differential configuration also helps in achieving a large PSRR, since variations of V_{DD} are, to a large extent, canceled in the differential output voltage V01 – V02.

The NMOS current source is added to the circuit to make the maximum and minimum

level of the output independent of the input common mode voltage. For proper operation of the differential amplifier all transistors including the one forming the current source are considered to operate in saturation. The differential pair is also matched and in an ideal case the two input nodes are considered to have same resistance. We also assume the current source "I" is ideal, that is, its internal conductance g is zero. The differential gain is the same as for a simple inverter; however the stage provides also a rejection of common-mode signals and of noise in the power supplies VDD and VSS, all of which are cancelled by the differential operation of the stage. The low frequency small signal equivalent circuit of the differential amplifier stage can be used to calculate the gain of the differential amplifier circuit. The gain of the differential amplifier circuit is given by

$$A_V = g_m R_D \quad \text{.....(13)}$$

Here gm is the transconductance of the transistors in the differential pair.

The differential pair can be looked at as two single transistor amplifiers in parallel to allow it the capability to reject disturbing common mode signals and it is thus the basis of all fully-differential circuits. Let us now take a look at the DC operation of the circuit. When the voltage at the gate of the two transistors forming the differential pair is the same they two operate with the same V_{gs} and hence they have the same current. Since the sum of the currents flowing through them is fixed by the current source we assume each current to be "$\frac{I_{SS}}{2}$" and we assume that the voltage drop across the two PMOS transistors is the same and hence the voltage at the two output terminals of the differential amplifier is the same. Thus we have zero differential output for zero differential input. Now consider the left gate voltage increases by V' and the right gate voltage decreases by V'. now increase in the gate voltage means increase in the current flowing through it but the sum of current flowing through the two transistors of the differential pair is fixed and equal to I_{SS} so the increase in current of one means decrease by the same amount in the current of the other. Let this change in current be i_c and can be given by

$$I_c = g_m \frac{(vgs1 - vgs2)}{2} \quad \text{.....(14)}$$

Where $(v_{gs1}\text{-}v_{gs2})$ is the differential input.

Now the output of the two output terminals can be given by

$$V_{01} = V_{equi} + i_c R_d \quad \text{.....(15)}$$

$$V_{02} = V_{equi} - i_c R_d \quad \text{.....(16)}$$

Thus the differential output is

$$V_{od} = 2\, i_c R_d \quad \text{..... (17)}$$

Thus the gain can be given by

$$A_{d,\,m} = ((V_{01} - V_{02})/(V_{gs1} - V_{gs2}))$$

$$\text{»} A_V = -g_m R_D \quad \text{..... (18)}$$

Though the offered current gain is the same as a single transistor amplifier it provides the additional advantage of high CMRR and PSRR.

Finally the differential amplifier symbol is shown in Figure 13 below:-

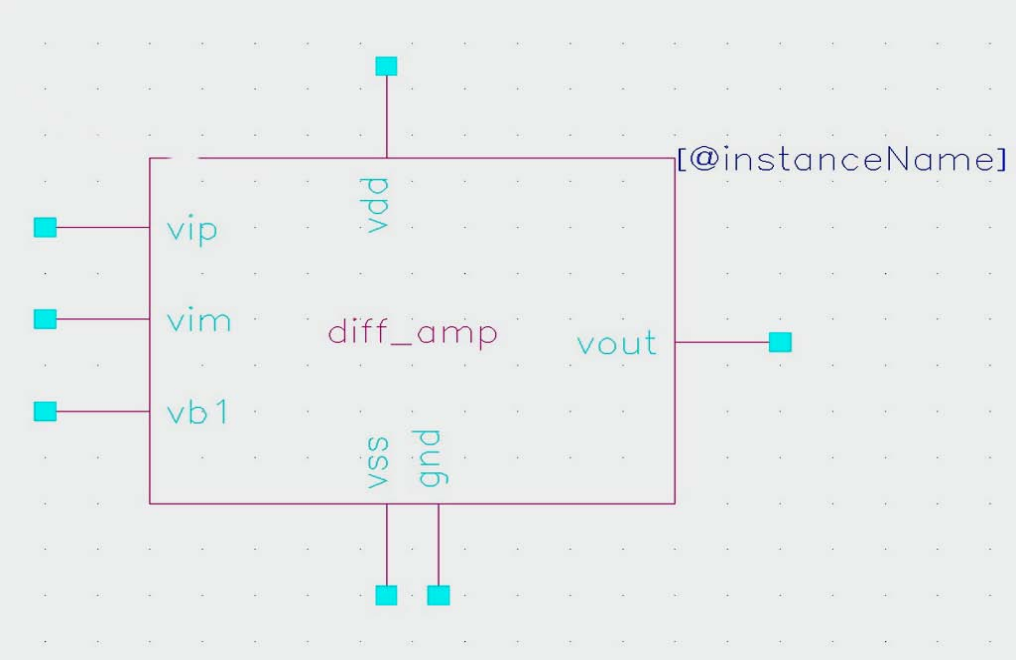

Figure 12: Diff-Amp Symbol View

Chapter 4

COMMON SOURCE AMPLIFIER STAGE

4.1 INTRODUCTION

A single stage operational amplifier that is a differential pair allows the direct flow of the small signal current produced by the input differential pair through the output impedance. This limits the gain of these topologies to the product of the input pair transconductance and the output impedance. Though the gain of such a circuit may be improved through the use of cascading in such circuits the output swing of the op-amp is further limited due to addition of transistor stages. Often these limitations need to be addressed as the gain and or voltage swing available from a cascade amplifier is not adequate for the required applications. In such cases we resort to two stage op-amps as they deal with the gain and output swing limitations. In such a configuration generally the first stage provides a high gain while the later provides a high swing. The two stage op-amps are thus more effective than the cascade op-amps as they isolate and deals separately with the gain and swing requirements.

Though various configurations can be used for both the first and second stage to implement the op-amp the first stage is most generally a differential amplifier and the second stage is implemented by employing a simple common source amplifier as it allows maximum voltage swing at the output. To increase the gain of the op-amp we may even resort to the use of cascode devices in the first stage and though the voltage swing at the input of the second stage of the second stage will be low the presence of the common source stage prevents the voltage drop across the cascode stage from affecting the output voltage swing.

The gain of such an op-amp is also greater than a single stage. Suppose when the first stage and second stage produces a gain of A_{v1} and A_{v2} respectively the op-amp produces a gain of (A_{v1} x A_{v2}). Thus both in terms of gain and voltage swing the two stage op-amp is advantages. However use of every stage contributes at least one pole in the open-loop transfer function thus it is difficult to guarantee stability of a multi-stage op-amp.

4.2 COMMON SOURCE AMPLIFIER

The principle of operation of a common source amplifier is based on the simple fact that by virtue of its transconductance, a MOSFET converts a variation in its gate to source voltage into a small-signal drain current which can be made to pass through a resistor to generate an output voltage.

For our design we choose a PMOS common source amplifier in the second stage. The reason behind choosing a PMOS common source amplifier is to obtain higher output swing as also more

gain while at the same time keeping the flicker noise at its minimum. PMOS amplifiers are believed to generate lesser flicker noise than NMOS amplifiers because of the lesser mobility of holes. Let us now consider a pmos common source amplifier:

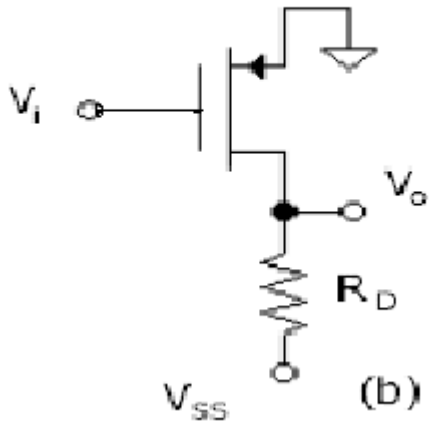

Figure 13: PMOS Common Source Amp.

Now for the given circuit as V_i decreases from zero the transistor is off and V_O is V_{ss}. Now as V_i approaches V_t the transistor is turned on. The transistor drives current through R_D and pulls up the output voltage. If V_{ss} is sufficiently negative the transistor turns on in saturation and therefore the output voltage V_O can be given as

$$V_O = -V_{ss} + \frac{1}{2} R_D \mu_p C_{ox} \frac{W}{L} (V_{in} - V_t)^2 \quad \text{.....(19)}$$

Where channel length modulation is neglected. As V_i decreases further , V_o rises more and the transistor continues to operate in saturation until V_i exceeds V_o by V_t . past this point the transistor goes into the triode region.

As the transconductance drops in the triode region the transistor is made to operate in the saturation region. Now using equation (19) we obtain the gain for a common source amplifier as

$$A_v = \frac{dv_{out}}{dv_{in}} = -g_m R_D \quad \text{.....(20)}$$

Even though this gain is derived for small signal operations, it can predict certain effects produced by the circuit when it senses a large signal swing at its output pretty accurately. Since the gm of the transistor itself is a function of the input signal given by the equation

$$g_m = \mu_p C_{ox} \frac{W}{L} (V_{in} - V_t) \quad \text{.....(21)}$$

the gain of the circuit changes substantially if there is a large change in the input of the circuit. Thus it is evident that the gain of the circuit varies substantially with the signal swing when it operates in the large signal mode. This nonlinearity generated by the dependence of the gain on the signal level is an undesirable effect.

4.3 COMMON SOURCE STAGE WITH CURRENT SOURCE LOAD

Now as evident from the gain of the amplifier increasing the load impedance of the Common Source stage allows us to obtain a large voltage gain in a single stage. But however using a resistor or a diode connected load to increase the load resistance also limits the voltage swing of the circuit. Thus the most practical choice for replacing the load of a cs stage is a current source. In this circuit both the transistors operate in saturation.

The circuit is shown here:

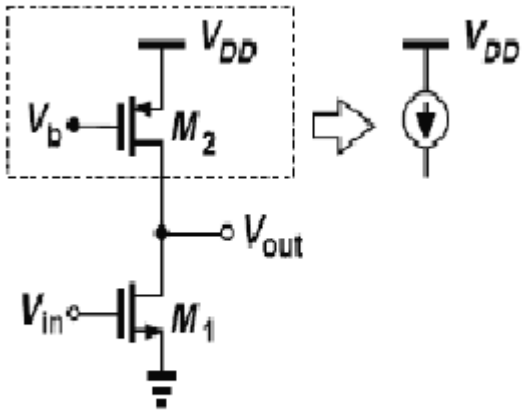

Figure 14: Common Source stage with current source load

Since the total impedance that appears in this circuit at the output node is given by

$$R_{equivalent} = (ro1 \parallel ro2) \quad \text{.....(22)}$$

The gain for the amplifier now becomes

$$Av = - gm (ro1 \parallel ro2) \quad \text{.....(23)}$$

The advantage of the current source over the resistor lies in the fact that the output impedence of M2 and the minimum voltage drop across it are less strongly coupled that the corresponding values of a

resistor. The current source provides the additional flexibility to the design of being able to vary the overdrive voltage of M_2 and hence the voltage swing at the output o the amplifier by simply varying the width of the transistor. If r_{o2} is not sufficiently large the length and width of the device can be varied to obtain the a smaller λ while maintaining the same overdrive voltage. Though the flexibility comes at the price of the large capacitance introduced by M_2 at the output node.

4.4 TRADEOFFS:

The magnitude of the gain can be increased by increasing W/L for the common source transistor or by increasing the voltage drop across the load or by decreasing the amplifier drain current. As evident from the above discussion this brings us to tradeoff between gain bandwidth and voltage swing. While increasing the device size means dealing with a greater capacitance value a higher voltage drop across the load means less output voltage swing. If we try to increase the gain by reducing Id while keeping the voltage drop across the load constant, the resistance must increase which will lead to a greater time constant at the output node.

The schematic for the common sourse amplifier stage used is given here

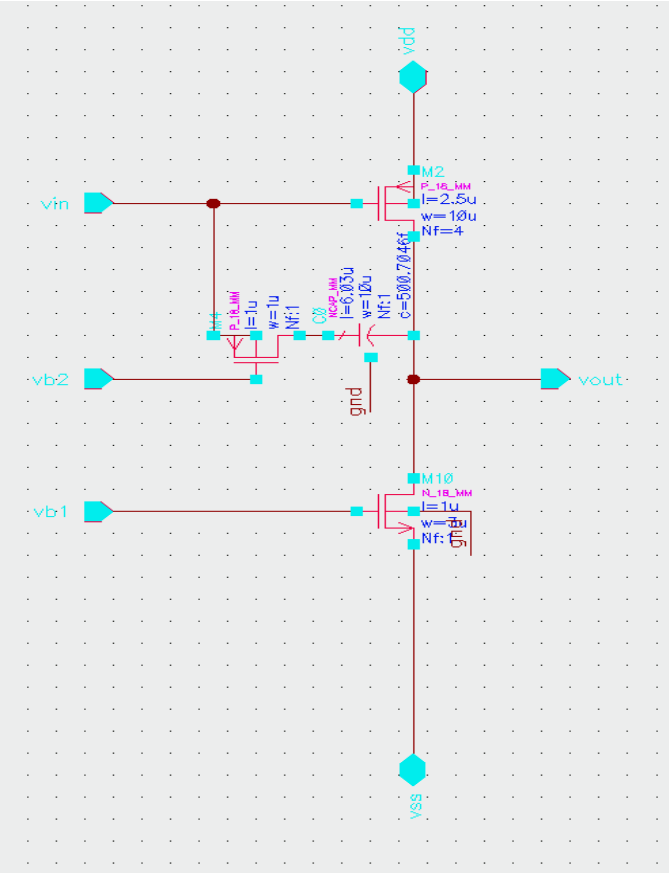

Figure 15: Common Source amplifier stage

Chapter 5

OPERATIONAL AMPLIFIER

5.1 INTRODUCTION

An operational amplifier is often called an op-amp. It is a DC-coupled differential input voltage amplifier with an rather high gain. In most general purpose op-amps there is a single ended output. Usually an op-amp produces an output voltage a million times larger than the voltage difference across its two input terminals. For most general applications of an op-amp a negative feedback is used to control the large voltage gain. The negative feedback also largely determines the magnitude of its output ("closed- loop") voltage gain in numerous amplifier applications, or the transfer function required. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration. An ideal opamp is characterized by a very high input impedance (ideally infinite) and low output impedance at the output terminal(s) (ideally zero).to put it simply the op- amp is one type of differential amplifier.

5.2 OPERATIONAL AMPLIFIER

The general operational amplifier symbol is as shown in Figure 16 below:-

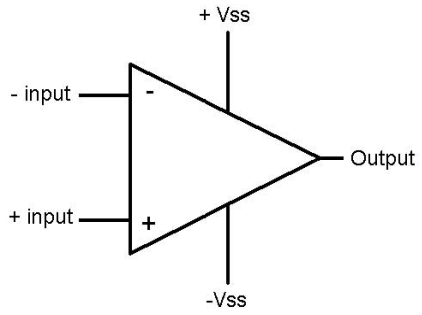

Figure 16: General operational amplifier

An ideal Operational Amplifier is a 3-terminal linear device. It consists of two input terminals with very high impedance. Basically the Operational Amplifier output signal is nothing but the difference of the two input signals being applied at the high impedance terminals magnified by a constant gain. [17-18]

Thus for an ideal op-amp the input signal is almost always a differential signal and hence a differential amplifier is generally used as the input stage of an Operational Amplifier. The op-amp block diagram shows a common op-amp symbol with two inputs marked by + and – and

an output. The terminals V_{DD} and V_{SS} are the terminals for the supply voltages. In general the op-amp is used with dual power supplies. The V_{SS} terminal is made negative to drag down the source potential of the NMOS transistors used in the design to a negative potential. This ensures that the op-amp can be used for wider range of differential inputs. For ideal operation of the op-amp circuit it all transistors are supposed to function in saturation. The negative power supply at V_{SS} ensures even if one of the inputs is grounded the differential pair action as the input stage of the op-amp is in saturation. The output voltage, V_{out} of the amplifier is given by the difference between the two input signals applied to the differential amplifier multiplied by some constant gain determined by the specs of the designed system. For designing an ideal op-amp many considerations are made. One those considerations involve the use of perfectly matched transistors for the input differential pair as well as at the load of the differential pair. The use of current mirrors in the op-amp circuit also creates the need for generation of matched transistors.

Ideal Operational Amplifiers have in general one output (although there are op-amps with differential outputs as well as many applications have need for them) of low impedance which is mostly referenced to a common ground terminal. In an ideal case the output of the op-amp should ignore any common mode signals in the input, i.e., if signals of identical dimensions are applied to both the inputs the output should be zero ideally. However, in practical amplifiers the output always varies slightly for the common mode input and this change of the output voltage with respect to variations in the common mode input voltage is measured for an op-amp by virtue of its Common Mode Rejection Ratio or CMRR.[26]

Most Operational Amplifiers have a characteristic high open loop DC gain. By the application of negative feedback in some form often we easily construct an operational amplifier circuit that has a very accurate gain characteristic which depends solely on the feedback used in the circuit. An operational amplifier output is independent of any common potential applied across both of its high impedance input terminals and the output depends only on the difference between the voltages. If both input terminals of an op-amp are at same potential the resultant output for an ideal op-amp will be zero. The gain of the Operational Amplifiers is commonly referred to as the Open Loop Differential Gain, and is denoted by the symbol (A_o).[26]

5.3 EQUIVALENT CIRCUIT OF AN OP-AMP

An equivalent op-amp circuit is shown in the circuit below. It consists of two inputs

often referred to as the inverting and non-inverting inputs. The input resistance or rather impedance is referred in the diagram as Z_{in} and the output impedance is given by Z_{out}. This is the basic block diagram of a op-amp which generally has a single output.

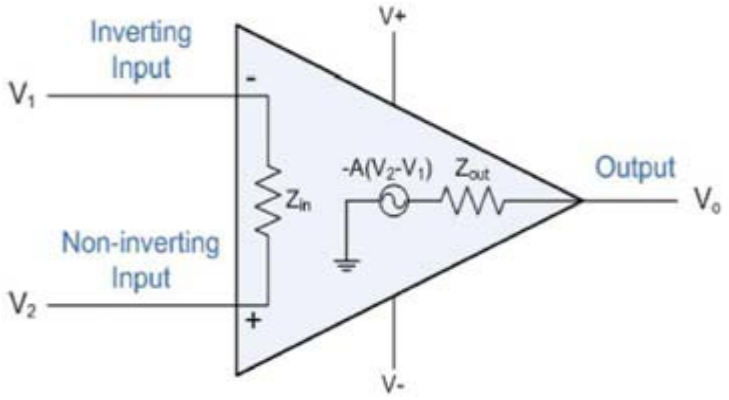

Figure 17: Equivalent Circuit for ideal operational amplifier

5.4 IDEALIZED CHARACTERISTICS

(a) Voltage Gain, (A) **Infinite**

(b) Input impedance (Z_{in}) **Infinite**

(c) Output impedance, (Z_{out}) **Zero**

(d) Bandwidth, (BW) **Infinite**

(e) Offset Voltage, (V_o) **Zero**

From the idealized characteristics above it is important to notice that the input resistance of the op-amp in an ideal case is infinite, so for an ideal op-amp no current flows into either input terminal. This is called the current rule. The differential input offset voltage is also zero and this is the voltage rule. These two properties should be noted carefully as they predict and help us understand the workings of the amplifier and in turn aid the analysis and design of operational amplifier circuits.

However, the infinite gain or bandwidth that characterizes an ideal operational amplifier is seldom found in a real Operational Amplifiers like the widely used uA741. Typically the "Open Loop Gain" of a real operational amplifier is defined as the amplifiers output amplification in absence of any external feedback signals. In common real operational amplifier there is an open loop gain of about 100dB at DC (at a frequency of zero Hz). This output gain is not however frequency independent and is found to gradually decreases at higher frequencies till it reaches "Unity Gain" or 1, at about 1-4MHz and this is also shown in following figure.

5.5 OPEN LOOP FREQUENCY RESPONSE CURVE

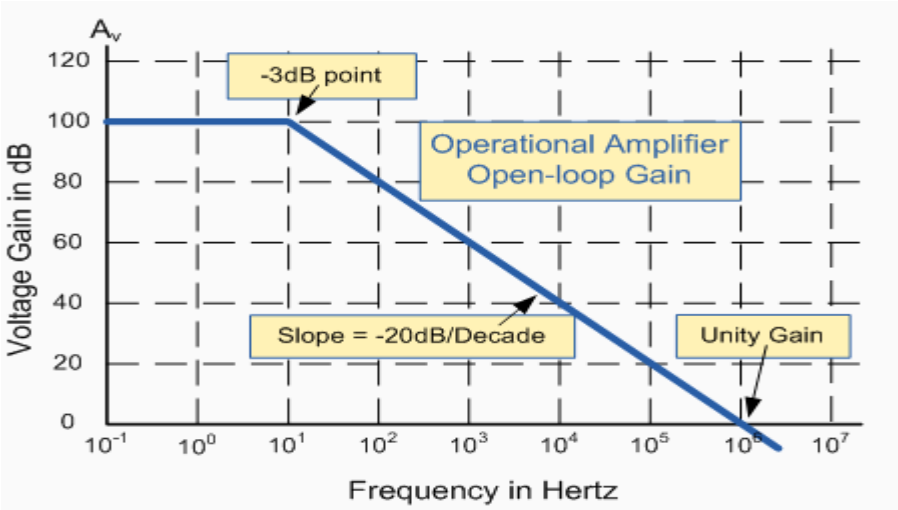

Figure 18: Open loop frequency curve

The product of gain against frequency for an op-amp is a constant at any point in the frequency response curve of the op-amp. The open loops frequency response curve shown above shows that. The unity gain frequency, i.e. the frequency at which the curve cuts the frequency axis (gain magnitude = 0 dB) also can be used to predict the amplifier gain at any point along the curve. This constant is referred to as the Gain Bandwidth Product or GBP.

The GBP of an op-amp is given by, GBP = Gain of Amplifier x Bandwidth or A x BW.

For example, from the above graph the amplifier gain at 100 KHz = 20dB or 10, then the GBP or Unity gain bandwidth = 100 kHz x 10 = 1MHz.

Similarly, a gain at 1 KHz = 60dB or 1000, therefore the GBP = 1,000 x 1,000 = 1,000,000.

We can use this same formula to obtain the Voltage Gain (A) of the amplifier:

Voltage Gain (A) = $\frac{V_{out}}{V_{in}}$ and in **Decibels** or (dB) is given as 20 log (A) or 20 log ($\frac{V_{out}}{V_{in}}$) in dB.

5.6 AN OPERATIONAL AMPLIFIER BANDWIDTH

The bandwidth of an operational amplifiers is defined as the frequency range over which the amplifier voltage gain is greater than 70.7% or -3dB (where we consider the maximum gain to be the reference or 0dB) of the maximum output value attained by the gain of the amplifier. Suppose if the maximum gain of an amplifier is 50dB for example then 47dB is given as the -3dB or 70.7% of V_{max} down point from the frequency response curve.

5.7 CHARACTERISTICS OF IDEAL AND THE REAL OP-AMPS

The main differences between the characteristics of ideal op-amp and the real op-amp are:-

1. Finite Gain: operational amplifiers are mainly used to amplify the input signal and the higher its open loop gain the better as in many applications they are used with a feedback loop, so ideal op-amps are characterized by a gain of infinity. For practical op-amps, the voltage gain is finite. Typical values for low frequencies and small signals are A = 102 – 105, corresponding to 40-100 dB gain.
2. Input impedance, (Z_{in}): The Input impedance of an op-amp for an ideal device has to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry.
3. Bandwidth, (BW): An ideal operational amplifier has an infinite Frequency Response and can thus be used to amplify signals of any frequency. However as evident from the frequency response curve below the gain of the amplifier is not contant irrespective of frequency and after the first pole it begins to drop with a slope of 20dB/decade thus the higher the frequency of the first pole the higher the range of freq over which it operates desirably.

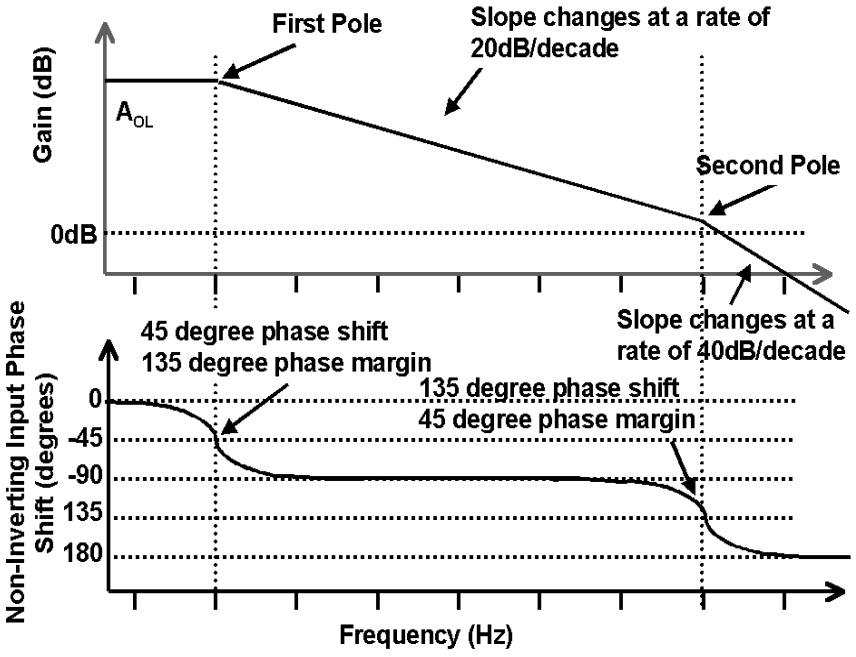

Figure 19: Op-Amp bandwidth sample graph

4. Finite Linear Range: The linear relation $V_0 = A (V_a - V_b)$ between the input and output voltages are valid only for a limited range of v0. Normally the maximum value of v0 for

linear operation is somewhat smaller than the positive dc supply voltage, the minimum value of v0 is somewhat positive with respect to the negative voltage.

5. Offset Voltage: The amplifiers output is supposed to be completely independent of common potentials applied to both inputs and is supposed to be zero when the voltage difference between the inverting and non-inverting inputs is zero. For an ideal op-amp, if $V_a = V_b$ (which is easily obtained by short circuiting the input terminals) then v0 = 0. In real devices, this is not exactly true, and a voltage $V_{0,off} \neq 0$ will occur at the output for shorted inputs. Since v0,off is usually directly proportional to the gain, the effect can be more conveniently described in terms of the input offset voltage $V_{in,off}$, defined as the differential input voltage needed to restore v0=0 in the real devices. For MOS op-amps $V_{in,off}$ is about 5-
   15mV.
6. Common Mode Rejection Ratio (CMRR): The common-mode input voltage is defined by $V_{in,c} = (V_a + V_b)/2$ as contrasted with the differential-mode input voltage $V_{in,d} = V_a - V_b$. The differential gain A_D and also the common-mode gain AC which can be measured as shown in figure, where $A_c = V_0 / V_{in,c}$.
   The CMRR is now defined as A_D/A_c or in logarithmic value CMRR = 20 log10(A_D / A_c) in dB. Typical CMRR values for MOS amplifiers are in the 60-80 dB range. The CMRR measures how much the op-amp can suppress common-mode signals at its inputs. These normally represent undesirable noise, and hence a large CMRR is an important requirement.
7. Frequency Response: Because of stray capacitances, finite carrier mobilities and so-on, the gain A decreases at high frequencies. It is usual to describe this effect in terms of the unity gain bandwidth, that is the frequency f_0 at which $|A(f_0)| = 1$. For MOS op-amps, f0 is usually in the range of 1-10 MHz. It can be measured with the op-amp connected in a voltage-follower configuration.
8. Slew Rate: For a large input step voltage, some transistors in the op-amp may be driven out of their saturation regions or completely cut-off. As a result the output will follow the input at a slower finite rate. The maximum rate of change dV_0/dt is called slew rate. It is not directly related to the frequency response. For typical MOS op-amps slew-rates of 1~20 V/μs can be obtained.

9. Nonzero Output Resistance: For a real MOS op-amp, the open loop output impedance is nonzero. It is usually resistive, and is of the order of 0.1-5KΩ for op-amps with an output buffer, it can be much higher (~1MΩ) for op-amps with un-buffered output. This affects the speed with which the op-amp can charge a capacitor connected to its output and hence the highest signal frequency.
10. Noise: The MOS transistor generates noise, which can be described in terms of an equivalent current source in parallel with the channel of the device. The noisy transistors in an op-amp give rise to a noise voltage von at the output of the op-amp, this can be again modeled by an equivalent voltage source $V_n = V_{on}/A$ at the op-amp input. Unfortunately, the magnitude of this noise is relatively high, especially in the low frequency band where the flicker noise of the input devices is high; it is about 10 times the noise occurring in an op-amp fabricated in bipolar technology. In a wideband (say in the 10Hz to 1MHz range), the equivalent input noise source is usually of the order of 10~50µV RMS, in contrast to the 3~5µv achievable for low-noise bipolar op-amps.

5.8 PRACTICAL STRUCTURE OF OP-AMP

The practical structure of op-amp consists of 3 main blocks.

(a) The first block is input differential amplifier, which is designed so that it provides very high input impedance, a large CMRR and PSRR, a low offset voltage, low noise and high gain. Its output should preferably be single ended, so that the rest of the op-amp need not contain symmetrical differential stages. Since the transistors in the input stage operate in their saturation regions there is an appreciable dc voltage difference between input and output signals of the input stage.

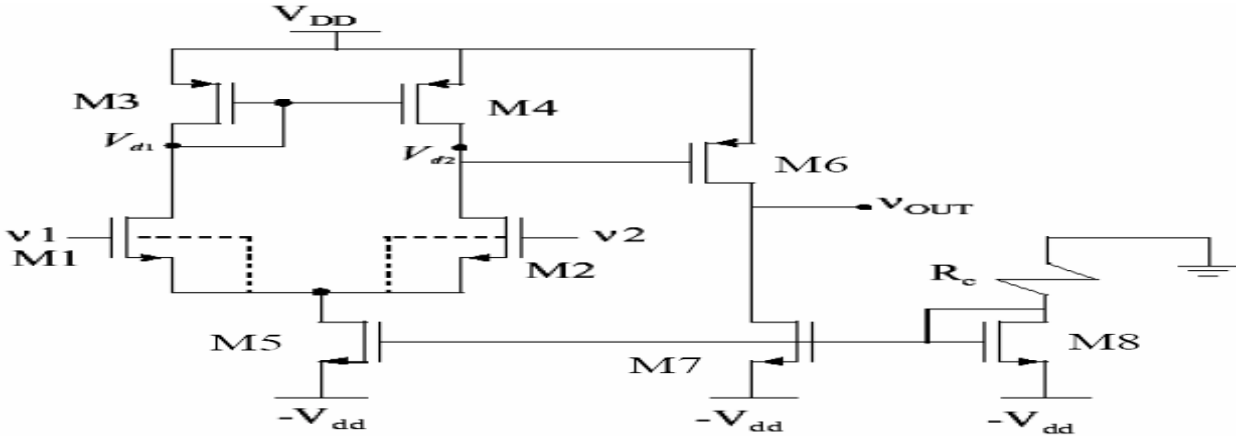

Figure 20: Block Diagram for a Practical Op-Amp

(b) The second stage performs one or more of the following functions:

Level shifting: This is needed to compensate for the dc voltage change occurring in the input stage, and thus to assure the appropriate dc bias for the following stages.

Added Gain: The gain provided by the input stage is not sufficient and additional amplification is required.

Differential to single ended conversion: In some circuits, the input stage has a differential output, and the conversion to single ended signals is performed in a subsequent stage.

(c) The third block is the output buffer. It provides the low output impedance and larger output current needed to drive the load of the op-amp. It normally does not contribute to the voltage gain. If the op-amp is an internal component of a switched-capacitor filter, then the output load is a capacitor, and the buffer need not provide very large current or very low output impedance. However if the op-amp is at the filter output, then it may have to drive a large capacitor and/or resistive load. This requires large current drive capability and very low output impedance which can only be attained by using large output devices with appreciable dc bias currents.

Finally the full op-amp schematic designed using the previous designed current mirror and differential amplifiers and the common source amplifiercircuit is as shown in figure 21 below:-

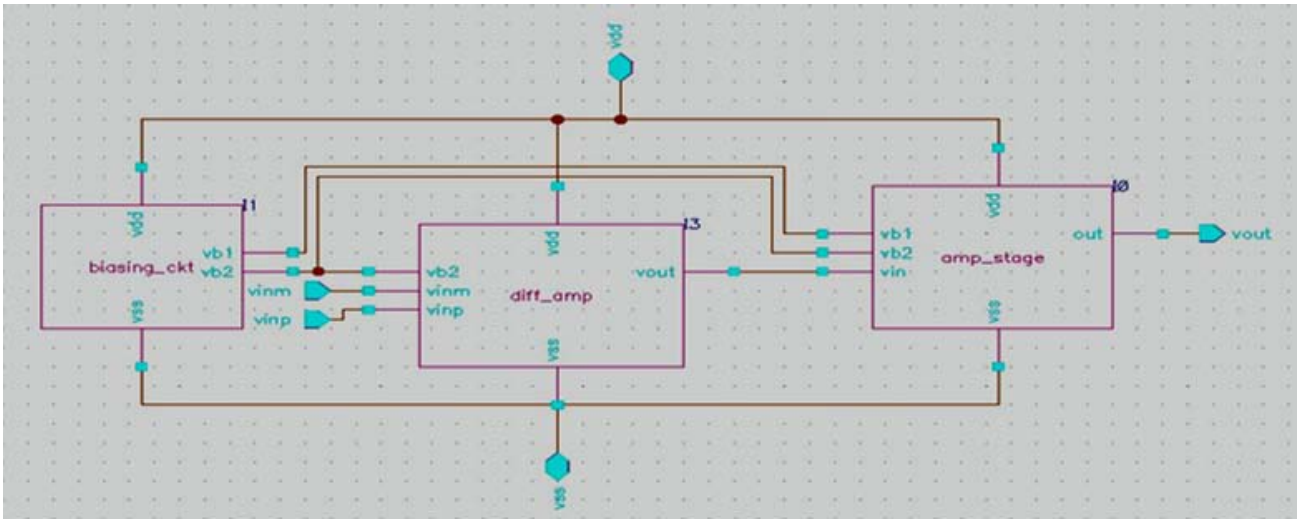

Figure 21: Block Diagram for the Proposed Op-Amp

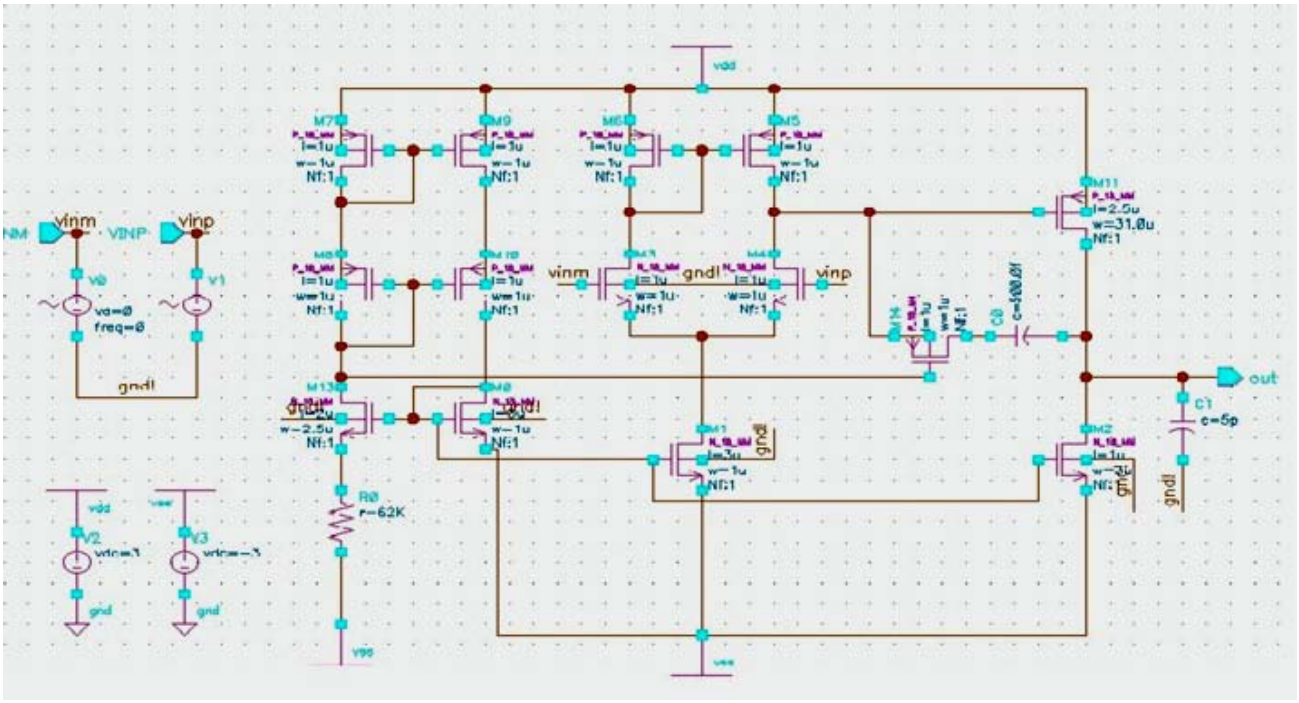

Figure 22: Op-Amp full schematic

Chapter 6

RESULTS AND DISCUSSION

6.1 INTRODUCTION

The designed op-amp was simulated to find the different characteristics of the designed op-amp. Further the layout of the designed op-amp was created and the parasitic capacitance and resistance was extracted. The extracted designs were then simulated with the parasitic values and compared with the schematic. Later in the chapter we also compare the obtained parameters of the device through simulation to the specifications for the device and with the post layout simulation results. The different results are presented here.

6.1.1 OFFSET VOLTAGE

It is the voltage obtained at the output terminals, when the input terminals are connected to ground terminal, i.e., 0 volts. Here the offset voltage calculated for the op-amp is -603mv.

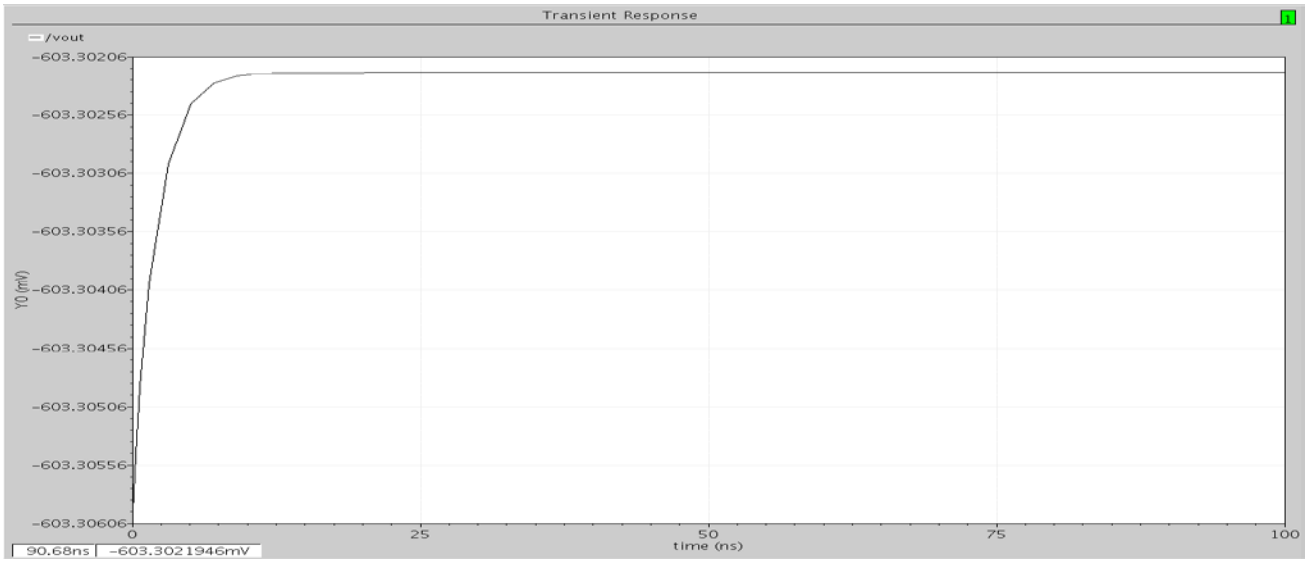

Figure 23: Op-Amp offset voltage

6.2.2 SLEW RATE

It is the maximum rate of change of output voltage. Here the slope of the curve calculated as 12.5 v/µs.

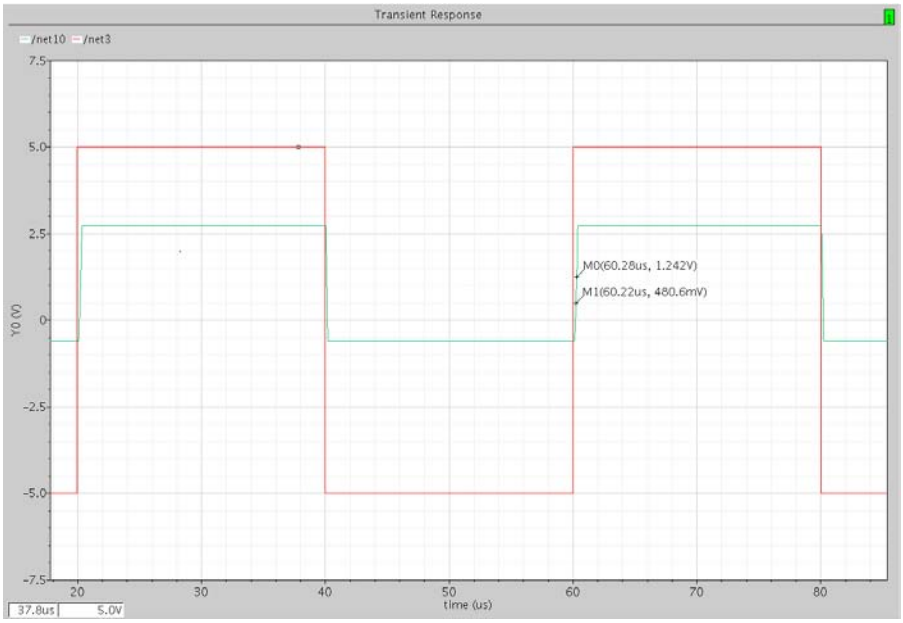

Figure 24: Op-amp slew rate

6.2.3 GAIN

It is defined as the ratio of the output to the input. Here the input voltage given as 1 volts sine wave. Hence the gain is calculated as 10.4v/v.

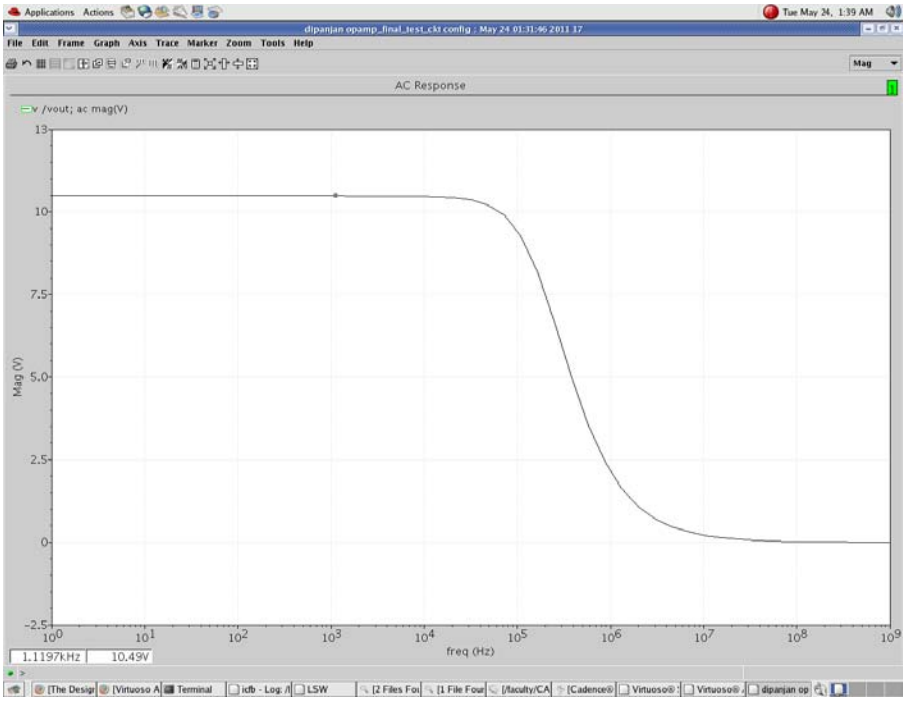

Figure 25: Op-Amp Gain

6.2.4 BANDWIDTH

It is the maximum allowable range of the frequencies. Here the bandwidth of this op-amp calculated as 2.16 MHz for unity gain and 202kHz at -3dB.

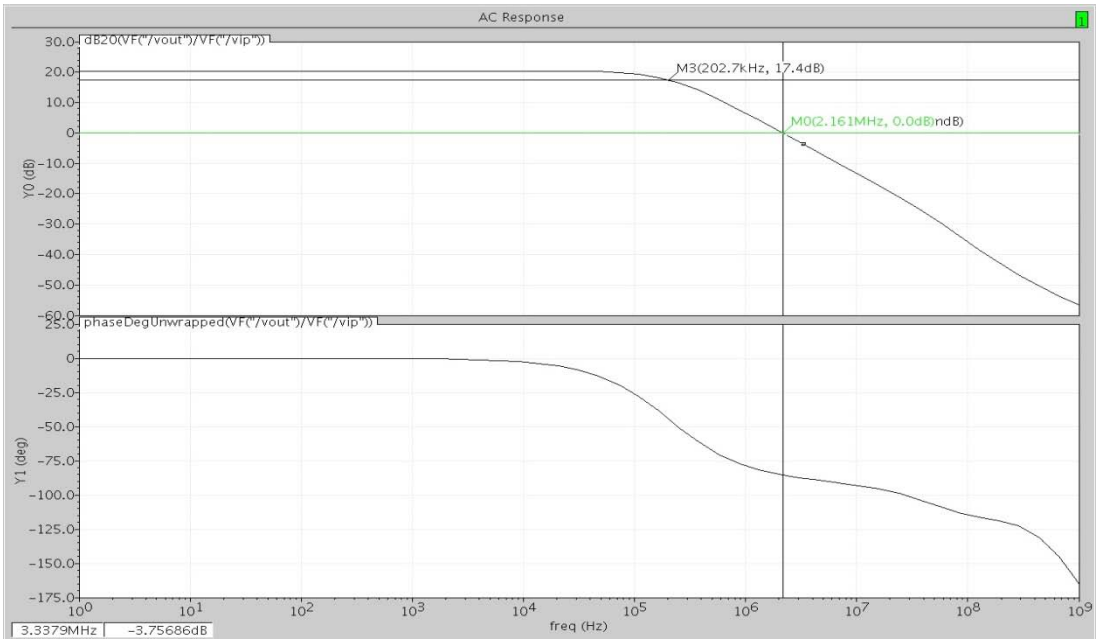

Figure 26: Op-Amp bandwidth

6.2.5 POWER DISSIPATION

The power dissipation of this op-amp is calculated as 0.9mW. The power is calculated as the power dissipated by the VDD source. To calculate the power in cadence we simulated the circuit and saved the DC operating points and calculated the power as the product of the total current drawn from the V_{DD} DC voltage source and the total DC potential across the circuit.(V_{DD} + |V_{SS}|)

Table 1: Observations for low power op-amp with supply 1.8v

Parameters	Specification	Simulation Results before layout	Simulation Results after layout
Gain	10 V/V || 20 dB	12 V/V || 22 dB	10.2 V/V || 20.14 dB
3-dB Bandwidth	20 kHz.	397 kHz.	200 kHz
UGB	N/A	4.6MHz	2.165 MHz
CMRR	>50 dB	80dB	64dB
PSRR	N/A	84dB|59dB	87dB|60dB
SLEW RATE	10 v/µs	25 v/µs	12.47v/µs
POWER DISSIPATION	1 mW.	0.9 mW	0.6 mW
ICMR	1.2V←→ 2.4V	-1V ←→ 2.4V	-1V ←→ 2.4V
Output Offset Voltage	N/A	-600 mV	-600 mV

6.4 CONCLUSION

The proposed design has been able to satisfy most of the specifications provided for the op-amp. The proposed op-amp is a two stage single output op-amp. The input stage is a differential amplifier and a common source stage forms the second stage of the op-amp. The layout of the design has been made and simulated. The post layout simulations abide by the given specification. The entire design has been done in UMC 180 nm technology.

The gain of the op-amp can be increased further by the use of cascade device in the input stage

The voltage swing may be increased by using a double ended output.

The gain and phase plot of the op-amp has been plotted during post layout simulations and we obtain a phase margin of about 95 degrees. So we can conclude that the op-amp is stable

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APPENDIX A:

LAYOUTS AND RC -EXTRACTED VIEWS

Bias circuit for amplifier current sinks :

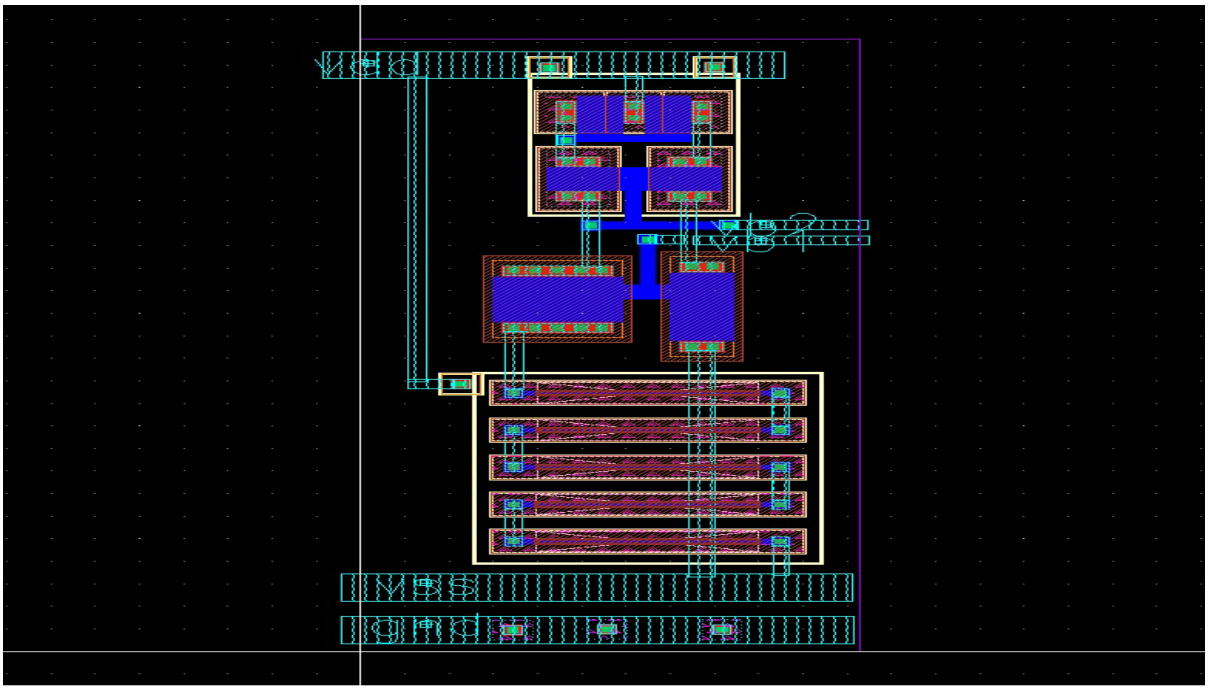

Figure 27: Layout view of Bias Circuit

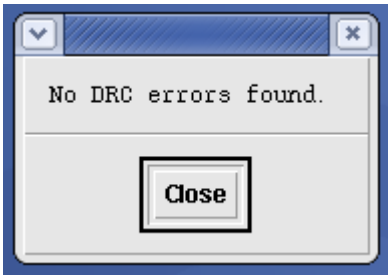

Figure 28: DRC Results for bias circuit

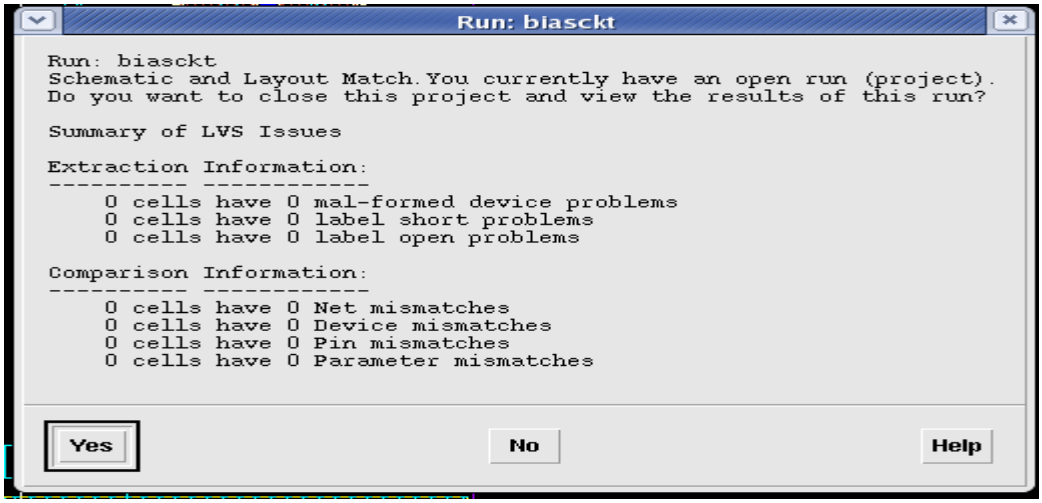

Figure 29: LVS Result

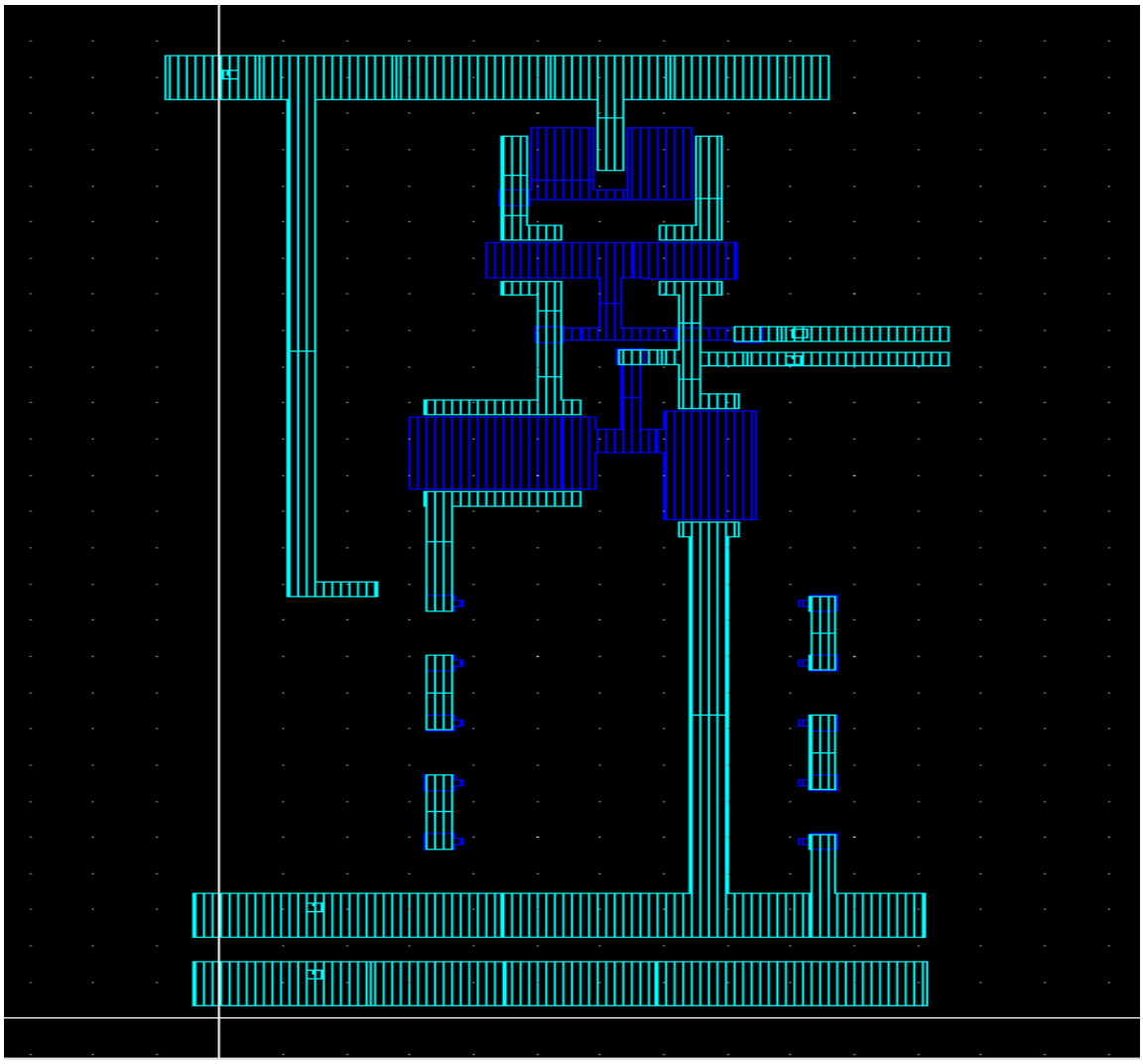

Figure 30: Bias Circuit RC extracted View

Differential amplifier:

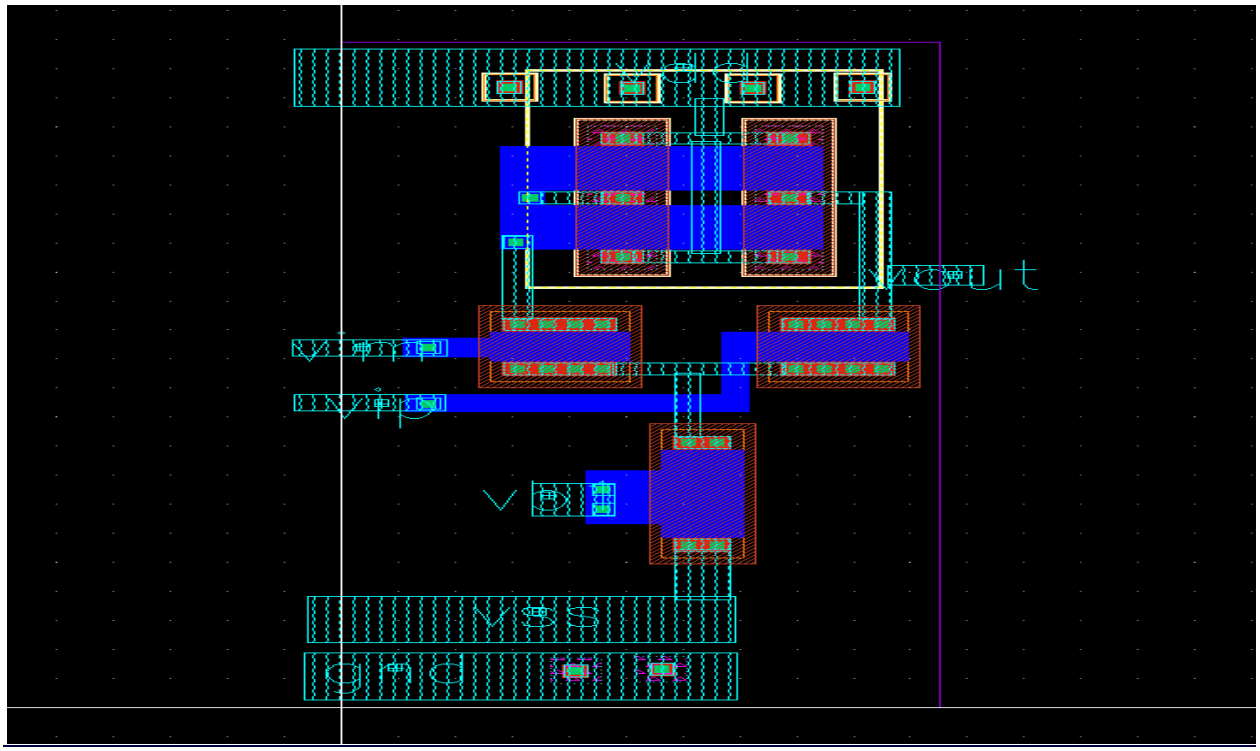

Figure 31: Diff amp layout view

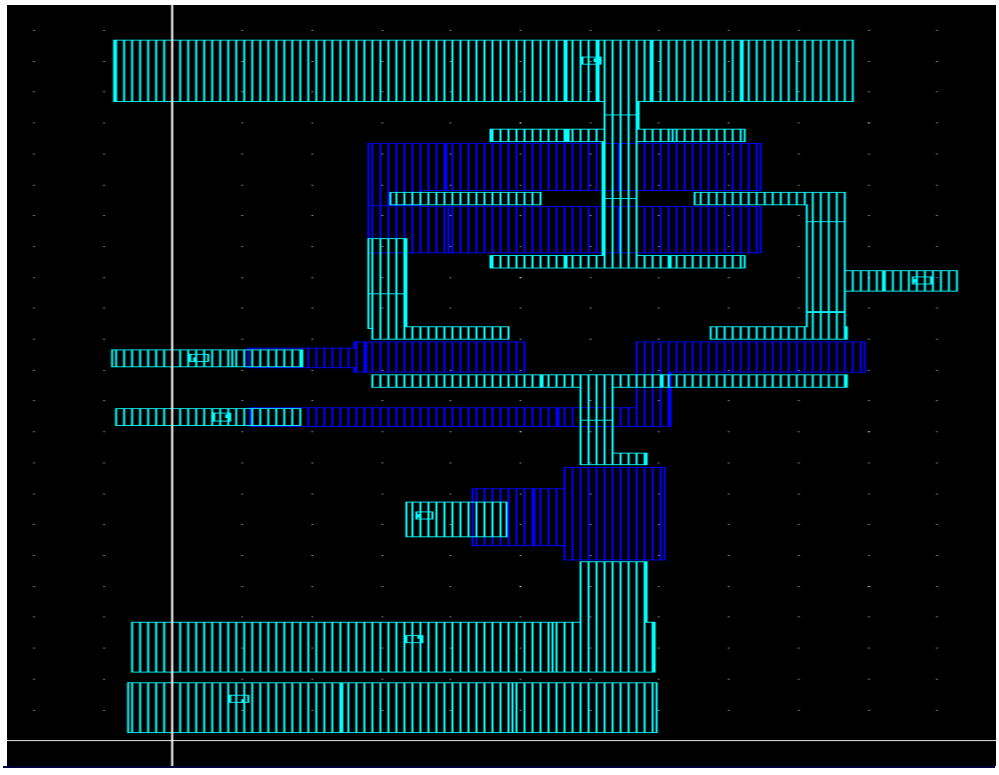

Figure 32:RC extracted view of differential amplifier

Common source amplifier stage:

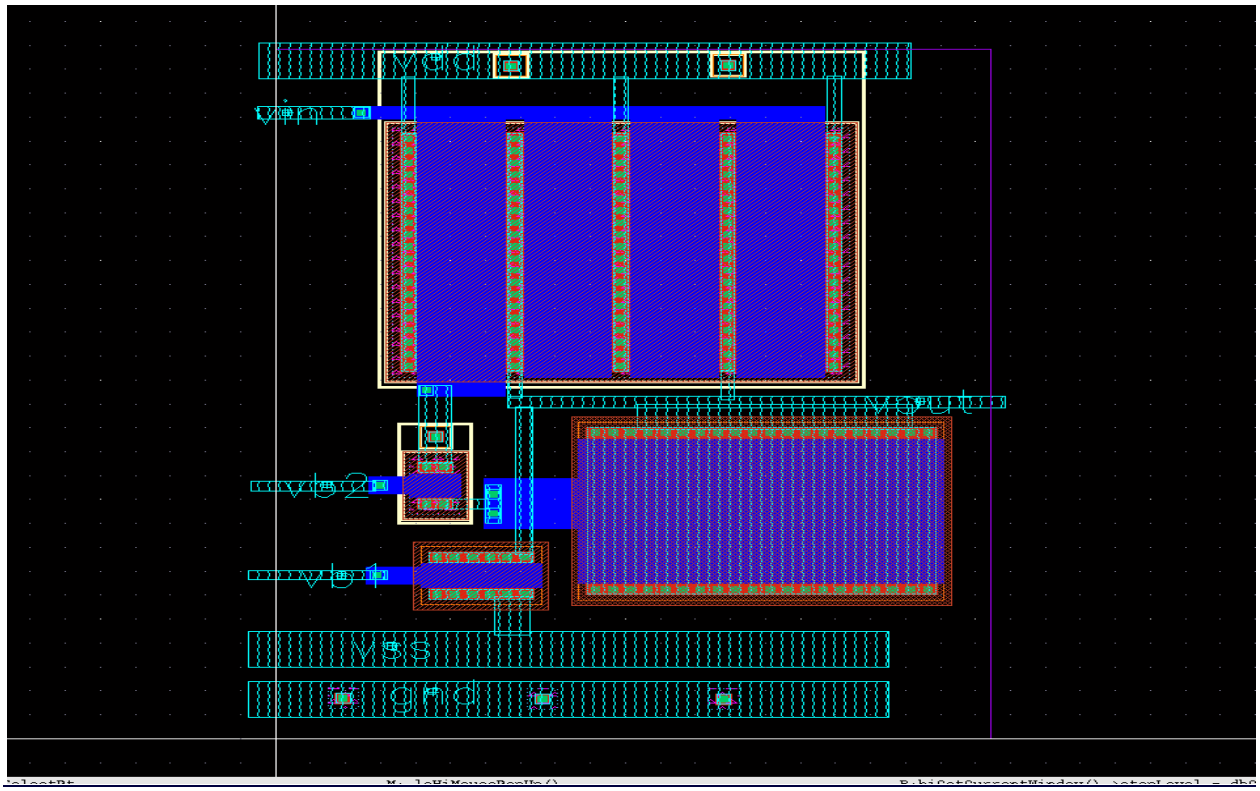

Figure 33: Common Source Amplifier layout view

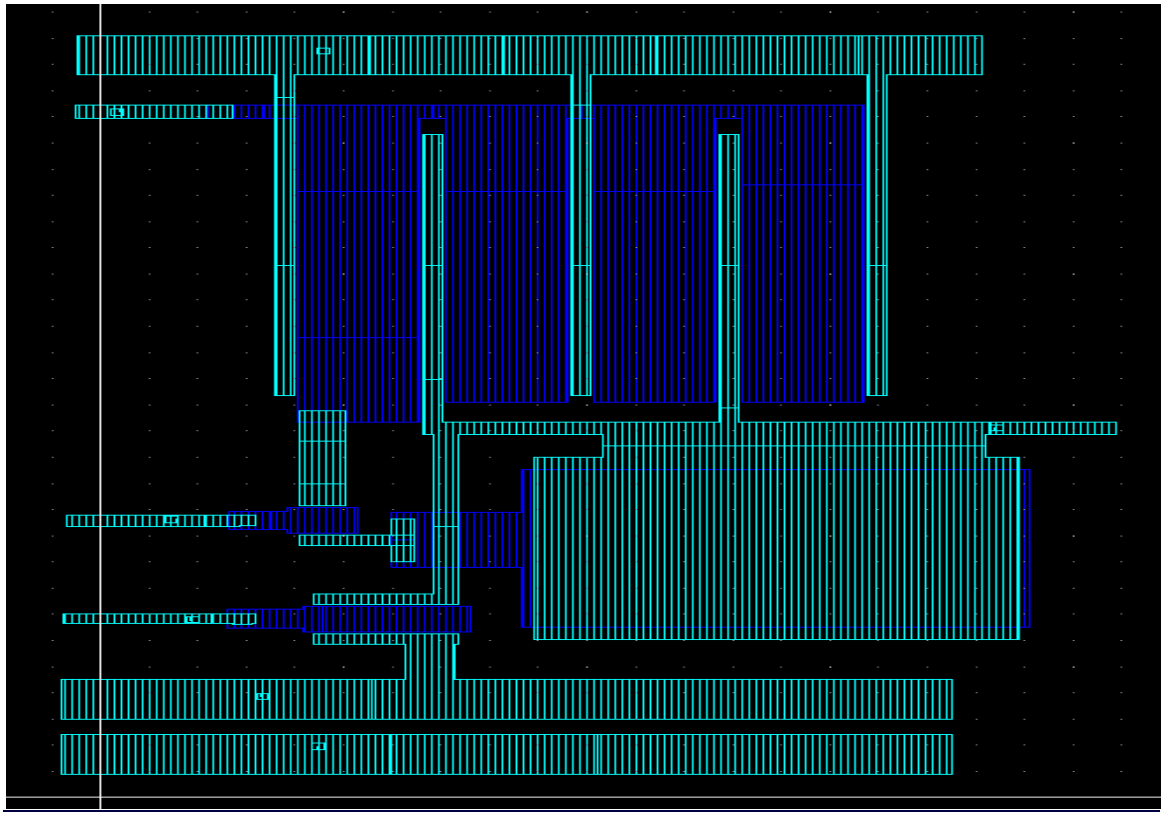

Figure 34: Common Source Amplifier RC extracted view

Opamp:

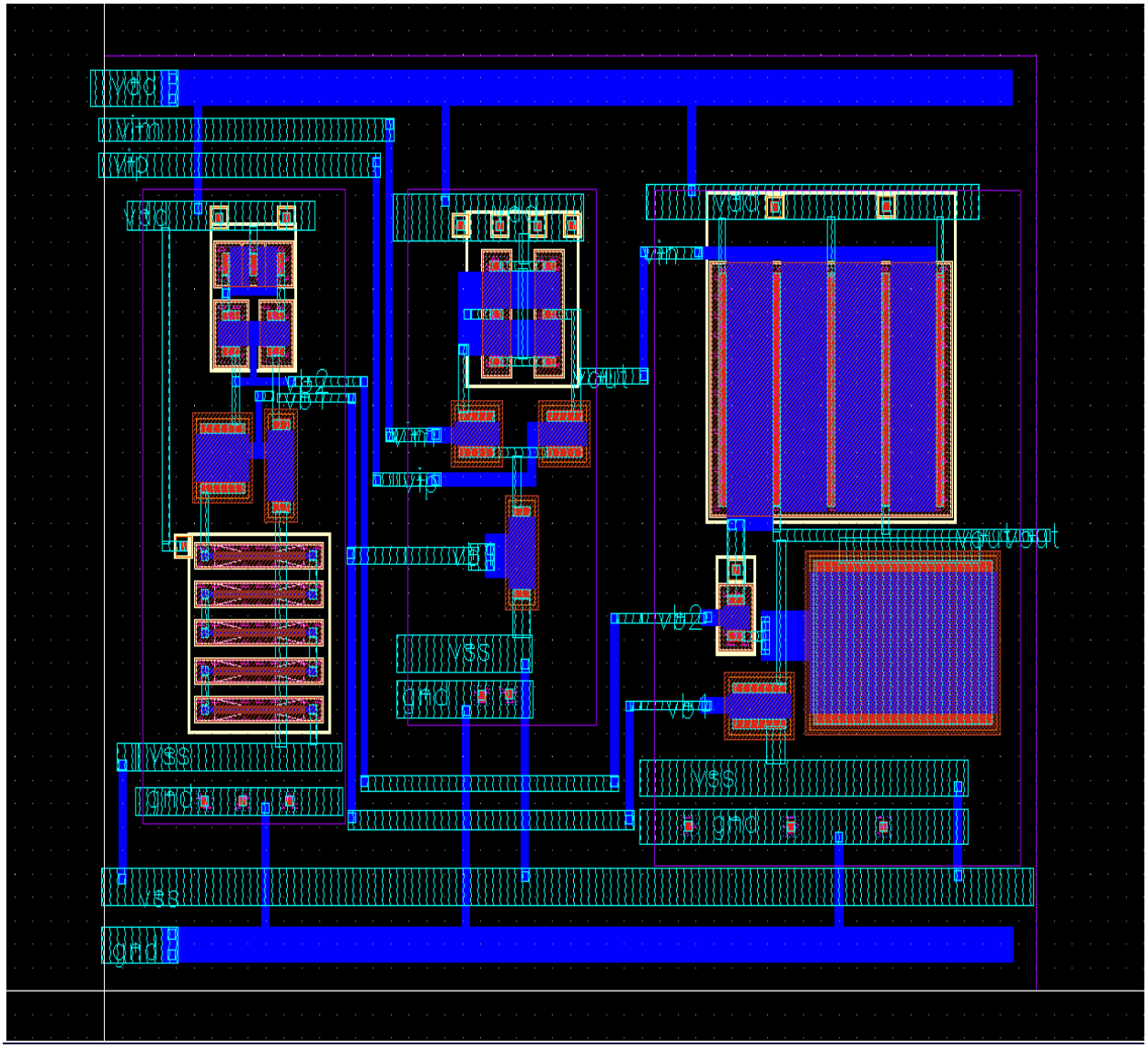

Figure 35: Op-amp layout view

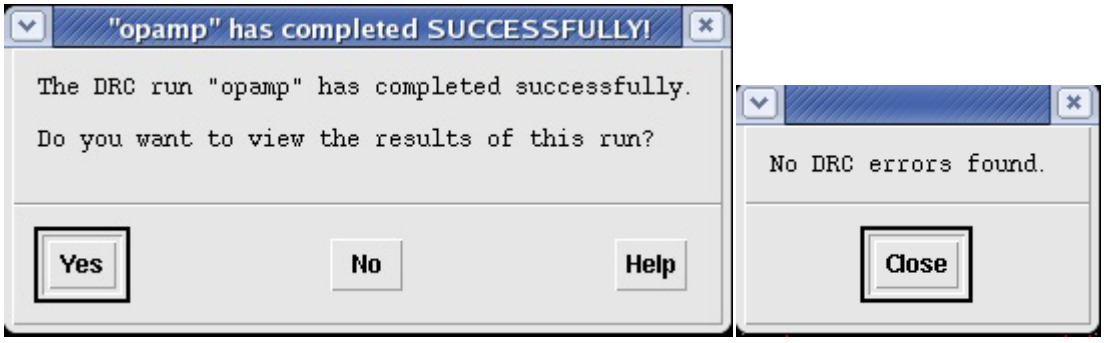

Figure 36: Op-amp DRC Results

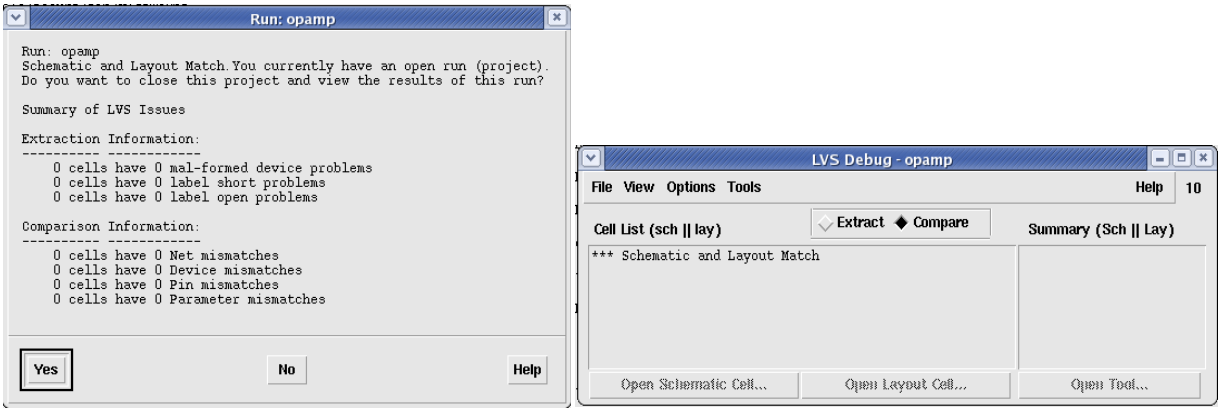

Figure 37: Op-Amp LVS Results

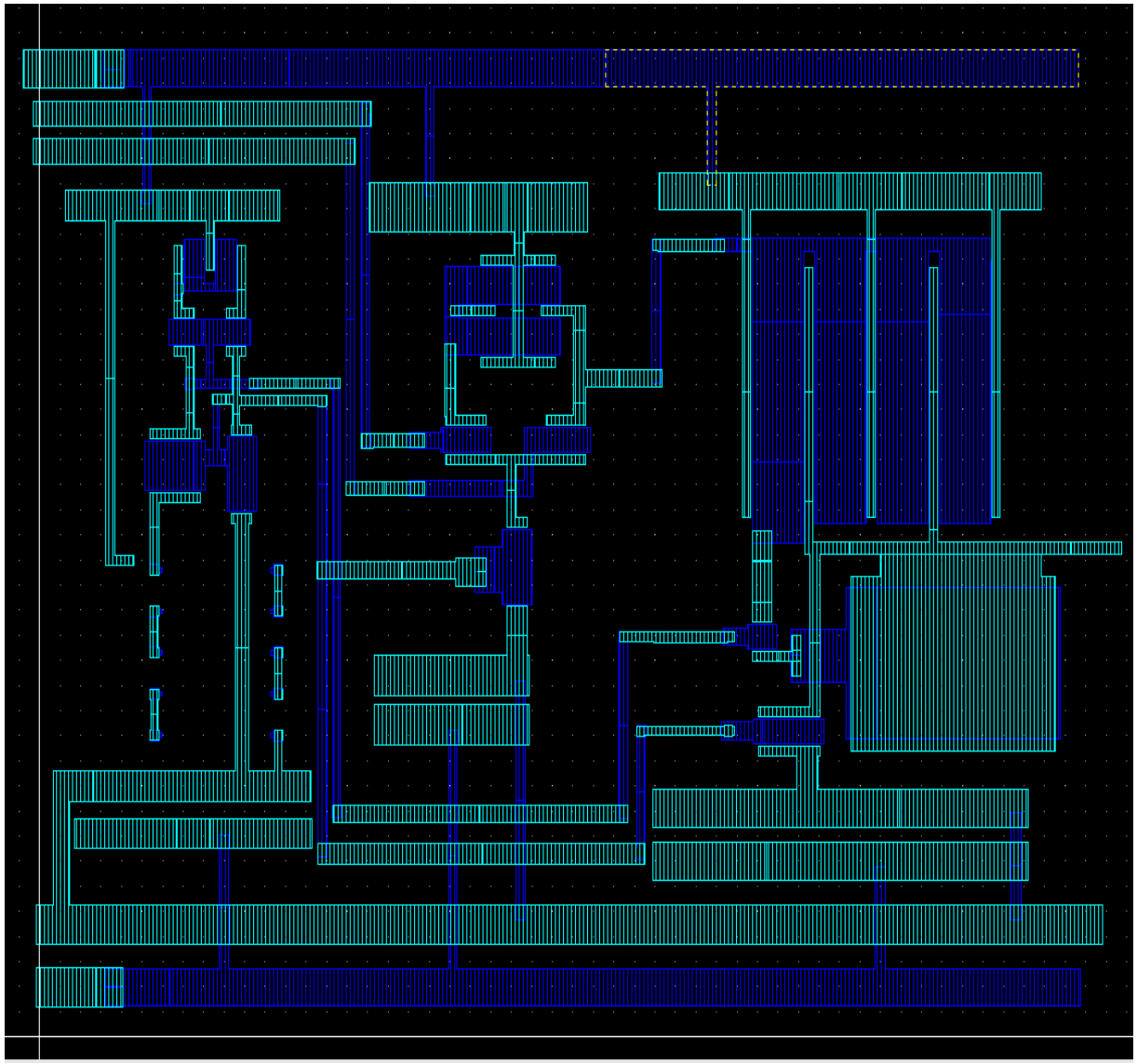

Figure 38: Op-Amp RC extracted view