VLSI Implementation of a Demand mode Dual Chamber Rate Responsive Cardiac Pacemaker

A Thesis submitted in partial fulfilment of the requirements for the degree of

Bachelor of Technology
in
Electronics and Instrumentation Engineering

Submitted by:

Abhipsa Panda
108EI007

Under the supervision of
Prof. Kamalakanta Mahapatra

Department of Electronics and Communication Engineering,

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C E R T I F I C A T E

This is to certify that the Thesis entitled, '**VLSI Implementation of a Demand mode Dual Chamber Rate Responsive Cardiac Pacemaker**' submitted by **Abhipsa Panda** in partial fulfilment of the requirements for the award of **Bachelor of Technology Degree** in **Electronics and Instrumentation Engineering** at the **National Institute of Technology Rourkela** is an authentic work carried out by her under my supervision. To the best of my knowledge and belief the matter embodied in the Thesis has not been submitted by her to any other University/Institute for the award of any Degree/Diploma.

Prof. Kamalakanta Mahapatra
Department of Electronics and Communication Engineering,
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A C K N O W L E D G E M E N T

This is a Research Project and I would never have been able to complete it successfully without some people. I would always be grateful to the following for their help and guidance throughout the project.

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Finally, a word of thanks to God, all my friends, everyone associated with this project directly or indirectly to make it a success.

Abhipsa Panda

A B S T R A C T

This project is aimed to design a dual chamber rate responsive cardiac pacemaker, implement it in VLSI and improvise on it for real time safety critical environments.

A state machine approach has been followed to achieve the desired purpose. The heart of the pacemaker system rests in the pulse generator which forms the major portion of the project. It has been developed using VHDL and implemented in hardware using FPGA. In the FSM, first an input event is detected. Once this input is detected a timer is set for approximately 0.8 sec, which will be the time between heartbeats, thus giving us 72 heartbeats per minute. Once the timer expires we check to see if a new event is detected. If one is detected we repeat the process of detection and waiting. If one has not been received we need to stimulate the heart and then repeat the process of detection and waiting.

The code has been optimized and modified for different pacemaker modes. Adequate effort has been put in for designing a sensing circuit and other peripherals like memory, data compression techniques and remote monitoring equipment, culminating in suggestions for improvement in respective areas. It closes with pacemaker testing for real life applications and scope for further work in the field.

C O N T E N T S

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