

Design of Digital FIR Filter using SPST based Multipliers

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

VLSI DESIGN and EMBEDDED SYSTEM

By

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Roll No : 20607010



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Under the Guidance of

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ABSTRACT

Multiplication and addition are the most basic operations in all DSP applications. We are going for a low power implementation of these basic operations, as the power has a huge impact on the life of battery, as well as on the system life time. This paper provides the experience of applying an advanced version of former spurious power suppression technique(SPST) on multipliers for high speed and low power purposes. For this first we are applying this SPST technique on adder. Later we use SPST based adder on both modified booth decoder and the compression tree of multipliers to enlarge the power reduction. The simulation results show that the SPST implementation with AND gates own extremely high flexibility on adjusting the data asserting time which not only facilitates the robustness of SPST but also leads speed improvement as well as dissipating very lesser power by gaining 40% power reduction.

For the application point of view i have designed a 12-tap,16 bit signed digital FIR Filter in which i have used SPST based adder and multiplier components to decrease the power as well as to increase the speed.

Simulation results show that the FIR filter with SPST based multipliers is owning approximately 35% power reduction and 15% speed improvement compared to a FIR filter with tree multipliers.

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