Design of Digital FIR Filter using SPST based Multipliers

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

VLSI DESIGN and EMBEDDED SYSTEM

By

CHANDRASHEKAR.K
Roll No : 20607010

Department of Electronics & Communication Engineering
National Institute of Technology
Rourkela
2008

Design of Digital FIR Filter using SPST based Multipliers

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

VLSI DESIGN and EMBEDDED SYSTEM

By

CHANDRASHEKAR.K
Roll No : 20607010

Under the Guidance of

Prof.K.K.MAHAPATRA

Department of Electronics & Communication Engineering
National Institute of Technology
Rourkela
2008

CONTENTS

Acknowledgement

I would like to express my gratitude to my major **Prof. K. K. Mahapatra** for his guidance, advice and constant support throughout my thesis work. I would like to thank him for being my advisor here at National Institute of Technology (Deemed University).

Next, I want to express my respects to **Prof. G.S.Rath**, **Prof. G. Panda, Prof. S.K. Patra** and **Dr. S. Meher** for teaching me and also helping me how to learn. They have been great sources of inspiration to me and I thank them from the bottom of my heart.

I would like to thank all faculty members and staff of the Department of Electronics and Communication Engineering, N.I.T. Rourkela for their generous help in various ways for the completion of this thesis.

I would also like to mention the names of **Jithendra sir,sudheer,vijay, leslin,sonali and sakshi** for helping me a lot during the thesis period.

I would like to thank all my friends and especially my classmates for all the thoughtful and mind stimulating discussions we had, which prompted us to think beyond the obvious. I've enjoyed their companionship so much during my stay at NIT, Rourkela.

I am especially indebted to my parents for their love, sacrifice, and support. They are my first teachers after I came to this world and have set great examples for me about how to live, study, and work.

CHANDRASHEKAR.K
Roll No: 20607010
Dept of ECE, NIT, Rourkela

ABSTRACT

Multiplication and addition are the most basic operations in all DSP applications. We are going for a low power implementation of these basic operations, as the power has a huge impact on the life of battery, as well as on the system life time. This paper provides the experience of applying an advanced version of former spurious power suppression technique(SPST) on multipliers for high speed and low power purposes. For this first we are applying this SPST technique on adder. Later we use SPST based adder on both modified booth decoder and the compression tree of multipliers to enlarge the power reduction. The simulation results show that the SPST implementation with AND gates own extremely high flexibility on adjusting the data asserting time which not only facilitates the robustness of SPST but also leads speed improvement as well as dissipating very lesser power by gaining 40% power reduction.

For the application point of view i have designed a 12-tap,16 bit signed digital FIR Filter in which i have used SPST based adder and multiplier components to decrease the power as well as to increase the speed.

Simulation results show that the FIR filter with SPST based multipliers is owning approximately 35% power reduction and 15% speed improvement compared to a FIR filter with tree multipliers.

LIST OF FIGURES

LIST OF TABLES

LIST OF WINDOWS