DEVELOPMENT OF EFFICIENT POWER SUPPLY FOR MICROPROCESSORS USING ZERO VOLTAGE SWITCHING

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DEVELOPMENT OF EFFICIENT POWER SUPPLY FOR MICROPROCESSORS USING ZERO VOLTAGE SWITCHING

A Thesis submitted in partial fulfillment of the requirements for the degree of

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By

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CERTIFICATE

This is to certify that the thesis entitled "**Development of Efficient Power Supply for Microprocessors using Zero Voltage Switching**", submitted by **Suchi Sraba Pattanayak (Roll. No. 109EE0296)** in partial fulfilment of the requirements for the award of **Bachelor of Technology** in **Electrical Engineering** during session 2012-2013 at National Institute of Technology, Rourkela is a bonafide record of research work carried out by them under my supervision and guidance.

The candidate has fulfilled all the prescribed requirements.

The Thesis which is based on candidate's own work, has not been submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a bachelor of technology degree in Electrical Engineering.

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Head of the Department

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Suchi Sraba Pattanayak

ABSTRACT

In order to meet the market demand for faster personal computers and laptops, microprocessor manufacturers are increasing the clock frequency at which the processor operates. And since the technology used is CMOS (Complementary Metal Oxide Semiconductor), the power dissipation of the microprocessor increases linearly with clock frequency. For very powerful processors, conventional heat dissipation methods are insufficient. Normally, a combination of power supply voltage reduction and selective clock speed reduction is used to reduce power dissipation. Thus special power supplies are used that would supply low voltages and high currents to meet the increasing load demands handled by the microprocessor.

This work presents a reliable and efficient low voltage high current Voltage Regulator Module (VRM) for devices using microprocessors like desktop computers, laptops and tablets. The Switched Mode Power Supply (SMPS) generally used in computers essentially converts the input AC supply into ±12 V or ±5 V DC supply but to step this DC voltage down to further low voltages (1.2 V), synchronous converters are the obvious choices owing to their low conduction and switching losses. In this project the various losses occurring in the standard buck converter, synchronous buck converter and multiphase synchronous buck converter (MSBC) is analyzed. It is then found that the high side switching loss dominates the total loss. Also, ZVS (Zero Voltage Switching), the most efficient soft switching technique is employed along with a SBC to form an efficient power supply.

The suggested ZVS SBC is then simulated using PSIM for design values of 3.3 V, 12 A output and a 200 kHz switching frequency. It is seen that this converter provides an efficient output as compared to a conventional SBC. Moreover, the resonant circuit is devoid of the switching loss. With this satisfactory result, the increase in efficiency of SBC along with ZVS is realized in this dissertation.

CONTENTS

LIST OF FIGURES

CHAPTER 1

1. Introduction

1.1 Research Background

A power supply unit (PSU) for desktop computers or laptops essentially converts AC to low voltage regulated DC supply for the various parts of a computer. Several DC power supplies are required, which has to be regulated accurately for stable operation. First generation computers used a heavy step down transformer and a linear power supply. Modern computers use a SMPS (Switched Mode Power Supply) with a *ferrite-cored* high frequency transformer because it is much lighter, less costly and more efficient than the conventional linear power supply. Most recent power supplies have a standby voltage available, which means that even in powered down or "switch off" state, it can be started remotely via the keyboard, mouse, infrared remote etc.

The PSU of the first computer ever built supplied ±12 V, ±5 V and a total of 63.5 W power most of which on the 5 V rail [1]. During this period, microchips operated on 5 V. As microchips gradually evolved, they begin operating at even lower voltages 3.3 V. Then Intel developed a PSU that supplied 3.3 V, 5 V and 12 V [2]. Further due to advancement in technology, transistors grew smaller and smaller in size and it became preferable to operate them on lower supply voltages. In order to supply large amount of low-voltage power to the microprocessors, a voltage regulator module (VRM) began to be included on motherboards. Today's processors require up to 100 A at 2 V [3] or less, which was impractical to be delivered by conventional off-board power supplies.

1.2 Motivation

Advancement in technology is driving VLSI (Very Large Scale Integrated) circuits in the path of greater transistor integration and faster clock frequencies. This has imposed a challenge for delivering high current at low voltage and high switching frequencies to modern processors. Continuous turn on and turn off the switches at high switching frequency forms the basis of switching loss, which is directly proportional to switching frequency. Furthermore, according to Moore's Law, the number of transistors will go on increasing due to which eliminating the switching loss for an efficient power supply becomes the need of the hour.

A Test conducted in 2005 suggested that computer power supplies are generally 70 to 80% efficient. 80% efficiency means that the power supply will provide 80 W of DC power when fed with 100 W of AC power, and the remaining 20 W is dissipated in terms of heat [4]. Efficient power supplies have the following advantages:

a) They save money by wasting less power.
b) They use less electricity to power the same computer.
c) They emit less waste heat, which results in significant energy savings on central air conditioning in the summer.

Therefore, various initiatives are underway to improve the efficiency of computer power supplies to as high as 95%.

Voltage Regulator Modules are the power suppliers to the microprocessor or the Central Processing Unit (CPU). These are essentially buck converters that convert the SMPS output voltage to much lower voltage as required by the CPU. Recent processors require voltages as low as 1 V [3].

This work presents a solution to design an efficient power supply for the computer microprocessors. This design is also applicable for portable products like laptops, tablets and kiosks.

1.3 Chopper Topology

As previously discussed, the VRM steps down the input voltage into standard 12 V/5 V which is again stepped down to the required low voltage. In order to do that, DC-DC choppers are used. The simplest known chopper is a buck converter.

1.3.1 Buck Converter

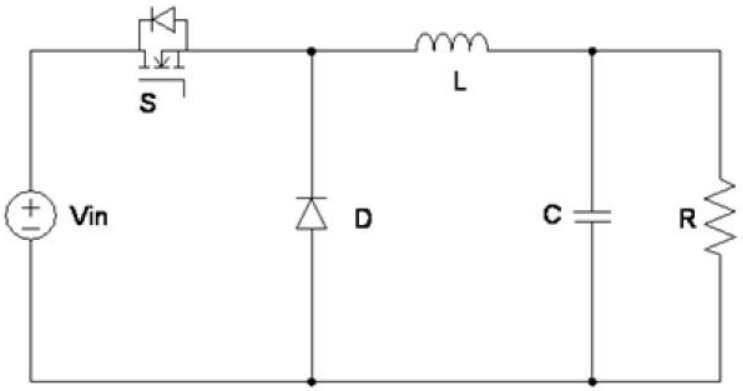

Figure 1: Buck Converter

In a buck converter, the average output voltage V_0, is less than the input voltage V_{in}. This acts like a step down converter.

The operation of the above circuit can be divided into two modes. Mode 1 begins when the MOSFET is switched ON at t=0. The input current, which rises, flows through filter inductor L, filter capacitor C, and the load resistor R. Mode 2 begins when the MOSFET is switched OFF at $t=t_1$. The freewheeling diode D_m conducts due to the energy stored by the inductor; and the inductor current continues to flow through L, C, load and diode D_m. The inductor current falls until the MOSFET is switched ON again in the next cycle. The waveforms for the voltage and currents are shown below for a continuous current flow in the inductor L.

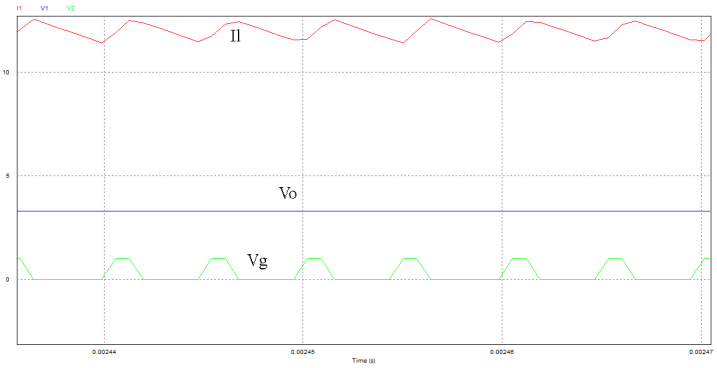

Figure 2: Waveforms of V0 and IL

During Mode 1:

$V_L = V_{in} - V_0$ (1)

$V_L = L\frac{di}{dt} \Rightarrow \Delta I_L = \int_0^{t_{on}} \frac{V_L}{L} dt = \frac{V_i - V_0}{L} t_{on}$, (2)

$t_{on} = kT$, where k is the duty cycle of switching.

During Mode 2:

$V_L = -V_0 \Rightarrow L\frac{di}{dt} = -V_0 \Rightarrow \Delta I_L = \oint_{t_{on}}^{T} -\frac{V_0}{L} dt = -\frac{V_0}{L}(T-kT) = -\frac{V_0}{L}T(1-k)$ (3)

Assuming steady state operation of converter, energy stored in each component at the end of commutation cycle is equal to that at the beginning of next cycle.

$\frac{V_{in}-V_0}{L}kT - \frac{V_0}{L}T(1-k) = 0 \Rightarrow V_0 = kV_{in}$ (4)

Since $k<1$, $V_0 < V_{in}$

But in practical cases, the switch has a finite nonlinear resistance. Its effect can gradually be negligible in most cases. But depending on the switching frequency, L and C, inductor current can be discontinuous.

Power loss in the diode $D_m = V_D I_0(1-k)$ [5],

where $V_D \rightarrow$ voltage drop across D_m

$I_0 \rightarrow$ load current

Basically, this diode D_m can be replaced by another device to reduce the power loss appearing across it.

1.3.2 Synchronous Buck Converter (SBC)

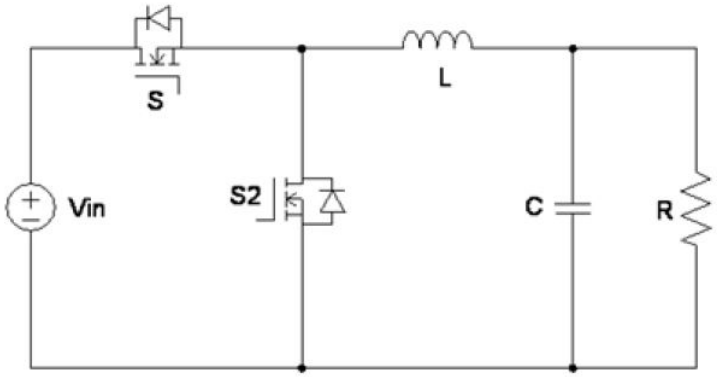

Figure 3: Synchronous Buck Converter

If the diode in a standard buck converter is replaced by another switch S_2 (basically a MOSFET) with very low R_{DSON}, the power loss will be

$$P_{loss} = I_0^2 R_{DSON}(1-k) \quad (5)$$

Comparing the power loss equations of diode with that of MOSFET, it is noted that systems designed for low duty cycle operation suffer from higher losses in the freewheeling diode and for such systems, it is advantageous to consider a synchronous buck converter design, which is nothing but the diode replaced by a switch.

Advantages of SBC over standard Buck Converter:

- Increased efficiency and reduced heat loss.
- Bi-Directionality, which lends itself to applications requiring regenerative braking.

Disadvantages:

- Higher cost of switch as compared to a diode.

- Complexity of circuit due to complementary gate signal required for S_2
- $C\frac{dV}{dt}$ induced Power Loss [6]

This system has to be completely synchronous. In the conventional buck converter, the freewheeling diode turned ON, on its own, shortly after switch turned OFF, as a result of the rising voltage across the diode. But in SBC, a gate signal has to be provided to the replacement switch S_2 when S_1 turns OFF to maintain continuity of current. There should be proper synchronism between gate signals of S_1 and S_2 i.e. both the switches should not turn ON at the same time. This is done in order to prevent *shoot-through* [7][8]. The simplest technique to avoid this is to provide a time delay between the turn off of S_1 and turn on of S_2 and vice versa. During this time delay, also known as dead time, the inductor current continues to flow through the internal body diode of S_2. When gate signal of S_2 is high, the inductor current flows through S_2. This topology provides better efficiency than the standard buck converter topology.

The SBC, which is in widespread use to provide low voltage high current power, converts 12 V or 5 V supply to voltages as low as 1.2 V for CPUs.

1.3.3 Multiphase Synchronous Buck Converter (MSBC)

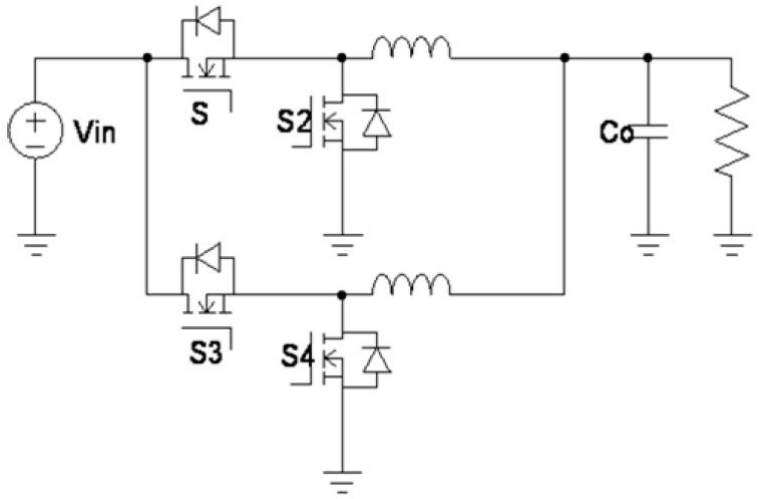

Figure 4: Multiphase Synchronous Buck Converter

The increased power consumption of microprocessors has rendered a single phase SBC insufficient to deliver the required current. If a SBC handles current more than its rated value, high thermal demands occur in the system components like inductors and MOSFETs. In order to meet the increasing current demand, VRMs use Multiphase Synchronous Buck Converters.

In a MSBC circuit topology, several basic SBC circuits are placed in between input and load. All the phases are turned ON at equally spaced intervals over the switching period.

Advantages:

- It can respond to load changes as quickly as if it switched at n times as fast, without increasing the switching losses. Therefore, it can respond to rapidly changing load of which microprocessor is a very good example.
- There is a significant decrease in switching ripple because of the effective increase in frequency.
- The load current divides in the multiple phases as a result of which heat losses on each of the switches are spread across a larger area.

PSUs convert the 12 V DC Supply to a lower voltage (around 1 V), suitable for the microprocessor. Modern CPU power requirements can exceed even 200 W, can change rapidly and have strict ripple free requirements (10 mV). In general, modern computers generally use 3 or 4 phase SBC [9].

1.4 Efficiency Issues

Factors on which efficiency depends:

- Conduction losses – Depend on Load
    - Resistance when MOSFET is conducting (R_{DSON})
    - Diode forward voltage drop (0.7V/0.4V)
    - Inductor Winding Resistance
    - Capacitor equivalent series resistance
- Switching losses:
    - Voltage Ampere Overlap loss
    - Frequency Switch loss
    - Reverse latence loss
    - Losses due to driving MOSFET gate and controller
    - Leakage current losses, and controller stand by consumption

In SBCs, semiconductor power electronics devices switch at very high current levels due to which these are associated with high power dissipation. Since the output voltage is generally a lot lower than the input voltages, it requires low duty cycle operation of the switch that causes

the MOSFET to turn ON and OFF in a very short period of time, thereby bring switching losses into picture [10][11]. These switching losses produce the following effects on the converters:

1. Limits the sampling frequency and efficiency
2. Induces noise due to high rate of change of current and voltage
3. Switching locus may exceed safe operating area.

Switching losses due to MOSFET $P_{loss} = \frac{VI_0(t_{rise}+t_{fall})}{2T}$. (6)

The switching losses can be reduced by decreasing the turn-on and turn-off times. But this requires the use of faster and more efficient switches. Another method would be is to use soft switching techniques like making the current or voltage across the switch zero before turning it ON.

In a conventional SBC, switching loss in the high side MOSFET is the predominant loss followed by the conduction loss of the low side MOSFET [12][13]. Thus, to offer high efficiency, the conduction and switching losses have to be reduced at higher frequencies [14]. The switching losses can be eliminated by available soft switching techniques.

For a SBC, additional losses may also occur during the time between the turn off of high side switch and turn on of the low side switch, when the internal body diode of the MOSFET conducts current. Proper selection of this overlap time determines the balance of "*shoot-through*" with increased power loss.

Power loss on the body diode $P_{bd} = V_F I_0 t_{NO} f_{SW}$,

Where V_F is the forward voltage of the body diode

t_{NO} is the selected non overlap time.

Power losses as a result of power required to turn the switches ON and OFF are dominated the gate charge. This can be minimized by selecting MOSFETs with low gate charge, by driving the MOSFET gate to a lower voltage or by operating at a lower frequency.

$P_{gatedrive} = Q_G V_{GS} f_{SW}$ (7)

Where Q_G is the gate charge of the selected MOSFET

V_{GS} is the peak gate-source voltage.

For N-MOSFETs, the high side switch must be driven to a higher voltage than V_1. Thus V_G must be different for high side and low side switches.

1.5 Solution

As previously discussed, there are two main techniques to eliminate the switching loss i.e. ZVS and ZCS. In both the techniques, the switching losses are eliminated as the current through or voltage across the semiconductor device is zero (while switching.) This allows the circuit to be used at very high frequencies without significantly decreasing converter efficiency. Also, it is seen that the harmonic content in the converter voltage and current waveforms is reduced [15].

Out of the above mentioned techniques, ZVS is the best choice for majority carrier semiconductors because the capacitive turn-on losses can be eliminated and ZCS is the best choice for minority carrier semiconductors [16]. Instead of using a series resonant circuit across the main switch, a shunt resonant circuit is used across the main switch where the parallel circuit is activated just before the turning ON of the main switch and deactivated after the main switch is turned ON. Thus, it achieves ZVS for the main switch and the synchronous switch and ZCS for the auxiliary switch. And it still keeps the advantages of the main switch because after the switching transition is over, the converter circuit works as a normal PWM converter [17][18].

1.6 Dissertation Outline

This chapter provides a discussion of the various drawbacks of a conventional buck converter, the advantages of a synchronous buck converter over a conventional buck converter and also gives an overview of the switching losses in a synchronous buck converter. It also provides a solution to eliminate the switching loss. Chapter 2 presents a analysis of various losses occurring in a synchronous buck converter and mathematically demonstrates that the high side switching loss is the majority player in the total loss of the converter circuit. Chapter 3 proposes the ZVS converter and explains the various modes of operation of the circuit and also designs various parameters of the circuit. Chapter 4 proves the high efficiency of the designed converter via simulation with PSIM and also discusses the superior results of the proposed converter. Chapter 5 summarizes the dissertation and points out the limitation of the circuit. It also proposes the future work in order to overcome the limitations of the proposed work.

CHAPTER **2**

2. Loss Analysis

For an efficient power supply using Buck Converters, switching losses reduction are highly essential. As the conclusion was previously stated that the high side switching loss dominates the low side switching loss, the mathematical analysis is carried out that will validate the need for elimination of high side switching loss.

A SBC is considered which has the following values:

V_s = 15 V

V_o = 3 V

I_o = 10 A

f_s = 500 kHz

MOSFETs used are of the make IRF 1312, having a R_{DSON} = 0.002 Ω [19]

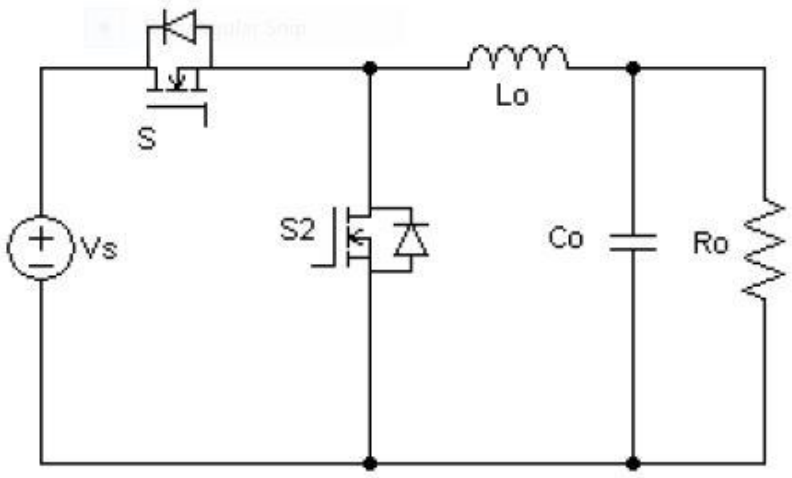

Figure 5: Synchronous Buck Converter

2.1 High Side Losses

Power loss in a MOSFET comprises of the conduction losses and the switching losses [20].

$$P_{HS} = P_{COND} + P_{SW} \quad (8)$$

Calculating Conduction Loss –

$$\text{Conduction loss } P_{COND} = I_0^2 R_{DSON} \times \text{Duty Cycle} = 10\times10\times10^{-3}\times\frac{3}{15} = 0.2W \quad (9)$$

Calculating Switching Loss –

Switching time of a MOSFET can be sub-divided into 5 phases as shown in the given graph:

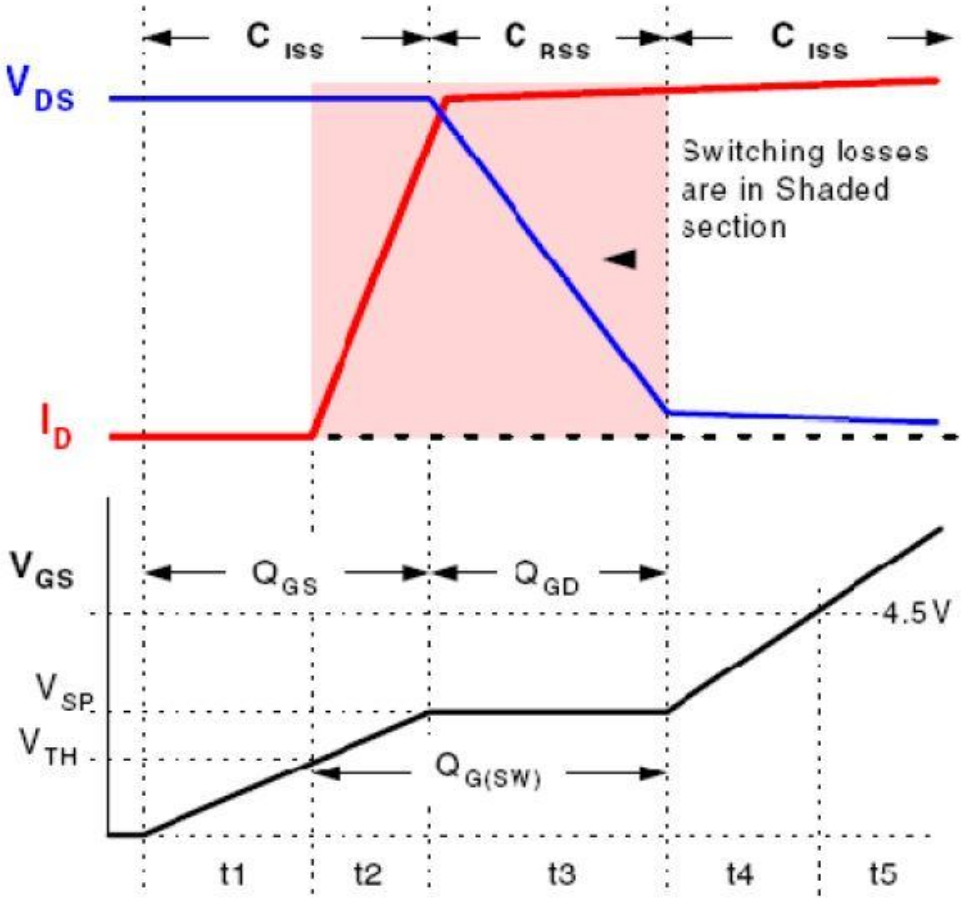

Figure 6: MOSFET Characteristics

Switching loss of a MOSFET is defined as the power loss that occurs in each switching interval, multiplied by the duty cycle of the switching interval.

The top graph shows the voltage across the MOSFET and the current flowing through it. The bottom graph represents V_{GS} as a function of time. This is similar to the shape of Q_G given in the datasheet [19].

Switching begins when the high side MOSFET driver turns ON and begins to supply current to S_1's gate to charge its input capacitance. Switching losses are zero until $V_{GS} = V_{TH}$, thus power loss during time period t_1, $P_{t_1} = 0$.

When $V_{GS} = V_{TH}$, input capacitance is being charged and I_D rises linearly till it reaches the load current I_0. During this period, entire input voltage appears across the MOSFET and energy $E_{t_2} = t_2 \times \frac{V_S I_0}{2}$. (10)

During t_3, I_0 is flowing through S_1 and V_{DS} begins to fall. So the entire gate current starts to recharge C_{GD}. Assuming constant current I_0 flows, V_{DS} starts falling from V_S to zero.

Thus $E_{t_3} = t_3 \times \frac{V_S I_0}{2}$. (11)

During t_4 and t_5, MOSFET is just fully enhancing the channel to obtain its rated R_{DSON} at rated V_{GS}. But the losses during this time are very small compared to t_2 and t_3, where the MOSFET was simultaneously sustain voltage and conducting current. Thus it is ignored in our analysis.

$P_{SW} = \frac{\frac{V_S I_0}{2} t2 + \frac{V_S I_0}{2} t3}{T} = \frac{V_S I_0}{2} (t_2 + t_3) f_s$. (12)

Equivalent Gate Circuit [9]–

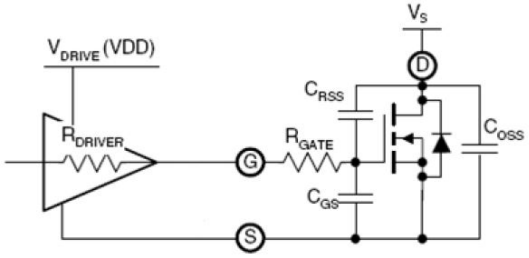

Figure 7: Gate Driver

In order to determine t_2 and t_3, we must know the total time the gate driver circuit takes to deliver all the charge required in a time period.

Since current is charge per time, we can calculate time by $t = \frac{Q_G}{I_{driver}}$. (13)

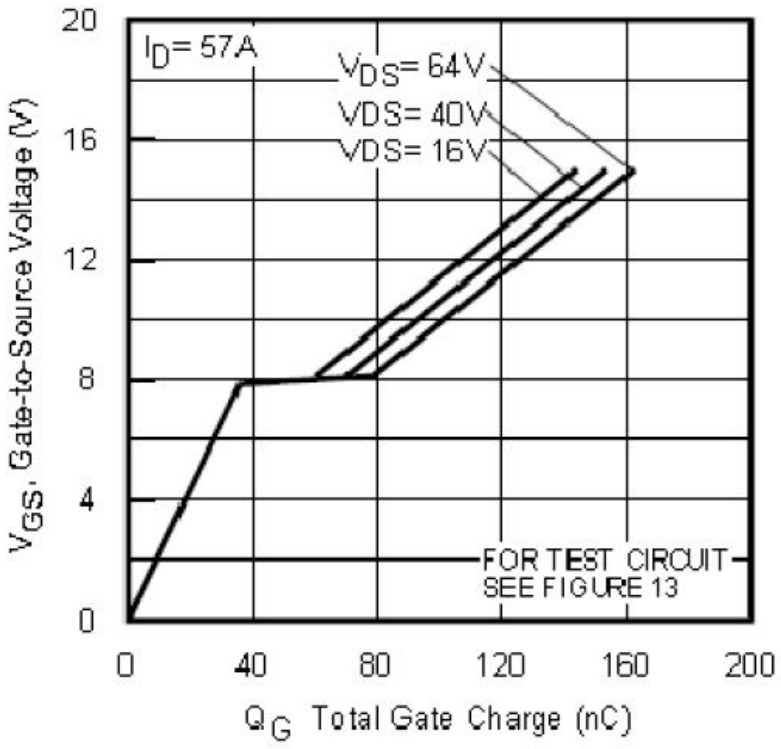

Figure 8: VGS QG Characteristics [19]

From the graph, it is evident that most of the switching time interval is at t_3, where the voltage is denoted as V_{SP}. This value can be calculated from the gate charge graph that is provided in the datasheets [19].

Thus from V_{GS} - Q_G graph, V_{SP} is found to be 8 V (as it is discernible from the graph that V_{SP} does not change significantly with V_{DS} and I_D.

Assumptions of gate driver circuit –

V_{DD} = 10 V

$R_{driver(pull\ up)}$ = 5 Ω

$R_{driver(pull\ down)}$ = 2 Ω

R_{gate} = 1.5 Ω

As V_{SP} = 8 V, gate current can be determined.

While MOSFET is about to start (gate pulse is rising),

$$I_{driver} = \frac{V_{DD} - V_{SP}}{R_{driver(pull\ up)} + R_{gate}} \quad (14)$$

$$= \frac{10-8}{5+1.5} - 0.308 \text{ A.}$$

When the gate signal is falling,

$I_{driver} = \frac{V_{SP}}{R_{driver(pull\ down)}+R_{gate}}$ (15)

$= \frac{8}{2+1.5} = 2.286$ A.

As it was seen that gate current during rising and falling time were different, these have to be treated separately.

Gate charge for a MOSFET to move through the switching interval

$Q_{G_{SW}} = Q_{GD} + \frac{Q_{GS}}{2}$ (from figure) (16)

$Q_{GD} + Q_{GS}$ is known from datasheet [19].

$Q_{GD} \approx 34$ nC, $Q_{GS} \approx 36$ nC

$\therefore Q_{G_{SW}} = 52$ nC

Now switching times can be easily calculated.

For rising time, $t_s = \frac{Q_G}{I_{driver}} = 168.831$ ns $= t_2$. [From (13)]

For falling time, $t_s = \frac{Q_G}{I_{driver}} = 22.747$ ns $= t_3$. [From (13)]

$\therefore P_{SW} = \frac{\frac{V_S I_0}{2} t2 + \frac{V_S I_0}{2} t3}{T} = 7.184$ W. [From (12)]

Total Power Loss = (0.27 +7.184) W = 7.384 W.

2.2 Low Side Losses

The low side losses calculation is similar to the high side loss calculation.

$P_{LS} = P_{SW} + P_{COND}$

Conduction Loss $P_{COND} = I_0^2 R_{DSON} \times (1 - \frac{V_0}{V_S}) = 10^2 \times 10 \times 10^{-3} (1 - \frac{3}{15}) = 0.8$ W.

Switching losses can be neglected since S_2 turns ON and OFF with only a diode across it.

Total power Loss = 0.8 W.

2.3 Gate Driver Loss

Power required to charge the gate $P_{GATE} = \frac{Q_G}{T} \times V_{DD}$ (17)

$\Rightarrow P_{GATE} = 140 \times 10^{-9} \times 500 \times 10^3 \times 10 = 0.7$ W.

This power is independent of the driver's output resistance and includes both the rising and falling edges. It is distributed between R_{driver} and R_{gate} and is proportional to their resistances.

P_{loss} due to rising edge $= \frac{P_{gate}}{2} \times \frac{R_{driver(pull\ up)}}{R_{total}} = 0.269$ W. (18)

P_{loss} due to falling edge = $\frac{P_{gate}}{2} \times \frac{R_{driver(pull\ down)}}{R_{total}}$ = 0.2 W. (18)

Total Power Loss in the driver = (0.269 + 0.2) W = 0.469 W.

The above analysis shows that that out of the 30 W output power of the converter, 7.184 W is the power loss in the high side which constitutes almost 23.947 % of total power whereas only 0.8 W of power loss occurs in the low side which constitutes only 2.667 % of the total power. Thus it is proven that the high side switching loss is large as compared to that of low side and it is highly necessary to minimize this for better performance.

CHAPTER 3

3. Converter Design and Operation

Here, the proposed circuit of single phase Zero Voltage Switching Synchronous Buck Converter [21] is introduced and its detailed operation with relevant waveforms and circuit diagrams is explained. After the operation, the particular design values of the converter is discussed and the device selection criteria is discussed.

3.1 Proposed Converter

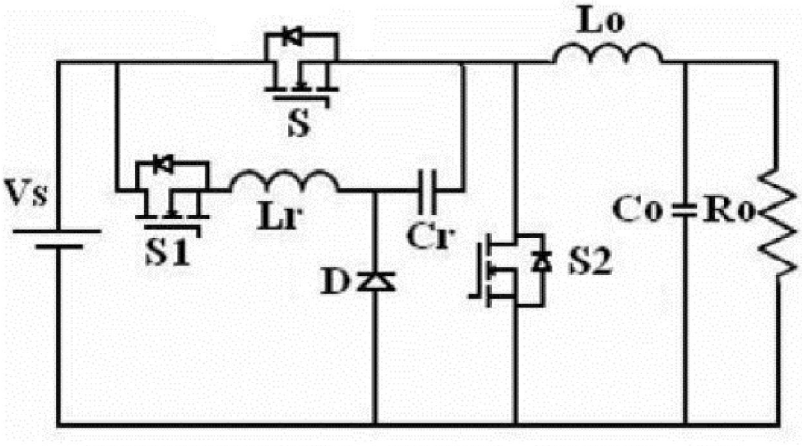

Figure 9: Proposed ZVS SBC

As seen from the figure, the proposed circuit consists of an auxiliary circuit added in parallel to switch, which is the only modification made to a Synchronous Buck Converter (SBC). The auxiliary circuit consists of S_1, L_r and C_r. It operates only for a short time to facilitate Zero Voltage Switching (ZVS) for S. The Schottky Diode D is used to discharge C_r to the load (before S_2 turns on.)

Several assumptions are made to simplify the steady state analysis of the above circuit.

1. V_s is constant.
2. V_0 is constant (i.e. C_0 is high.)
3. I_0 is constant (i.e. L_0 is high.)
4. $L_0 >> L_r$.
5. Reverse recovery times of the diodes are very small and hence they are ignored.

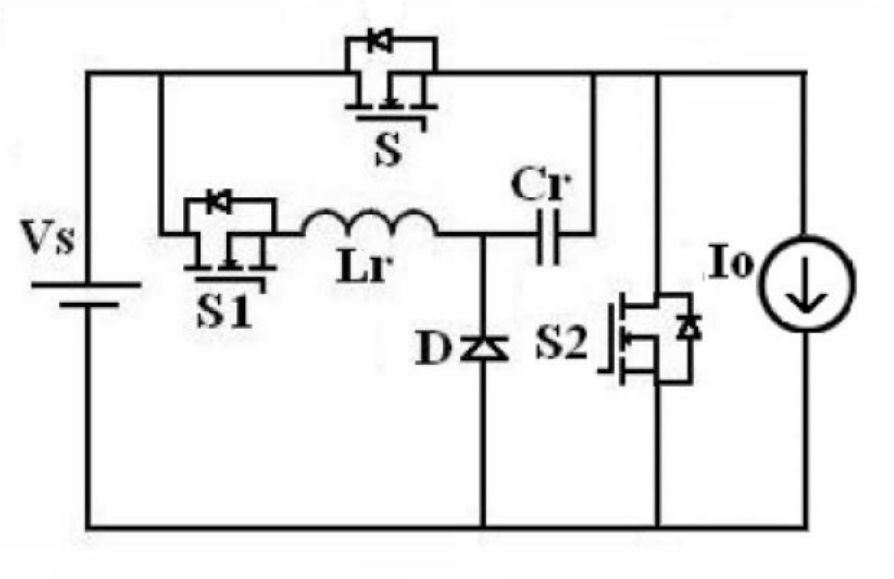

Figure 10: Simplified ZVS SBC

3.2 Modes of Operation

The operation of the above circuit can be understood by dividing into 7 modes.

1. Mode 1 (t_0, t_1): At t_0, S_1 is turned on, but current flowing through S_1 at that instant is 0 due to the presence of L_r. The current flowing through L_r and C_r rise at the same rate as the fall of current through S_2 (S_2 was conducting prior to t_0.) Thus, resonance occurs and this mode ends at t_1 where $i_{Lr} = I_0$ and S_2 turns off.

$$i_{S_2} = I_0 - i_{L_r} \quad (19)$$

$$i_{L_r}(t - t_0) = \frac{V_S}{Z} \sin \omega(t - t_0) \quad (20)$$

$$\omega = \frac{1}{\sqrt{L_r C_r}} \text{ (Resonant Frequency)}$$

$$Z = \sqrt{\frac{L_r}{C_r}} \text{ (Characteristic Impedance)}$$

At $t = t_1$,

$$V_{C_r}(t_1 - t_0) = V_{C_{r_1}} \quad (21)$$

$$i_{L_r}(t_1 - t_0) = I_0 \quad (22)$$

$$t_{01} = t_1 - t_0 = \frac{1}{\omega}\sin^{-1}\frac{I_0 Z}{V_S} \quad (23)$$

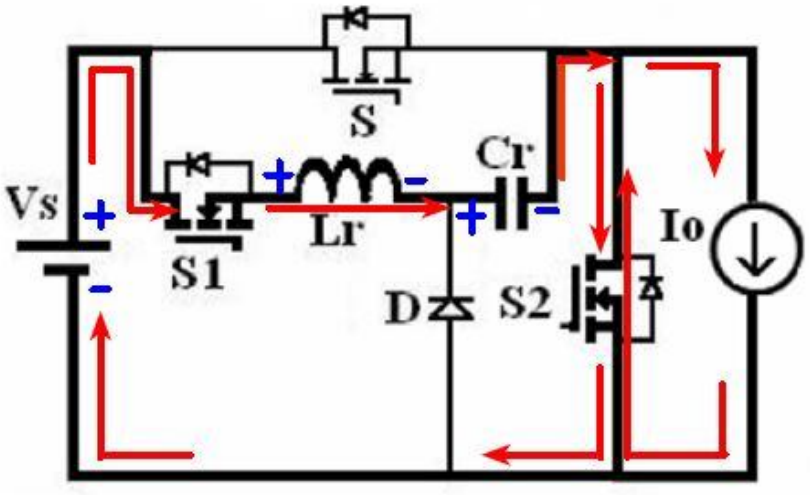

Figure 11: Converter Operation in Mode 1

2. Mode 2 (t_1 to t_2): As L_r and C_r continue to resonate, the current in excess to I_0 flows through the body diode of S, which is responsible for its ZVS turn on. The conduction of the body diode discharges the stray capacitance C_{DS} across S. As the auxiliary circuit is providing the required load, the body diode of S_2 does not conduct thereby saving the loss due to output voltage drop during dead time period as in case of conventional converters. When C_{DS} is discharged, the inductor current gain reaches I_0 and this mode ends.

$$i_{S_2} = 0 \quad (24)$$

$$i_{L_r}(t - t_1) = \frac{V_S - V_{C_{r_1}}}{Z}\sin\omega(t - t_1) + I_0\cos\omega(t - t_1) \quad (25)$$

$At\ t = t_2,$

$$i_{L_r}(t - t_0) = I_0 \quad (26)$$

$$t_{12} = \frac{2}{\omega}\tan^{-1}\frac{V_S - V_{C_{r_1}}}{I_0 Z} \quad (27)$$

$$V_{C_r}(t_1 - t_0) = V_{C_{r_2}} \quad (28)$$

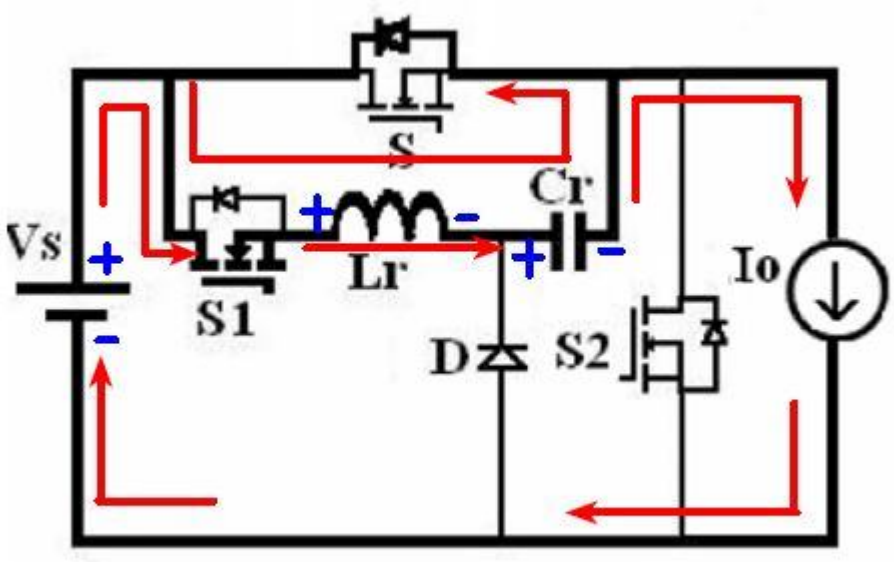

Figure 12: Converter Operation in Mode 2

3. Mode 3 (t_2, t_3): After t_2, S is turned on with ZVS. Now, growth rate of i_S is determined by resonance between L_r and C_r, which continues and i_{lr} begins to decrease. Again, since is turned on when $i_{Lr} = I_0$, body diode of S_2 does not conduct as S_1 is supplying the required output. This mode ends when $i_{Lr} = 0$ and $V_{cr} = V_{cr(max)}$.

$$i_{L_r}(t - t_2) = \frac{-V_{C_{r_2}}}{Z} \sin \omega(t - t_2) + I_0 \cos \omega(t - t_2) \quad (29)$$

$At\ t = t_3,$

$$i_{L_r} = 0 \quad (30)$$

$$t_{23} = \tan^{-1} \frac{I_0 Z}{V_{C_{r_2}}} \quad (31)$$

$$V_{C_r}(t_3) = V_{C_{r(max)}} \quad (32)$$

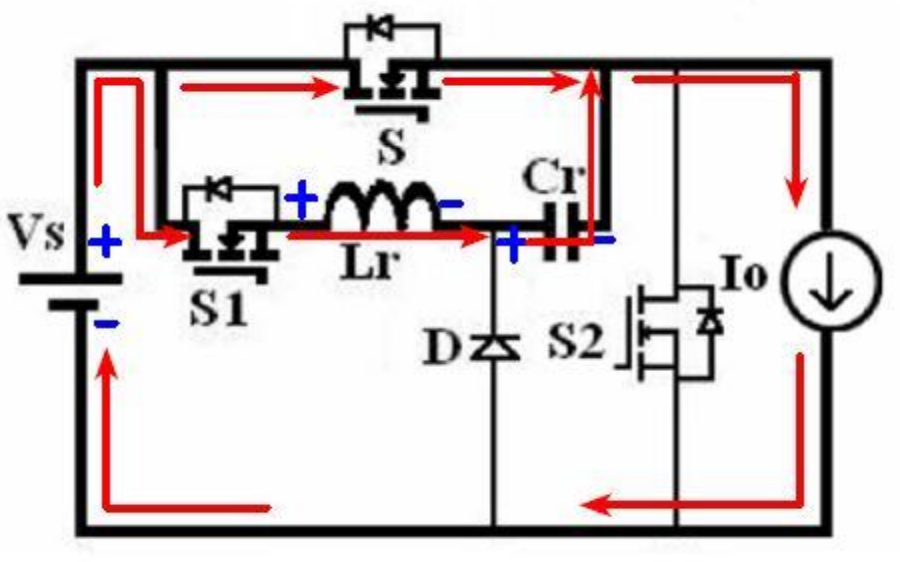

Figure 13: Converter Operation in Mode 3

4. Mode 4 (t_3, t_4): At t_3, S_1 turns off by Zero Current Switching (ZCS). The resonant capacitor C_r starts discharging through the body diode of S_1, which causes i_{Lr} to increase in the reverse direction. i_{Lr} reaches to a maximum negative and then increases to 0. At the end of this mode, body diode of S_1 is turned off and the resonant peak current flowing through the main switch is 0. $V_{Cr} = -V_{Cr(max)}$.

$$i_{L_r}(t - t_4) = \frac{-V_{C_{rmax}}}{Z} \sin \omega(t - t_4) \quad (33)$$

At t = t_4,

$i_{Lr}(t_4) = 0$. (34)

$t_{34} = \frac{\pi}{\omega}$ (35)

$$V_{Cr}(t_4) = -V_{Cr3} \quad (36)$$

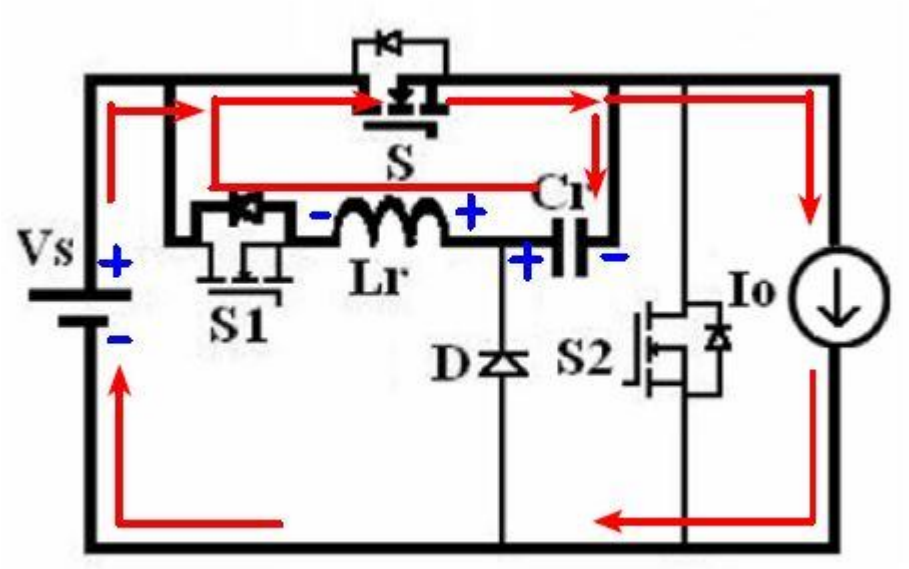

Figure 14: Converter Operation in Mode 4

5. Mode 5 (t_4, t_5): The body diode of S_1 has already turned off at t_4. Now, only S carries the load current. Hence, there is no resonance and the circuit works as a conventional Pulse Width Modulation (PWM) buck converter.

$$i_S = I_0 \quad (37)$$

$$V_{C_r}(t_5) = -V_{C_{r_3}} \quad (38)$$

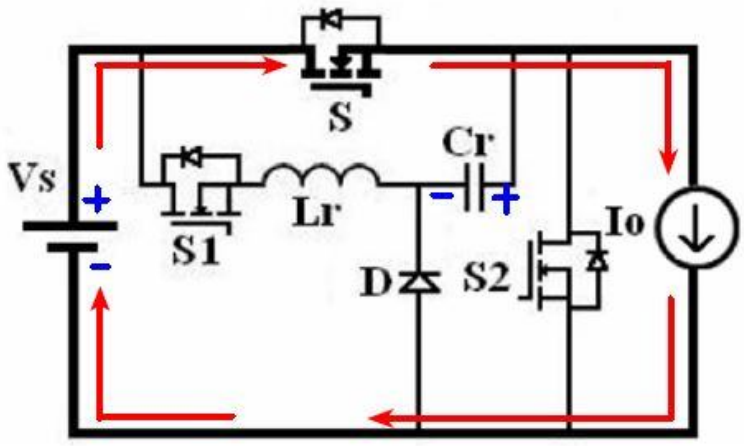

Figure 15: Converter Operation in Mode 5

6. Mode 6 (t_5, t_6): At t_5, S turns off with ZVS and D starts conducting. Resonant energy stored in C_r is transferred to the load through D. This mode lasts till C_r discharges.

$$V_{C_r}(t - t_5) = -V_{C_{r_3}} + \frac{I_0}{C_r}(t - t_5) \quad (39)$$

$$At\ t = t_6,$$

$$V_{C_r}(t_6) = 0 \quad (40)$$

$$t_{56} = \frac{C_r V_{C_{r3}}}{I_0} \quad (41)$$

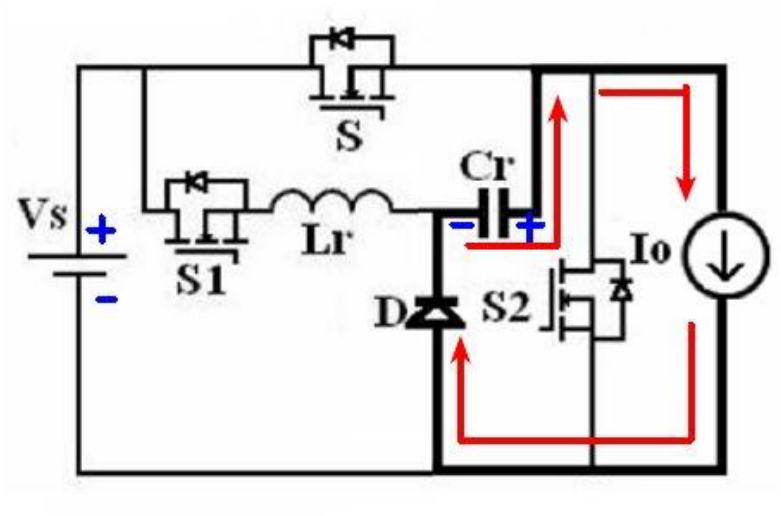

Figure 16: Converter Operation in Mode 6

7. Mode 7 (t_6, t_7): Here, the circuit operates as a conventional PWM buck converter until S_1 is turned on in the next switching cycle.

$$i_{S_2} = I_0 \quad (42)$$

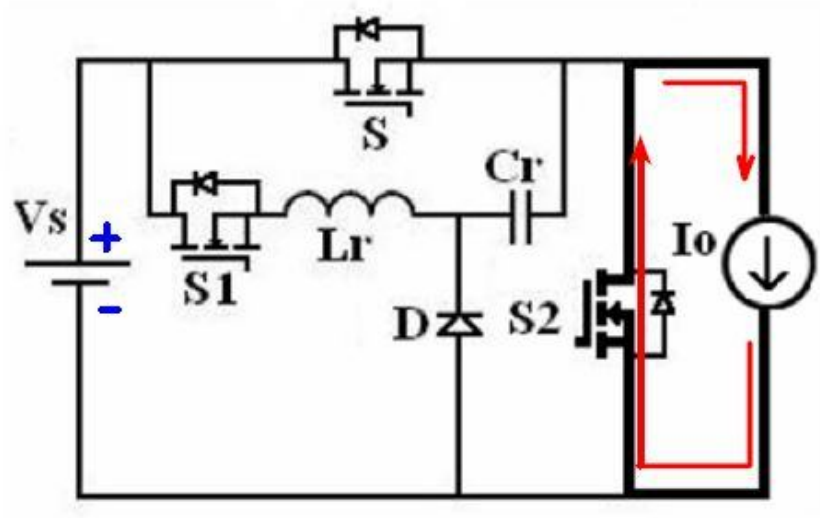

Figure 17: Converter Operation in Mode 7

3.3 Converter Design Procedure

In a conventional SBC, inductor current consists of DC current I_0 and a linear ripple of peak magnitude dI. In a well-designed converter, the DC component I_0 flows only to the load resistance R_0 and the entire inductor ripple current flows through C_0 as it is such designed [5]. Thus choosing high values of L_0 and C_0 gives a ripple free constant output current and voltage at a constant load.

From the operation of the converter, we know that the auxiliary circuit operates only for a short period of time and for the remaining time, the circuit works as a conventional SBC. Hence L_0 and C_0 values are computed as done for a conventional SBC.

Let us design the converter for a 3.3 V, 12 A power supply from a 12 V supply at a switching frequency of 200 kHz.

$$L_0 = \frac{(V_S - V_0) d T_S}{2\Delta i_L} \quad (43)$$

Assuming a 5% current ripple, L_0 comes out to be 9.969 µH ≈ 10 µH.

Similarly, $C_0 = \frac{\Delta i_L T_S}{8\Delta V_C}$ (44)

C_0 comes out to be 113.64 µF ≈ 110 µF.

The auxiliary circuit turns on before the main switch and turns off after the main switch is turned on. During the period in between, the resonant inductor is charged to I_p, which is generally designed to be higher than I_0.

V_S forces current to flow and hence charge L_r and C_r till time t_2 i.e. till inductor current charges to I_p.

$$i_{L_r}(t) = I_p \sin \omega t \quad (45)$$

$$I_p = V_S \sqrt{\frac{C_r}{L_r}} \quad (46)$$

For our assumed values, let I_p be 12.2 A (> I_0)

So, $C_r = 1.0336 L_r$ (47)

$t_p = \frac{\pi}{2\omega}$ (48)

As f_s = 200 kHz, T_s = 5 µs.

Assuming S is turned on at 0.4166 µs (30° of 360°, one switching cycle) and the peak value occurs at t_p = 0.375 µs, we get L_r = 231.09 nH ≈ 230 nF.

C_r comes out to be 238.85 nF ≈ 240 nF (from equation 47)

3.4 Selection of Devices

3.4.1 Mosfet Selection

The obvious dilemma while selecting MOSFET arises whether to use a n-channel MOSFET or a p-channel MOSFET. So let us ponder about the advantages and disadvantages of each.

n-channel MOSFET –

Advantages:

1. Lower R_{DSON} for a given die size and lower gate charge.
2. Inexpensive.

Disadvantage: It requires a bootstrapped drive circuit or a special bias supply for the driver to work.

p-channel MOSFET –

Advantages:

1. The gate driver arrangement required is simple.
2. The gate is pulled down a few volts below the input voltage to turn on.

Disadvantages:

1. Cost is higher for an equivalent R_{DSON}.
2. Switching times are slower.

Thus for an efficient power supply and to minimize switching losses, an n-channel MOSFET with very low R_{DSON} is preferred.

3.4.2 L and C selection

Inductor value depends on switching frequency, transient performance and conduction losses in inductor and other components.

Benefits of low L values:

1. Low DCR – low DC inductor losses in windings.
2. Fewer turns – higher DC saturation current.
3. High $\frac{dI}{dT}$ – faster response to load step/dump.
4. High $\frac{dI}{dT}$ – fewer output capacitors required for good load transient recovery.

Benefits of high L values:

1. Low ripple – lower AC inductor losses in core and windings.
2. Low ripple – lower conduction losses in MOSFETs.
3. Low ripple – lower RMS ripple current for capacitors.
4. Low ripple – continuous inductor current flow over wider load range.

In general, lower inductor values are best for high frequency converters, since the peak to peak ripple current decreases linearly with switching frequency. A good decision would be to select an inductor that produces around 10% to 20% ripple of full load DC current.

Too large an inductance value leads to poor loop response, and too small an inductance value leads to high AC losses. The capacitor value is chosen based on L. High capacitance gives fewer ripples and vice versa.

CHAPTER 4

4. Simulation Results and Discussion

This section reveals the simulation results of the proposed synchronous buck converter model. The parameters have been taken for simulation study is given in the appendix.

Figure 18 shows the switching waveform of S in SBC.

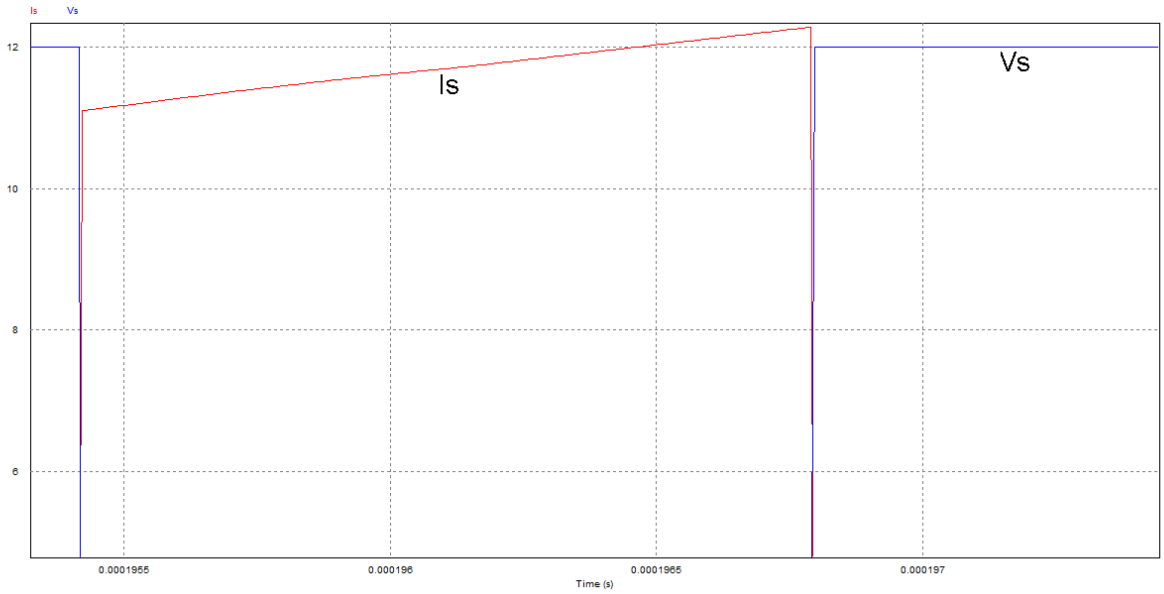

Figure 18: Switching waveform of S in SBC

Figure 19 shows the enlarged version of S in SBC.

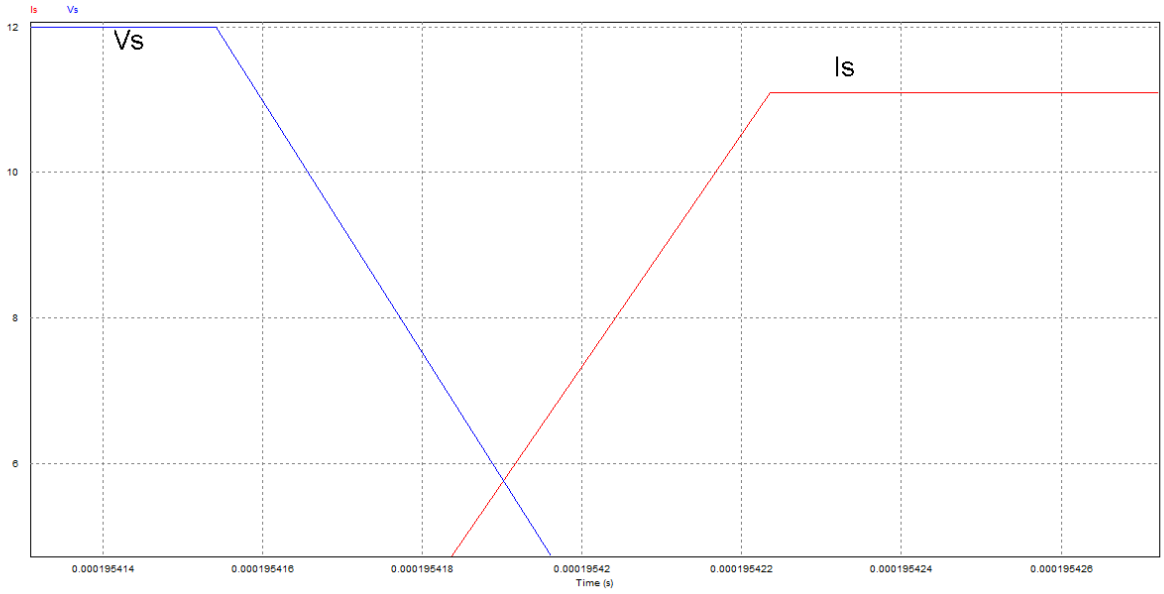

Figure 19: Enlarged waveform of S in SBC

Figure 20 shows the switching waveform of S in ZVS SBC.

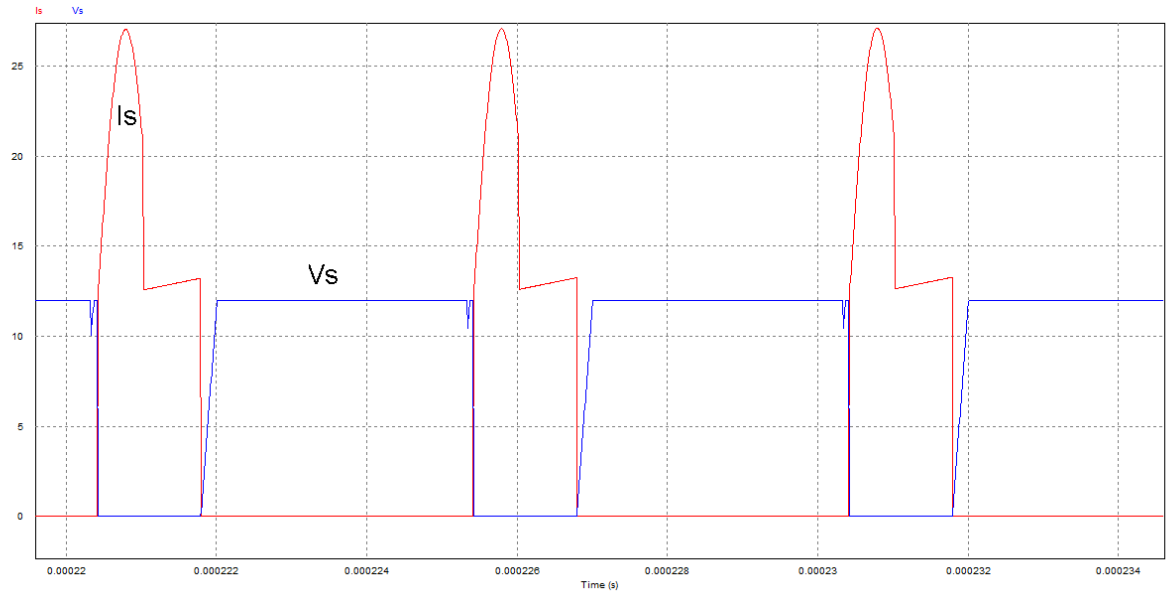

Figure 20: Switching waveform of S in ZVS SBC

Figure 18 and Figure 19 show the switching loss suffered by switch S from its switching action. Figure 20 shows that the switching loss is absent in case of a ZVS SBC. The only issue arising from the ZVS SBC is the rising of the peak current, which increases the conduction loss to 0.801 W as opposed to the conduction loss of 0.396 W in a SBC. Also, switching loss in SBC is 1.847 W and for ZVS SBC, it is negligible. It is seen that switching loss increases with frequency. Since S_1 conducts only for a short period of time, the conduction losses appearing across it is negligible. Taking all these factors into account, it is seen that a ZVS SBC is more efficient than a SBC.

Figure 21 shows that S_1 is also devoid of switching loss.

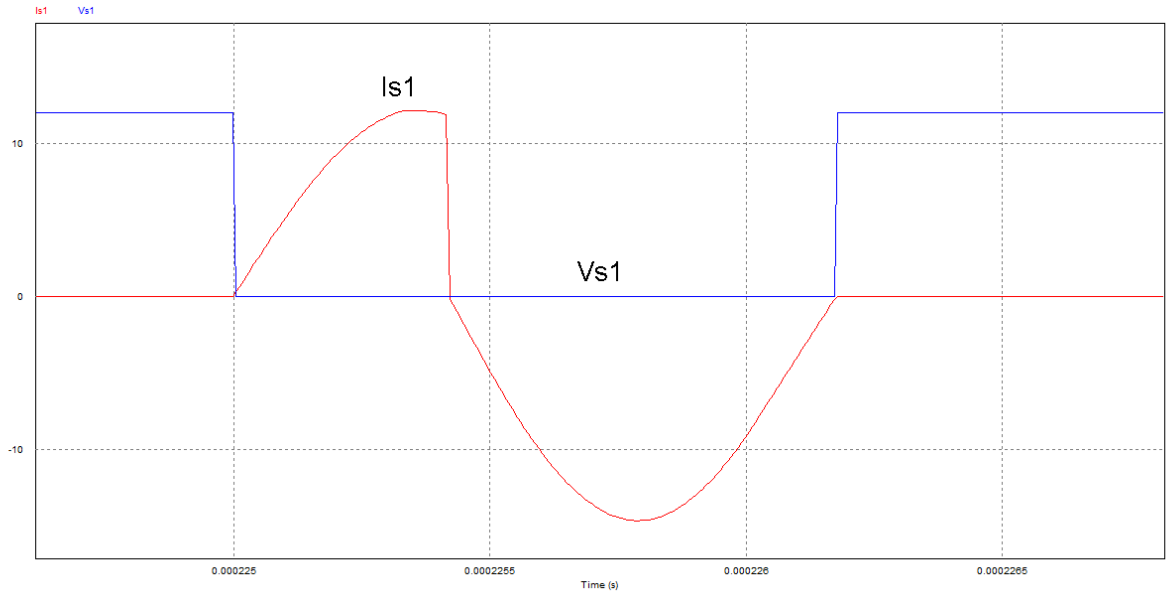

Figure 21: Switching waveform of S1

Figure 22 and Figure 23 shows the switching waveform of S_2 and the resonant voltage across the capacitor V_{cr}.

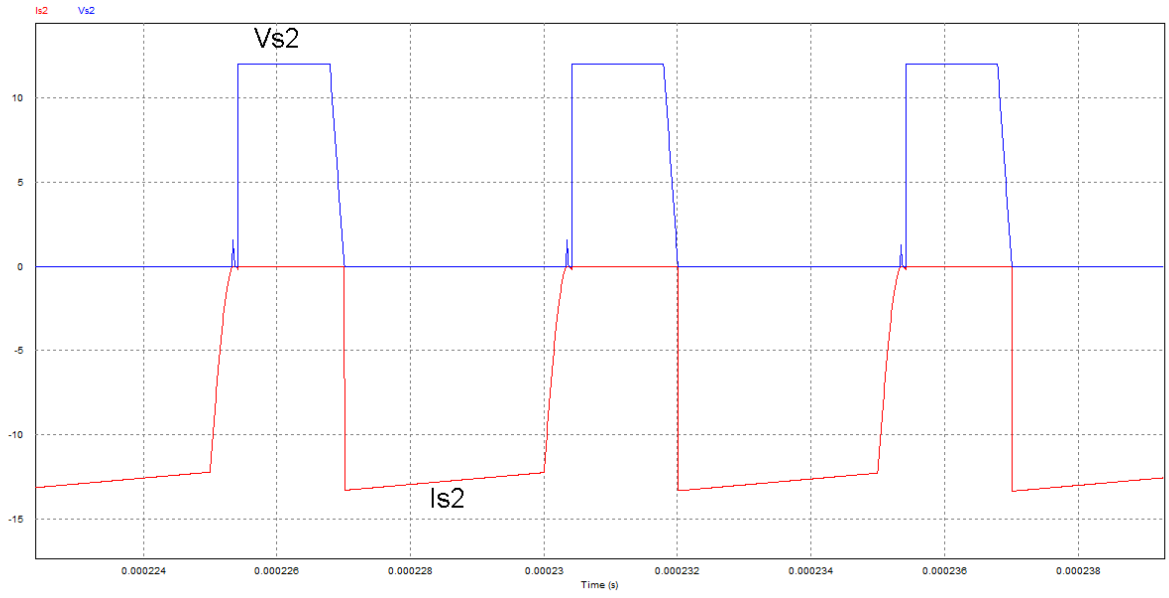

Figure 22: Switching waveform of S2

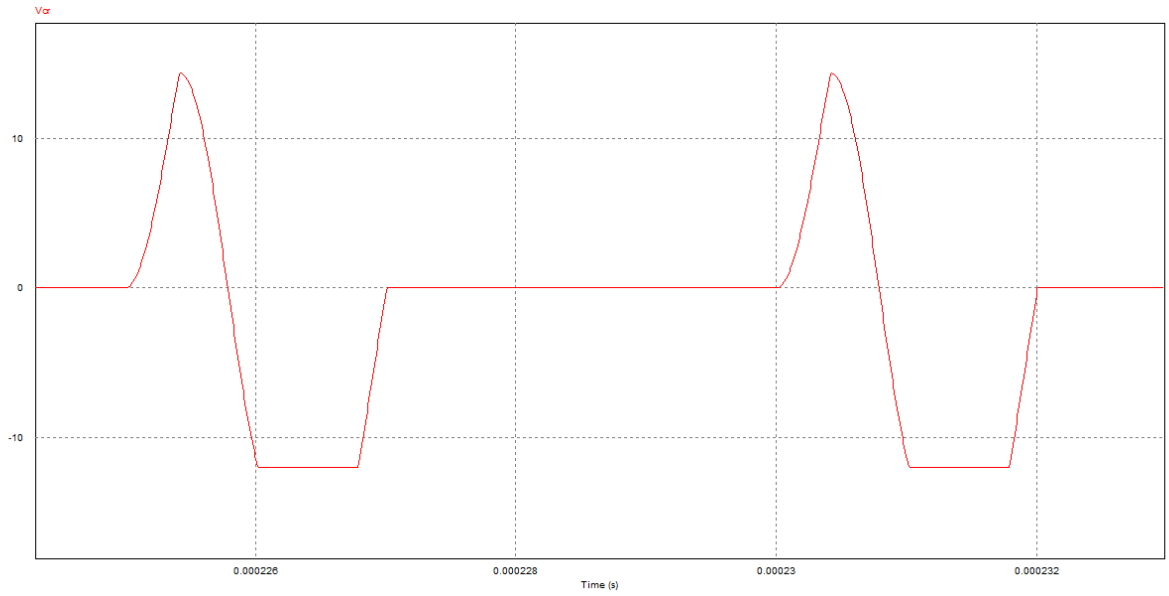

Figure 23: Voltage across capacitor Vcr

Figure 24 and Figure 25 shows the ripple current through the capacitor and inductor respectively. This proves the tolerant output voltage of the power supply as all of the current flowing through the inductor flows through the capacitor and the output load current remains almost constant.

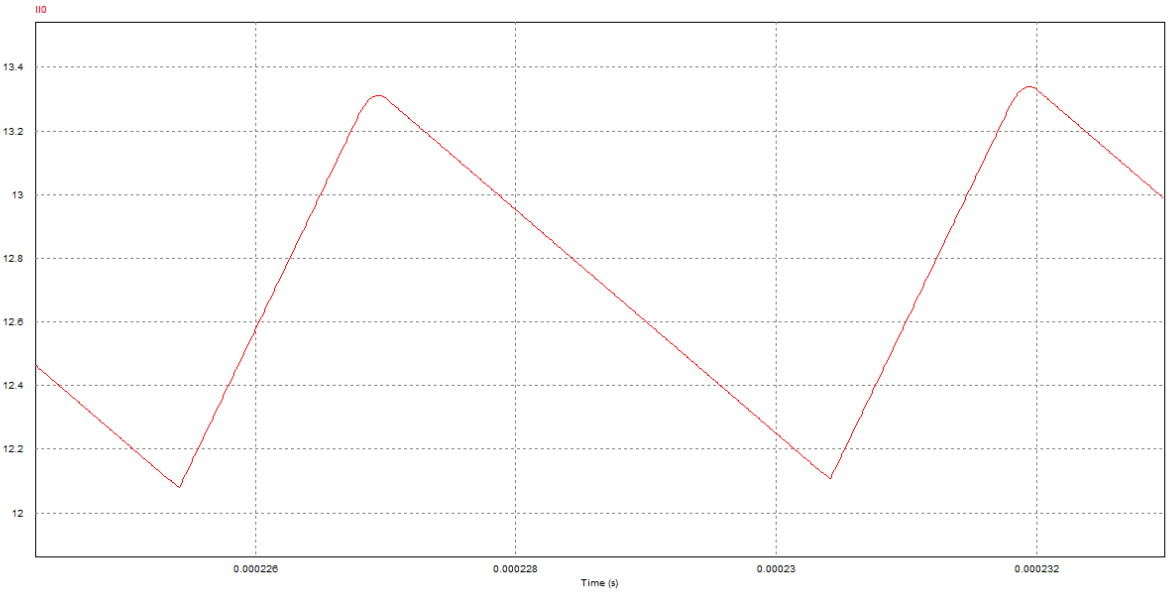

Figure 24: Ripple current through inductor L0

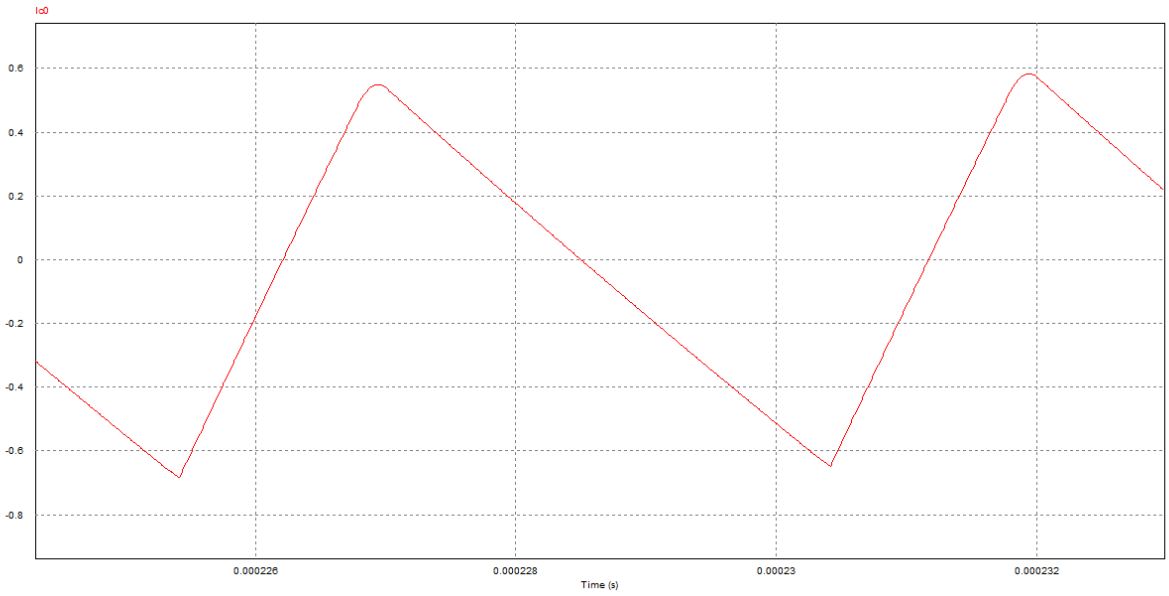

Figure 25: Ripple current through inductor C0

Figure 26 and Figure 27 shows the output voltage and output current respectively.

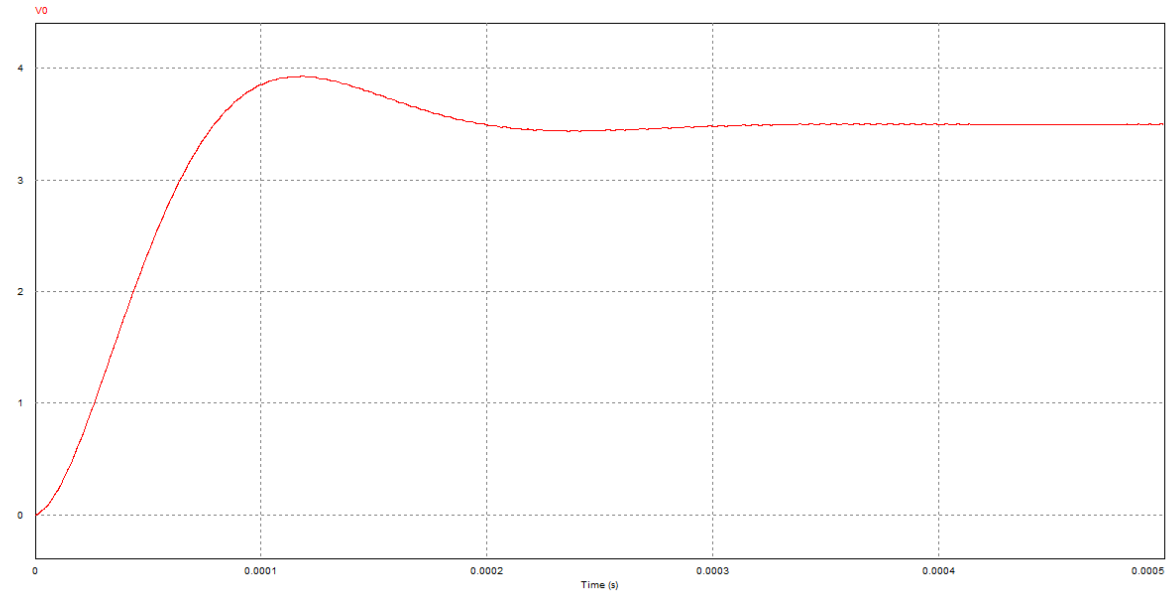

Figure 26: Output Voltage

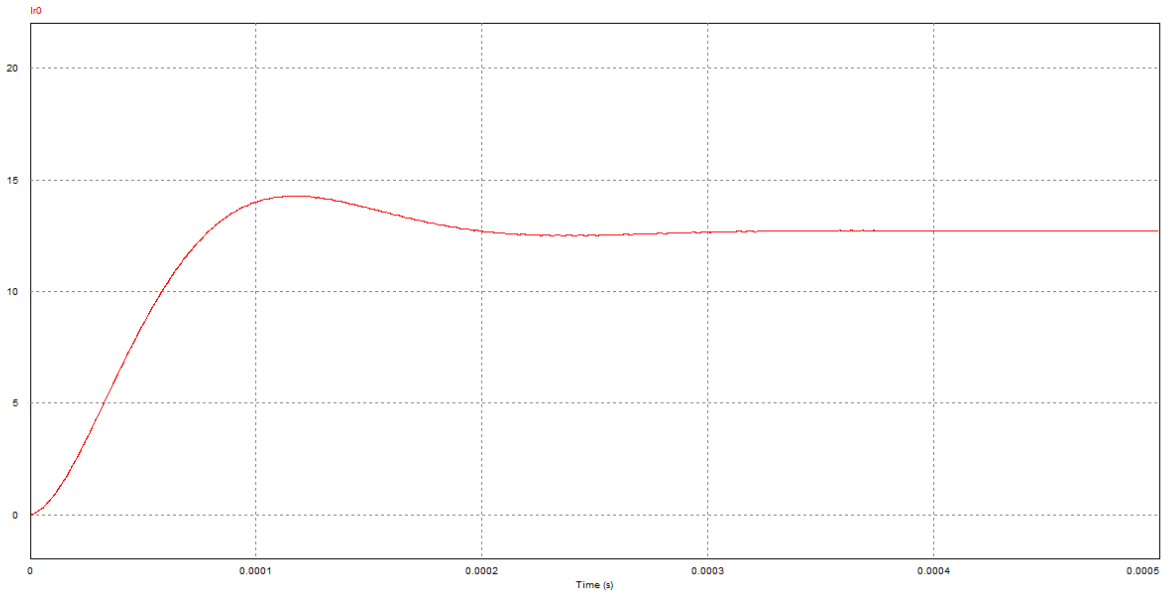

Figure 27: Output Current

CHAPTER 5

5. Conclusion and Future Work

5.1 Conclusion

With the various researches going on to reduce the size of microprocessors by increasing the number of switches (transistors) and increasing the clock frequency, elimination of switching losses in order to increase the efficiency has become the need of the hour. Therefore, this work focuses on developing a highly efficient power supply to power the microprocessors used in the market.

This dissertation focuses on the various alternative circuits to supply power, their various drawbacks and also offers a solution to select a synchronous buck converter in place of a conventional buck converter. It also carries out an analysis of the various losses occurring in a synchronous buck converter and models a Zero Voltage Switching (ZVS) SBC for portable applications.

From the mathematical analysis carried out in Chapter 2, it was seen that the high side losses dominates the low side losses in case of a synchronous buck converter. Hence, this work focuses on eliminating the high side losses with the help of ZVS in order to increase the efficiency of the power supply.

Following the results obtained from the analysis, a ZVS SBC is modelled to eliminate the high side switching losses of the SBC by using a resonant circuit in parallel with the main switch. Then this model is simulated for a 12 V input, 3.3 V output, 12A current output and at a frequency of 200 kHz. From the simulation results it can be concluded that none of the switches suffer from switching loss.

Finally, it can be concluded that eliminating the switching loss using ZVS occurring in power semiconductor devices is a promising solution to increase the efficiency of the power supply. It can even be used to power present and future generation processors.

5.2 Future Work

For high current devices, several ZVS SBC circuits can be used in parallel to form a ZVS MSBC supply. This supply can meet the current requirement of such devices. But this advantage comes at a cost of higher price and size of the converter. Thus, a single auxiliary circuit can be designed for any number of phases (parallel circuits) used. But it also has several disadvantages like:

1. While the auxiliary circuit operates, some current flows through the body diodes of all the switches that are not conducting.
2. If we design a logic circuit to rule out the above problem, the converter circuit becomes too complex.

Solving the above mentioned issues is a challenge to power supply design engineers. It may also result in a further high efficiency power supply, which is not achieved in this work.

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