Stability Analysis and Compensator design for Cascaded Converters

A Thesis Submitted in Partial Fulfilment

for the Award of the Degree of

Master of Technology

in Electrical Engineering with Specialization in

Control & Automation

by

B Raghuma Reddy

Department of Electrical Engineering

National Institute of Technology, Rourkela

2011-2013

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B Raghuma Reddy

(211EE3331)

Under the Supervision of

Prof. Susovon Samanta

Department of Electrical Engineering

National Institute of Technology, Rourkela

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Department of Electrical Engineering

National Institute of Technology Rourkela

Certificate

This is to certify that the Thesis entitled, ***"Stability Analysis and Compensator design for Cascaded Converters"*** submitted by ***"B Raghuma Reddy"*** to the National Institute of Technology Rourkela is a bonafide research work carried out by him under my guidance and is worthy for the award of the degree of **"Master of Technology"** in Electrical Engineering specializing in **"Control & Automation"** from this institute. The embodiment of this thesis is not submitted in any other university and/or institute for the award of any degree or diploma to the best of our knowledge and belief.

Date:

Place:

Prof. Susovon Samanta

Assistant Professor

Department of Electrical Engineering

Supervisor

ACKNOWLEDGEMENTS

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Last, but not the least, I would like to dedicate this thesis to my family, for their love, patience, and understanding.

B Raghuma Reddy
211EE3331

ABSTRACT

The present work deals with the modeling and the stability of the cascade converters. When a converter tightly regulates its output, it behaves as a constant power load (CPL). The problem of CPLs is that they show negative incremental resistance that causes instability in the system. Hence the CPL has been modeled and linearizaed to study its effect on the source converter. On this basis, it was found that because of the negative resistance exhibited by the CPL, the control to output transfer function possessed a RHP pole and thus makes system unstable. The effect of the introduction of small resistance in series with inductor of source converter on the stability was analyzed. Also the compensation on the basis of the passive components i.e. snubbers were designed so as to reduce the power dissipation due to the resistance. Type III compensation was designed by taking the input impedance of the load converter as the load for the source converter using K factor method. Further, based on input impedance, minor loop gain concept was used for stabilizing the system.

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LIST OF ABBRIVATIONS

DC Direct Current

CPL Constant power load

DPS Distributed power system

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CHAPTER 1

INTRODUCTION TO CASCADED CONVERTERS

CHAPTER 1

INTRODUCTION TO CASCADED CONVERTERS

1.1 Introduction

Multi-converter power electronic systems find its application in a number of scenarios for electric power distribution such as space vehicles, hybrid electric vehicles etc. Usually they consist of multiple numbers of the converters and inverters connected between different buses. Therefore the overall size and hence the complexity of such a distribution system is very high and hence the design task of such a system is not carried out as a whole rather it is divided into a number of subsystems consisting of the single converters assuming to be operating as a standalone system. The designed standalone system is then integrated in order to form the overall power electronic system. However, there arises an inherent instability problem in such an integrated system due to the interaction between different subsystems, which were designed as a stable system assuming that they are standalone. Hence, in the multi converter electronic system instability can be induced due to the loading of the other converter subsystems. When a converter or an inverter tightly regulates its output, it behaves as a constant power load (CPL). One of the basic problems associated with the CPL's is that exhibit negative incremental resistance and hence negative impedance and therefore causes system instability. In this work, a linearized model for the CPL has been developed, and on the basis of this the stability analysis of the control to output transfer function has been done. On this basis it was found that because of the negative resistance exhibited by the CPL, the control to output transfer function possessed a RHP pole and thus making it unstable. Based on the transfer function analysis, it was found that the compensation could be provided by the small resistance in the series with the inductance if the source converter. However, the introduction of the resistance causes power dissipation, and hence reduces the efficiency of the system. Therefore the compensation based on based on the passive components (snubbers) was implemented. However, the snubbers consisted of the more no of components and are associated with more number of complexities. Further, the input impedance of the cascaded converters as derived by the two different approaches in this work was found to exhibit frequency dynamics. Type III compensation was designed by taking the input impedance of the load converter as the load for the source converter using K factor method. The stability analysis based on the input and output impedance was done based on the minor loop gain.

1.2 Literature Survey

The characteristics of cascaded converters and the related stability problem have been presented in [1]. At the subsystem level, the dynamics of buck converter with a constant power load has been reported in [2]. Further [3],[4] presents the State space averaging method of the DC DC buck converter and the control to output transfer functions has been designed in it. The buck converter model for the same has been developed in the Simulink in [5].Mathematical calculation of input and output impedance of closed loop converter has been done in [6]. Dynamic profile of

switched mode converter or the cascaded converters has been investigated in [7]. Issues in dynamic analysis and design of interconnected DC-DC power supply system reveals that the input impedance of such a system exhibits some dynamics with the frequency and it is not constant [8]. Further, the stability of two stage distributed power system by using minor loop gain technique has been investigated in [9]. The minor loop gain concept has been used for the impedance criteria for the system stability in [10]. Hence using the design of the compensator by K factor method for the satisfying the desired impedance criteria was developed in [11], [12].

1.3 Motivation

With the development of renewable energy, DC distribution power system (DPS) becomes more and more attractive. The stability of whole system is still a big concern though every single converter is well designed based on the stand-alone operation with sufficient stability. Since the cascaded connection of power converters is one of the most dominant connection forms in the DC DPS, the stability analysis of the cascaded system is very important to ensure stability of the whole system. Tightly regulated closed-loop converters are problematic when used as a load since they tend to draw constant power and exhibit negative incremental resistance. This negative resistance causes stability problems for the feeder system, whether it is an input filter or another converter. This work aims at modeling and stabilizing the cascaded converters by employing different compensation techniques and analyzing its effects on their performance.

1.4 Objectives

The following are the objectives of the thesis.

- To study characteristics of the cascaded converters
- To study modeling of the DC DC converter and linearization of the CPL
- To calculate input impedance of the closed loop converter
- To study minor loop gain concept for stabilizing the cascaded converters
- To design Type III compensator for cascaded converters

1.5 Thesis Organization

The work in thesis is organized into six chapters which are discussed below.

Chapter 1. Provides introduction to cascaded converters.

Chapter 2. Provides modeling and linearization of cascaded converters.

Chapter 3. Provides input and output impedance of the closed loop converter.

Chapter 4. Provides stability analysis of cascaded converters.

Chapter 5. Provides compensator design for cascaded converters.

Chapter 6. Concludes the work with scope for future work.

CHAPTER 2

MODELING AND LINEARIZATION OF CPL

CHAPTER 2

MODELING AND LINEARIZATION OF CPL

2.1 Modeling of Cascaded Converters

When tightly regulated closed-loop converters used as a load, they tend to draw constant power and exhibit negative incremental resistance. This negative resistance causes stability problems for the source converter.

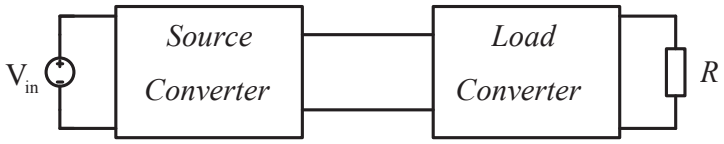

Fig 2.1: Block Diagram of Cascaded Converters.

Representing cascaded converters in terms of components

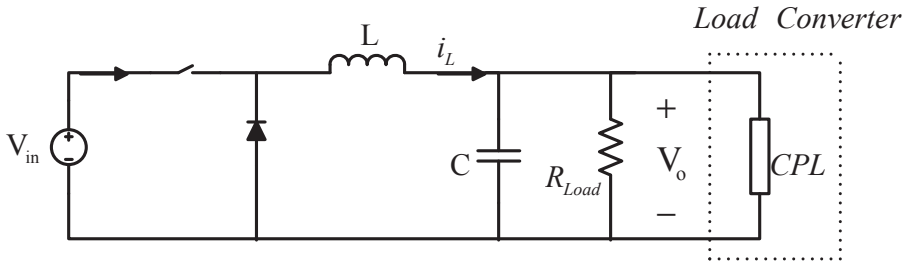

Fig 2.2: DC-DC Buck Converter loaded by a CPL.

Fig 2.2 shows buck converter loaded by another buck converter, tightly regulated converter represents constant power load (CPL).

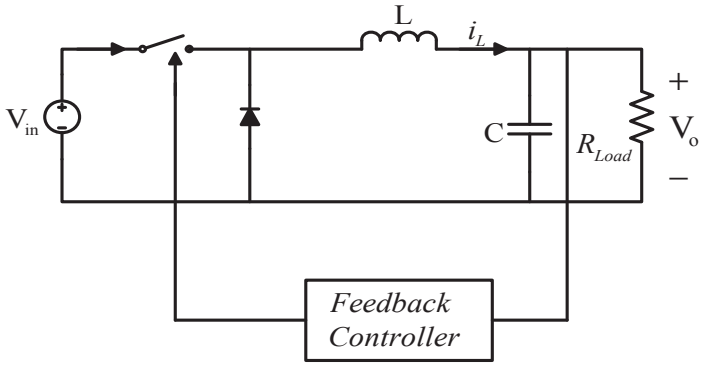

Fig 2.3: Tightly regulated DC/DC buck converter.

2.1.1 Linear Model of a CPL

Consider a tightly regulated converter shown in Fig 2.3. If the output load of the converter is constant and the converter tightly regulates its output voltage, then whatever the input voltage is, the output voltage will be constant. It means that, the output power of the converter is constant at $P_{out} = V^2_{out}/R$. If we assume that by changing the input voltage of the converter the efficiency does not change significantly, the input power would be constant and equal to $P_{in} = P_{out}/\eta$. To use the linear control methods to solve the problem, it is required to have a linear equivalent model for a CPL around the operating point. For a CPL, we can write

$$i = \frac{P}{v} \tag{2.1}$$

For a given operating point (I = P/V), the rate of change in current can be obtained from (2.1) as follows:

$$\frac{\partial i}{\partial v} = -\frac{P}{V^2} \tag{2.2}$$

So, the curve representing the voltage versus current for a CPL can be approximated by a straight line that is tangent to the curve at the operating point. The equation for this line (current) is given as follows

$$i = -\frac{P}{V^2}v + 2\frac{P}{V} \tag{2.3}$$

Equation (2.3) implies that at a given operating point, a CPL can be approximated by a negative resistance parallel with a constant current source as follows:

$$R_{CPL} = -\frac{V^2}{P_{CPL}} \tag{2.4}$$

$$I_{CPL} = 2\frac{P}{V} \tag{2.5}$$

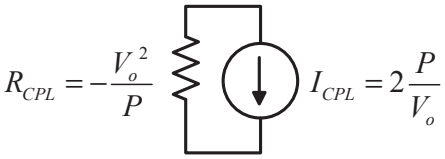

Fig 2.4: Equivalent representation of CPL.

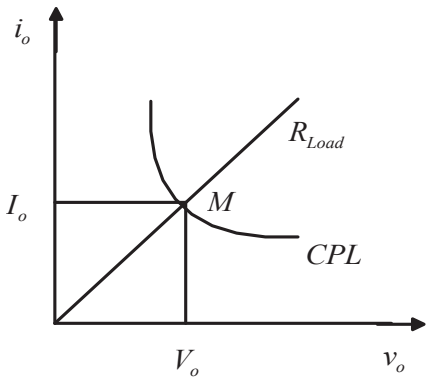

Fig 2.5: Characteristics of CPL.

Replacing equivalent circuit of CPL in fig 2

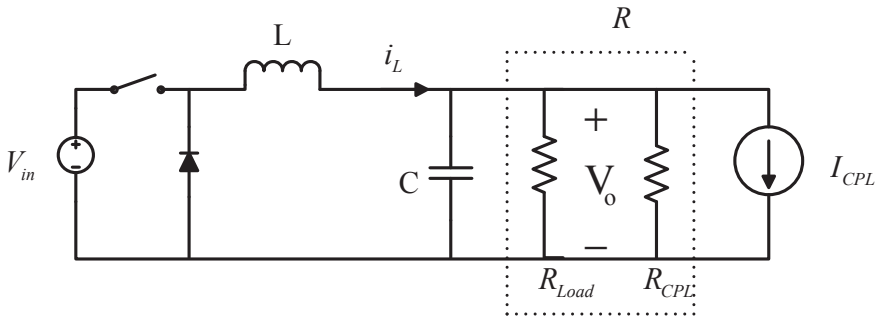

Fig 2.6: Buck and CPL replaced with their equivalent model.

Consider a cascaded configuration in which a feeder converter is loaded by another converter that acts like a CPL. In addition, without losing the generality of the discussion, suppose that the feeder is an open-loop buck converter in CCM. To understand the effect of the CPL to the feeder system (source converter) we have to derive control to output transfer function, so using state average method we can derive transfer functions.

2.2 State Space Description of Buck Converter

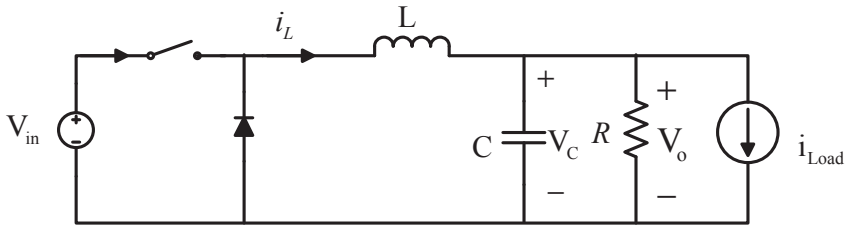

Fig 2.7: The circuit of the buck converter.

2.2.1 State Space Description When Switch in ON State

When switch is on, the equivalent circuit of the buck converter as follows

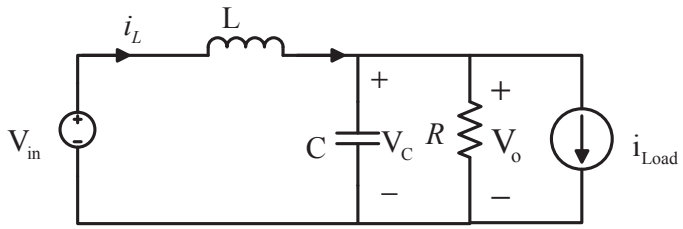

Fig 2.8: The buck converter when switch is ON state.

ON State

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{Load} \end{bmatrix}$$

$$v_o = v_C \tag{2.6}$$

$$v_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{Load} \end{bmatrix}$$

State space system when switch is ON state

$$\begin{aligned} \dot{x}(t) &= A_1 x(t) + B_1 u(t) \\ y(t) &= C_1 x(t) + E_1 u(t) \end{aligned} \tag{2.7}$$

$$A_1 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \qquad B_1 = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} \quad C_1 = \begin{bmatrix} 0 & 1 \end{bmatrix} \quad E_1 = \begin{bmatrix} 0 & 0 \end{bmatrix} \tag{2.8}$$

2.2.2 State Space Description When Switch in OFF State

When switch is off, the equivalent circuit of the buck converter as follows

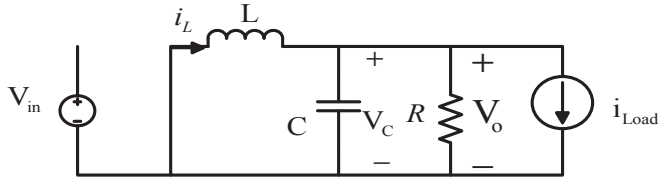

Fig 2.9: The buck converter when switch is OFF state.

OFF State

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} R_L & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{Load} \end{bmatrix}$$
$$v_o = v_C \qquad (2.9)$$
$$v_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{Load} \end{bmatrix}$$

State space system when switch is OFF State

$$\dot{x}(t) = A_2 x(t) + B_2 u(t)$$
$$y(t) = C_2 x(t) + E_2 u(t) \qquad (2.10)$$

$$A_2 = \begin{bmatrix} R_L & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad B_2 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} \quad C_2 = \begin{bmatrix} 0 & 1 \end{bmatrix} \quad E_2 = \begin{bmatrix} 0 & 0 \end{bmatrix} \qquad (2.11)$$

2.2.3 State-Space Average Method

The converter behaves like switching between the two different linear time-invariant systems (2.7) and (2.10) during the switching period, so it looks like a time-variant system. State-space averaging will be used in the next subsection to approximate this time-variant system with a linear continuous time time-invariant system. The first step is calculating a nonlinear time-invariant system by means of averaging and the second step is linearizing this nonlinear system.

The two linear systems are first averaged with respect to their duration in the switching period:

$$\frac{dx(t)}{dt} = (d(t)A_1 + (1-d(t))A_2)x(t) + (d(t)B_1 + (1-d(t))B_2)u(t)$$
$$y(t) = (d(t)C_1 + (1-d(t))C_2)x(t) + (d(t)E_1 + (1-d(t))E_2)u(t) \qquad (2.12)$$

(2.12) is an approximation of the time-variant system and new variable names should formally have been used. To limit the number of variable names, this is not made. The duty cycle, d(t), is an additional input signal in (2.12). A new input vector is therefore defined.

$$u'(t) = \begin{bmatrix} u(t) \\ d(t) \end{bmatrix} \qquad (2.13)$$

A nonlinear time-invariant system with state vector x(t), input vector u'(t), and output vector y(t), are written as

$$\frac{dx(t)}{dt} = f(x(t), u'(t))$$
$$y(t) = g(x(t), u'(t)) \tag{2.14}$$

Apply linearization method, where we can define the deviations at operating point as follows:

$$x(t) = X + \hat{x}(t)$$
$$u'(t) = U' + \hat{u}'(t) \tag{2.15}$$
$$y(t) = Y + \hat{y}(t)$$

The operating-point (DC, steady state) can be denoted by capital letters and perturbation (ac) signals can be denoted by the hat-symbol (^). Assume the operating point is at equilibrium point, i.e.

$$f(x(t), u'(t))\big|_{\substack{x(t)=X \\ u'(t)=U'}} = 0 \tag{2.16}$$

The operating point output values are

$$Y = g(x(t), u'(t))\big|_{\substack{x(t)=X \\ u'(t)=U'}} \tag{2.17}$$

The following linearized (ac, small-signal) system can now be obtained from (2.14) (Goodwin, Graebe and Salgado, 2001, Section 3.10) :

$$\frac{d\hat{x}(t)}{dt} = A'\hat{x}(t) + B'\hat{u}'(t)$$
$$\hat{y}(t) = C'\hat{x}(t) + E'\hat{u}'(t) \tag{2.18}$$

Where

$$A' = \left[\frac{\partial f}{\partial x}\right]_{\substack{x(t)=X \\ u'(t)=U'}}$$
$$B' = \left[\frac{\partial f}{\partial u'}\right]_{\substack{x(t)=X \\ u'(t)=U'}}$$
$$C' = \left[\frac{\partial g}{\partial x}\right]_{\substack{x(t)=X \\ u'(t)=U'}} \tag{2.19}$$
$$E' = \left[\frac{\partial g}{\partial u'}\right]_{\substack{x(t)=X \\ u'(t)=U'}}$$

(2.18) is an approximation of the nonlinear system and new variable names should formally have been used. To limit the number of variable names, this is not made.

$$u'(t) = \begin{bmatrix} u(t) \\ d(t) \end{bmatrix} = \begin{bmatrix} U \\ D \end{bmatrix} + \begin{bmatrix} \hat{u}(t) \\ \hat{d}(t) \end{bmatrix} \tag{2.20}$$

$$\begin{aligned} d'(t) &= 1 - d(t) \\ D' &= 1 - D \end{aligned} \tag{2.21}$$

At operating point eq. (2.16) and (2.17) are written using with eq. (2.12)

$$\begin{aligned} 0 &= AX + BU \\ Y &= CX + EU \end{aligned} \tag{2.22}$$

Where

$$\begin{aligned} A &= DA_1 + D'A_2 \\ B &= DB_1 + D'B_2 \\ C &= DC_1 + D'C_2 \\ E &= DE_1 + D'E_2 \end{aligned} \tag{2.23}$$

Solving eq. (2.22) for X and Y

$$\begin{aligned} X &= -A^{-1}BU \\ Y &= (-CA^{-1}B + E)U \end{aligned} \tag{2.24}$$

$$\begin{aligned} A' &= A \\ B' &= \left[\frac{\partial f}{\partial u} \quad \frac{\partial f}{\partial d} \right]_{\substack{x(t)=X \\ u'(t)=U'}} = [B \quad (A_1 - A_2)X + (B_1 - B_2)U] = [B \quad B_d] \\ C' &= C \\ E' &= \left[\frac{\partial f}{\partial u} \quad \frac{\partial f}{\partial d} \right]_{\substack{x(t)=X \\ u'(t)=U'}} = [E \quad (C_1 - C_2)X + (E_1 - E_2)U] = [E \quad E_d] \end{aligned} \tag{2.25}$$

Eq. (18) becomes

$$\begin{aligned} \frac{d\hat{x}(t)}{dt} &= A\hat{x}(t) + B'\hat{u}'(t) \\ \hat{y}(t) &= C\hat{x}(t) + E'\hat{u}'(t) \end{aligned} \tag{2.26}$$

Applying Laplace Transform to above equation

$$\begin{aligned} s\hat{x}(s) &= A\hat{x}(s) + B'\hat{u}'(s) \\ \hat{y}(s) &= C\hat{x}'(s) + E'\hat{u}'(s) \end{aligned} \tag{2.27}$$

$$\hat{x}(s) = (sI - A)^{-1} B'\hat{u}'(s)$$
$$\hat{y}(s) = C\hat{x}'(s) + E'\hat{u}'(s) \quad (2.28)$$

2.2.4 Extracting the Transfer functions

We can extract six transfer function from the above equation, but we require only contrl to output transfer function

Control to output transfer function

$$G_{vd} = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{RV_{in}}{RLCs^2 + Ls + R} \quad (2.29)$$

2.3 Stability Analysis

Poles of the above transfer function

$$\text{Poles } P_1, P_2 = \frac{-L \pm \sqrt{L^2 - 4R^2LC}}{2RLC} \quad (2.30)$$

According to fig 2.5 equivalent of R as follows

$$R = R_{Load} \,||\, R_{CPL} \quad (2.31)$$

If $R_{Load} = \infty$

$$R = R_{CPL} \quad (2.32)$$

So R is negative value, Poles are in right half plane, so system will become unstable.

2.3.1 Compensation by R_L

By Considering R_L in series with inductor, the system may become stable.

Poles of the system with R_L

$$P_1, P_2 = \frac{-(L + R_L CR) \pm \sqrt{(L + R_L CR)^2 - 4LC(R + R_L)}}{2RLC} \quad (2.33)$$

If $R<0$ and $|R|<R_L$, then the system should have two real poles, and one of them should be in the right-hand side of the s-plane (right half-plane, RHP); therefore, the system should be unstable

If $|R|>R_L$ and $(((L/R) + R_LC)^2 - 4LC(1+(R_L/R))) < 0$, then poles are complex conjugate, and the real value of the poles depends on the value of $((L/R)+R_LC)$. If $(((L/R) + R_LC)^2 - 4LC(1+(R_L/R))) > 0$, since

L, C, R_L >0 and $|R|>R_L$, we would have $|(L/R)+R_LC|>\left(((L/R)+R_LC)^2-4LC(1+(R_L/R))\right)^{1/2}$. The stability of the system will depend on the value of $((L/R)+R_LC)$.In practical cases $|R|>R_L$, so we will concentrate when $|R|>R_L$ .From (2.33),for making system stable $((L/R)+R_LC)$ should be positive. The value calculated from (2.31) is negative then the stability criterion implies

$$\frac{L}{|R|}<R_LC \tag{2.34}$$

If equation (2.34) does not hold, either R_L or C should be increased or L should be decreased to make this inequality valid.

If R_L is increased, it has to keep below |R| .Considering (2.31), we can stabilize the system by adding the resistance to the output of the converter but it will result more dissipation.

Let us find the amount of power dissipation that is produced by the following two cases:

1) When the compensation is done by increasing the resistive load and 2) when R_L is increased.

In the first case, a resistive load that produces a dissipation equal to P_{CPL} is required, i.e.

$$R_{Load}(Max)=\frac{V^2}{P_{CPL}} \tag{2.35}$$

This resistive load cancels the equivalent negative resistance of the CPL given by (4). The amount of power dissipation is very large so it is not acceptable. Calculate the minimum required R_L such that the total compensation can be done by R_L i.e. $R_{Load} = \infty$. With respect to (2.34), the minimum required R_L is

$$R_L=\frac{L}{C}\frac{1}{|R|} \tag{2.36}$$

$$R_{Load}=\infty \Rightarrow R=R_{CPL}=-\frac{V^2}{P_{CPL}} \tag{2.37}$$

Therefore

$$R_L=\frac{L}{C}.\frac{P_{CPL}}{V^2_{out}} \tag{2.38}$$

The above value should not greater than the |R| for a stable system. With an output power equal to P_{CPL} and with output voltage V_o, the average output current, which is equal to the average inductor current, will be

$$I_L = \frac{P_{CPL}}{V} \tag{2.39}$$

Therefore

$$P_{R_L} = R_L I^2_L = \frac{L}{C}\frac{P^3_{CPL}}{V^4} \tag{2.40}$$

From (2.40) we can conclude that if the output voltage is less, the power dissipation across R_L is high. In addition, as mentioned earlier, for a negative output equivalent load resistance, the necessary condition for stability is that $R|<R_L$. Therefore, substituting $R_L = |R| = |\infty||R_{CPL}| = \left(V_{out}{}^2 / P_{CPL}\right)$ and (2.39) into (2.40),

We have

$$P_{R_L}(\text{Max}) = \frac{V^2}{P_{CPL}}\left(\frac{P_{CPL}}{V}\right)^2 = P_{CPL} \tag{2.41}$$

From (2.41) we can say compensating the CPL by increasing R_L is more efficient than by increasing R_{Load}. Equation (2.41) also states that the maximum compensation that can be done with R_L will produce an amount of dissipation equal to the power of the CPL. In other words, if the amount of R_L calculated from (38) produces a power dissipation more than P_{CPL}, the compensation of the CPL cannot be done only by increasing R_L.

If the ON resistance of the switch and the diode are taken into account in, the characteristic polynomial (CP) of the buck converter is calculated as follows:

$$CP = LCs^2 + \left(\frac{L}{R} + (R_s D + R_L + R_D(1-D))C\right)s + \left(\frac{R_s D + R_L + R_D(1-D)}{R} + 1\right) \tag{2.42}$$

Equation (2.42) shows that $R_s.D$ and $R_D.(1-D)$ act similar to R_L and, therefore, it's contribute damping to the LC system

2.3.2 Compensation by Snubber Circuits

There are different circuit configurations that provides the necessary damping only near the frequencies where the LC tank can exhibit undesired oscillations. Therefore, the use of them in the circuits can reduce the power dissipation. These circuits were initially used for the damping of

the input filters of the converters. However the instability problem associated with the input filter of a closed loop converter is analogous to the instability caused by the CPL loaded to a converter..

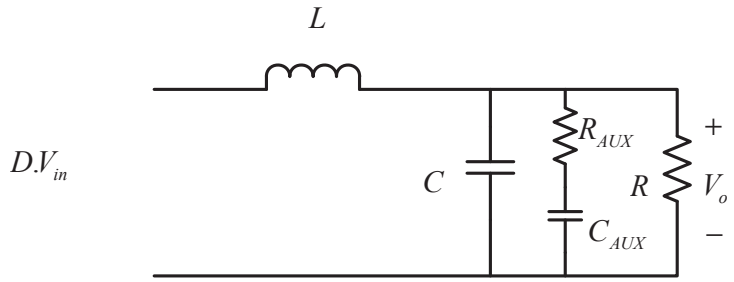

Fig 2.10: Buck Converter with RC Snubber.

As shown in the Fig 2.10, an RC network has been added for providing the damping to the output of the converter. The capacitor blocks the DC current, and hence at DC level, no dissipation is produced. However, the values of R_{Aux} and $C_{Aux}$is selected in such a way that the capacitor acts as a short circuit while the resistance remain operating at the frequencies where the LC filter can exhibit oscillations (because of the negative resistance R).

Snubbers are small auxiliary networks the power electronics switching circuits employed for controlling the effects of circuit reactance. It aids the enhancement of circuit performance of the switching circuits and provides higher reliability, better efficiency, higher switching frequency, lesser EMI, and reduced size and weight. The basic function of a snubber in the reactive circuit is the energy absorption. This it provides necessary circuit damping, controls the rate of change of current or voltage (or it clamps the voltage overshoot).

Snubbers can be designed from either passive or active elements. Passive snubbers consist of the resistors, capacitors, inductors and diodes. Active snubbers consist of the transistors or other active switching devices, which exploits its parasitic components to serve as the function of the passive components to act as a snubber circuit. However, it often requires a significant amount of extra circuitry. The simple RC snubber dampens the parasitic resonances in the power stage and it is mostly used among all snubber circuits. It is used for the voltage rise control for the output inductances as well as across the switches and diodes.

The capacitor and resistor values can be determined from the other circuit components. The snubber capacitance is usually two to four times the circuit capacitance value. The value of the snubber resistor can be calculated from the impedance of the parasitic resonant circuit.

Tightly regulated load converter can draw constant power from source converter shows negative resistance (-R) to source converter but load converter is having dynamics (Input Impedance). Therefore, in next chapter, we will know how to calculate input impedance closed loop converter and it will affect source converter.

CHAPTER 3
INPUT AND OUTPUT IMPEDANCE OF CLOSED LOOP CONVERTER AND STABILITY ANALYSIS OF CASCADED CONVERTERS

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3.1Input Impedance of Open Loop Buck Converter

The input impedance of a DC-DC converter is defined as the ratio of perturbations in the input voltage ($\hat{v}_i$) to the perturbations in the current ($\hat{i}_i$) when perturbation of the load current ($\hat{i}_{load}$) is zero. As above, since the converter is operating in open loop mode, ($\hat{d}$) should be set to zero as well:

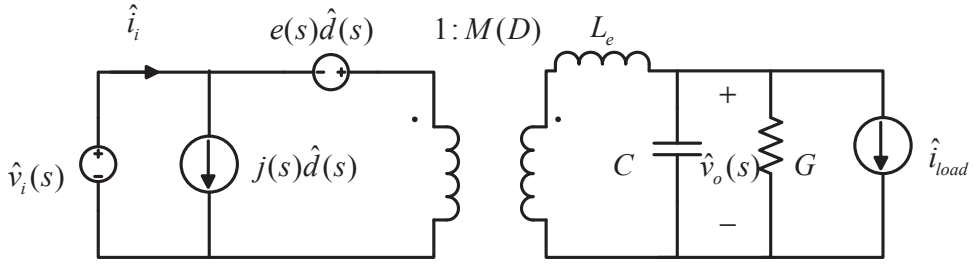


Fig 3.1: Small signal converter model.

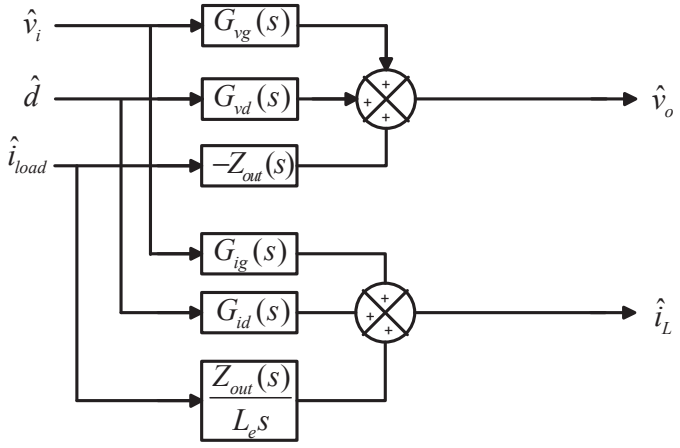


Fig 3.2: Mathematical representation of small signal converter model.

By state space average method we can get

$$G_{vg}(s)=\left.\frac{\hat{v}_o(s)}{\hat{v}_i(s)}\right|_{\hat{d}(s),\hat{g}(s)=0}=\frac{M(D)}{L_eCs^2+L_eGs+1} \tag{3.1}$$

$$G_{vd}(s)=\left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{v}_i(s),\hat{g}(s)=0}=\frac{M(D)e(s)}{L_eCs^2+L_eGs+1} \tag{3.2}$$

$$G_{ig}(s)=\left.\frac{\hat{i}_L(s)}{\hat{v}_i(s)}\right|_{\hat{d}(s),\hat{g}(s)=0}=\frac{M(D)G(1+\frac{C}{G}s)}{L_eCs^2+L_eGs+1} \tag{3.3}$$

$$G_{id}(s)=\left.\frac{\hat{i}_L(s)}{\hat{d}(s)}\right|_{\hat{v}_i(s),\hat{g}(s)=0}=\frac{M(D)e(s)G(1+\frac{C}{G}s)}{L_eCs^2+L_eGs+1} \tag{3.4}$$

$$Z_{out}(s)=\left.\frac{\hat{v}_o(s)}{-\hat{i}_{load}(s)}\right|_{\hat{d}(s),\hat{v}_i(s)=0}=\frac{L_es}{L_eCs^2+L_eGs+1} \tag{3.5}$$

From the definition of input impedance of open loop converter

$$Z_{in}(s)=\left.\frac{\hat{v}_i(s)}{\hat{i}_i(s)}\right|_{\hat{d}(s),\hat{i}_{load}(s)=0} \tag{3.6}$$

With $(\hat{i}_{load})$ and $(\hat{d})$ set to zero the circuit of Fig 3.1. The following relationship can then be derived using circuit analysis:

$$\hat{i}_L(s)=\hat{v}_i(s).\frac{M(D)G(1+\frac{C}{G}s)}{L_eCs^2+L_eGs+1}=\hat{v}_i(s).G_{ig}(s) \tag{3.7}$$

With $\hat{d}$ set to zero, analysis of Fig 3.1 indicates that the relationship between $\hat{i}$ and $\hat{i}_L$ can be expressed as

$$\hat{i}_i(s)=M(D).\hat{i}_L(s) \tag{3.8}$$

Eliminating $\hat{i}_L(s)$ from above equations we will get following equation

$$\frac{\hat{i}_i(s)}{M(D)}=\hat{v}_i(s).G_{ig}(s) \tag{3.9}$$

Therefore, the open loop input impedance can be written as

$$Z_{in}(s)=\left.\frac{\hat{v}_i(s)}{\hat{i}_i(s)}\right|_{\hat{d}(s),\hat{i}_{load}(s)=0}=\frac{1}{M(D).G_{ig}(s)} \tag{3.10}$$

3.2 Input Impedance of Closed Loop Buck Converter

Converter	$M(D)$	L_e	$e(s)$	$j(s)$
Buck	D	L	$\frac{V_{out}}{D^2}$	$\frac{V_{out}}{R}$
Boost	$\frac{1}{D'}$	$\frac{L}{D'^2}$	$V_{out}\left(1-\frac{sL}{D'^2R}\right)$	$\frac{V_{out}}{D'^2R}$
Buck - Boost	$\frac{-D}{D'}$	$\frac{L}{D'^2}$	$\frac{-V_{out}}{D'^2}\left(1-\frac{sDL}{D'^2R}\right)$	$\frac{-V_{out}}{D'^2R}$

Table 3.1: Canonical Model Parameters for Buck, Boost and Buck- Boost Converters.

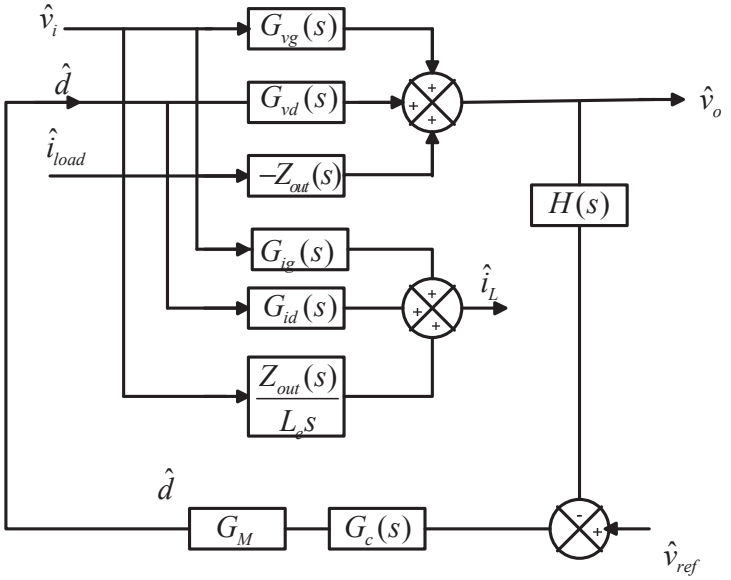


Fig 3.3: Mathematical representation of the closed loop converter in voltage mode control.

Closed loop input impedance is defined as the ratio of perturbations in the input voltage ($\hat{v}_i$) to the perturbations in the input current ($\hat{i}_L$) when perturbation of the load current ($\hat{i}_{load}$) is zero:

$$Z_{in,CL}(s)=\left.\frac{\hat{v}_i(s)}{\hat{i}_i(s)}\right|_{\hat{i}_{load}(s)=0} \tag{3.11}$$

If $\hat{i}_{load}$ and $\hat{v}_{ref}$ are both equal to zero, the following equations can be obtained by analysis of Fig 3.3

$$\hat{d} = -\hat{v}_o H(s) G_c(s) G_M(s)$$
$$\hat{v}_o = G_{vd}\hat{d} + G_{vg}\hat{v}_i \tag{3.12}$$

The relationship between input current perturbation and inductor current perturbation can be obtained from fig 3.1 when $\hat{v}_i, \hat{d} = 0$.

$$\hat{i}_i(s) = j(s)\hat{d} + M(D)\hat{i}_L \tag{3.13}$$

Finally, for the following equation can be obtained from Fig 3.3:

$$\hat{i}_L = G_{id}\hat{d} + G_{ig}\hat{v}_i \tag{3.14}$$

If it is eliminated from (3.13) and (3.14), and combined with equations of (3.12), the following system of linear equations is obtained:

$$\hat{d} + \hat{v}_o H(s) G_c(s) G_M(s) = 0$$
$$G_{vd}\hat{d} - \hat{v}_o + G_{vg}\hat{v}_i = 0 \tag{3.15}$$
$$\hat{i}_i(s) = (j(s) + M(D)G_{id})\hat{d} + M(D)G_{ig}\hat{v}_i$$

From above two eq., replace $\hat{v}_o$ in first eq.

$$\hat{d} + \left(G_{vd}\hat{d} + G_{vg}\hat{v}_i\right) H G_c G_M = 0 \tag{3.16}$$

$$\left(1 + G_{vd}\hat{d} + G_{vg}\hat{v}\right)\hat{d} + H G_c G_M G_{vg}\hat{v}_i = 0 \tag{3.17}$$

$$\hat{d} = -\frac{H G_c G_M G_{vg}\hat{v}_i}{1+T} \tag{3.18}$$

$$-\left(j + MG_{id}\right)\left(\frac{H G_c G_M G_{vg}\hat{v}_i}{1+T}\right) + MG_{ig}\hat{v}_i = \hat{i}_i \tag{3.19}$$

$$\frac{\hat{i}_i}{\hat{v}_i} = -\left(\frac{\left(j + MG_{id}\right) H G_c G_M G_{vg} + MG_{ig}\left(1+T\right)}{1+T}\right) \tag{3.20}$$

$$\frac{\hat{i}_i}{\hat{v}_i} = \left(\frac{-jH G_c G_M G_{vg} + MG_{ig} + MH G_c G_M\left(G_{vg}G_{id} - G_{ig}G_{vd}\right)}{1+T}\right) \tag{3.21}$$

W.K.T $G_{vg}G_{id} - G_{ig}G_{vd} = 0$ (3.22)

$$Y_{inc} = \frac{-jHG_cG_MG_{vg} + MG_{ig}}{1+T} \tag{3.23}$$

$$Y_{inc} = \frac{MG_{ig}}{1+T}\left(1 - \frac{jHG_cG_MG_{vg}}{MG_{ig}}\right) \tag{3.24}$$

$$Z_{inc} = \frac{(1+T)}{MG_{ig}}\left(\frac{1}{1 - \frac{jHG_cG_MG_{vg}}{MG_{ig}}}\right) \tag{3.25}$$

$$Z_{in} = \frac{1}{MG_{ig}} \tag{3.26}$$

$$Z_{inc} = Z_{in}\left(\frac{1+T}{1 - j\frac{TG_{vg}}{G_{vd}}Z_{in}}\right) \tag{3.27}$$

$$\frac{G_{vg}}{G_{vd}} = \frac{1}{e} \tag{3.28}$$

From Table 1 for Buck Converter

$$\frac{j(s)}{e(s)} = \frac{D^2}{R} \tag{3.29}$$

Substituting all the values in the above equation

$$Z_{in,CL}(s) = \left.\frac{\hat{v}_i(s)}{\hat{i}_i(s)}\right|_{\hat{i}_{load}(s)=0} = Z_{in}(s)\left(\frac{1+T}{1 - T\frac{D^2}{R}Z_{in}(s)}\right) \tag{3.30}$$

3.3 Output Impedance of Open Loop Buck Converter

The output impedance of a DC-DC converter is defined as the ratio of the perturbations of the output voltage ($\hat{v}_o$) to the negative perturbations of the load current ($\hat{i}_{load}$) when perturbation of the input voltage ($\hat{v}_i$) is zero. Since the goal is to calculate the open loop output impedance, ($\hat{d}$) is set to zero as well:

$$Z_{out}(s)=\left.\frac{\hat{v}_o(s)}{-\hat{i}_{load}(s)}\right|_{\hat{d}(s),\hat{v}_i(s)=0} \tag{3.31}$$

Setting $\hat{v}_i$ and $\hat{d}$ equal to zero in fig 3.1

A relationship for $(\hat{v}_o)$ is extracted by using circuit analysis:

$$\hat{v}_o=-\hat{i}_{load}(s)\times\frac{L_e s}{L_e C s^2+L_e G s+1} \tag{3.32}$$

Referring to the definition of output impedance, the open loop output impedance is calculated as:

$$Z_{out}(s)=\left.\frac{\hat{v}_o(s)}{-\hat{i}_{load}(s)}\right|_{\hat{d}(s),\hat{v}_i(s)=0}=\frac{L_e s}{L_e C s^2+L_e G s+1} \tag{3.33}$$

3.4 Output Impedance of Closed Loop Buck Converter

Closed-loop output impedance is defined as the ratio of perturbations in the output voltage $(\hat{v}_o)$ to the negative perturbations of the load current load $(-\hat{i}_{load})$ when the perturbation of the input voltage $(\hat{v}_i)$ equal to zero, the following equations can be obtained from fig 3.3:

$$\begin{aligned}\hat{d}&=\left(\hat{v}_{ref}-\hat{v}_o H(s)\right)G_c(s)G_M(s)\\ \hat{v}_o&=G_{vd}(s)\hat{d}+\hat{i}_{load}Z_{out}\end{aligned} \tag{3.34}$$

If $\hat{v}_{ref}$ is equal to zero, the closed-loop output impedance can be found by solving above equation

$$Z_{out,CL}(s)=\left.\frac{\hat{v}_o(s)}{-\hat{i}_{load}(s)}\right|_{\hat{v}_i(s)=0}=\frac{Z_{out}}{1+H(s)G_c(s)G_{vd}(s)G_M(s)} \tag{3.35}$$

$$Z_{out,CL}(s)=\frac{Z_{out}}{1+T} \tag{3.36}$$

Where $T=H(s)G_c(s)G_{vd}(s)G_M(s)$

Parameters of Source and Load converter

$f_{sw}=100KHz, V_{in}=20V, V_o=10V,$
$L=318.3\mu H, C=318.3\mu F, R_L=0.3$
$G_c=\frac{8.4e6(s+4275)^2}{s(s+2.3e5)^2}$

$f_{sw}=100KHz, V_{in}=10V, V_o=5V,$
$L=39.788\mu H, C=159.154\mu F, R=2.5\Omega$
$G_c=\frac{6.78e7(s+1.71e4)^2}{s(s+9.234e5)^2}$

3.5 Results

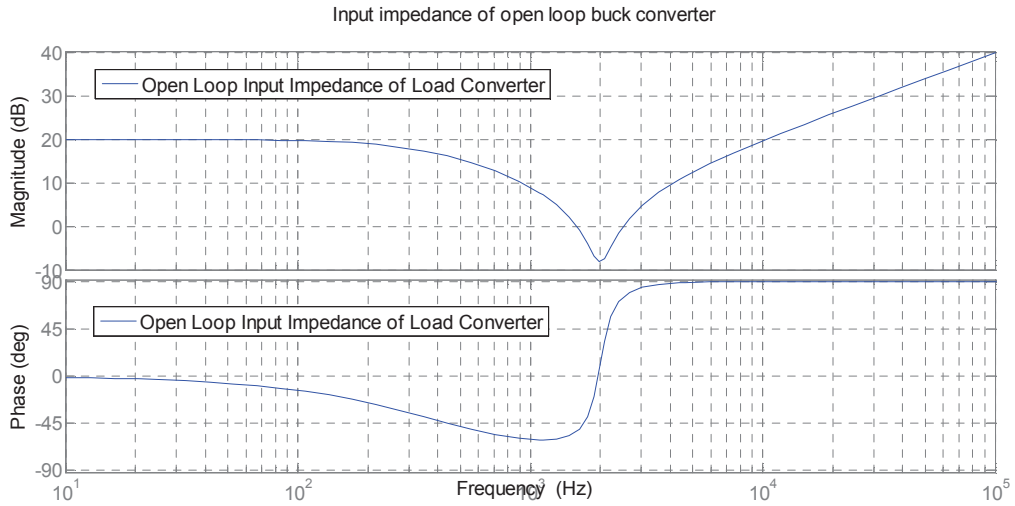


Fig 3.4: Input impedance of open loop buck converter.

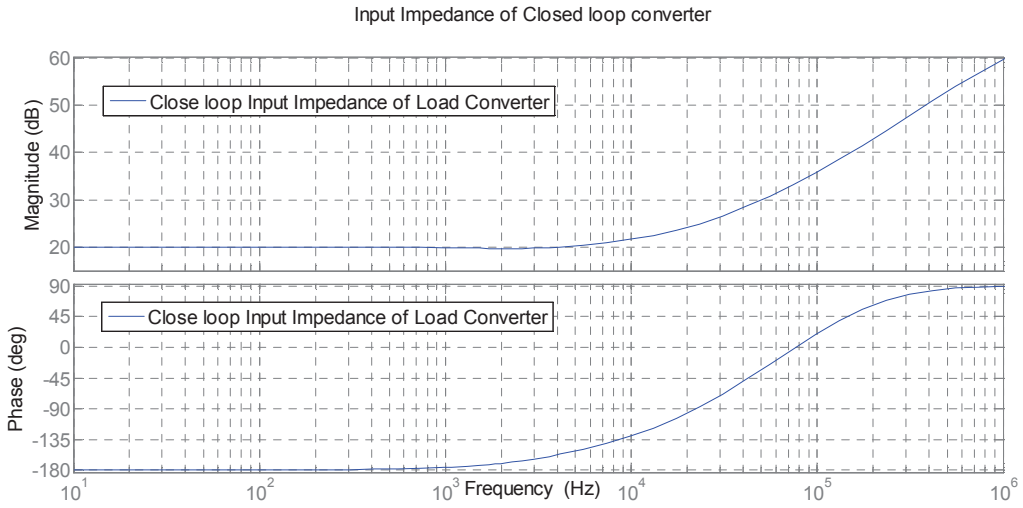


Fig 3.5: Input impedance of closed loop buck converter.

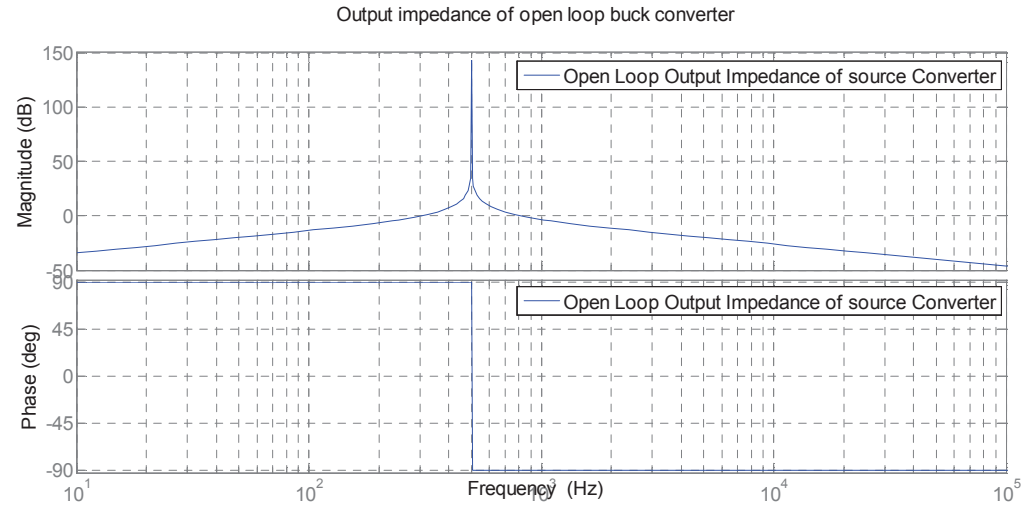


Fig 3.6: Output impedance of open loop buck converter.

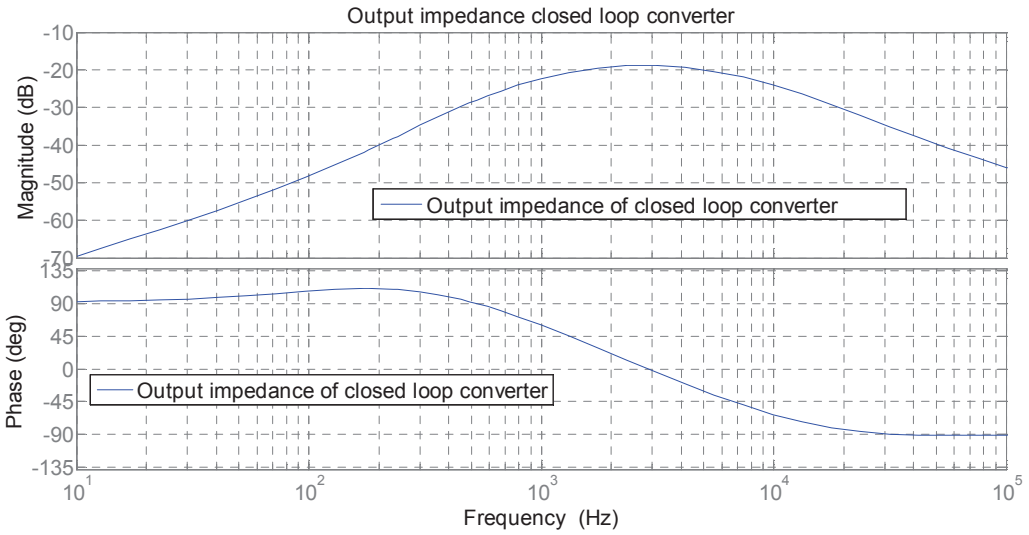


Fig 3.7 Output impedance of closed loop buck converter.

3.6 Stability Analysis

3.6.1Two Stage Distributed System

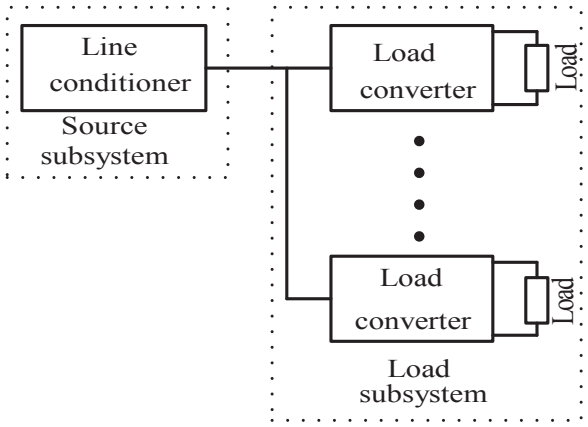


Fig 3.8: Two stage DC distributed system.

A two-stage DPS consisting of a line source converter feeding the load converters has been shown in Fig 3.8. We have two methods of designing the above DSP out of which in first we can design the line conditioner separately by using an ac unterminated modeling approach. After that based on the output impedance characteristics of the line conditioner, we can set out the specifications for the load subsystem's input impedance so as to ensure the stability of the system. One sufficient condition to ensure the stability of the overall system is that the magnitude of the input impedance of the load subsystem should be forced to be always greater the output impedance of the source converter. However it is quite a conservative approach and hence difficult to achieve the load impedance specification requiring an impedance separation at the interface.

3.6.2 System Stability Margin

Impedance criterion provides the practical way for the analysis of the small signal stability of a DSP. As can be seen from the Fig 3.9, if the standalone operation of the both source and load subsystems are respectively stable, then the minor loop gain which is equivalent to the impedance ratio Z_o/Z_i between source and load modules, determines the small signal stability of the whole system,

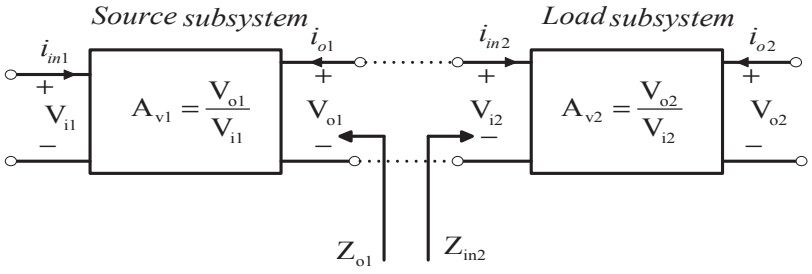


Fig 3.9: Impedance Criterion.

This "minor loop" is the voltage-current feedback loop existing between source and load modules. In the block diagram of Fig 3.10, this "minor loop" has been highlighted with thick arrows. Since

stand alone operation of both of the source and load modules are stable, the overall system stability can be now determined by this inter-module "minor loop".

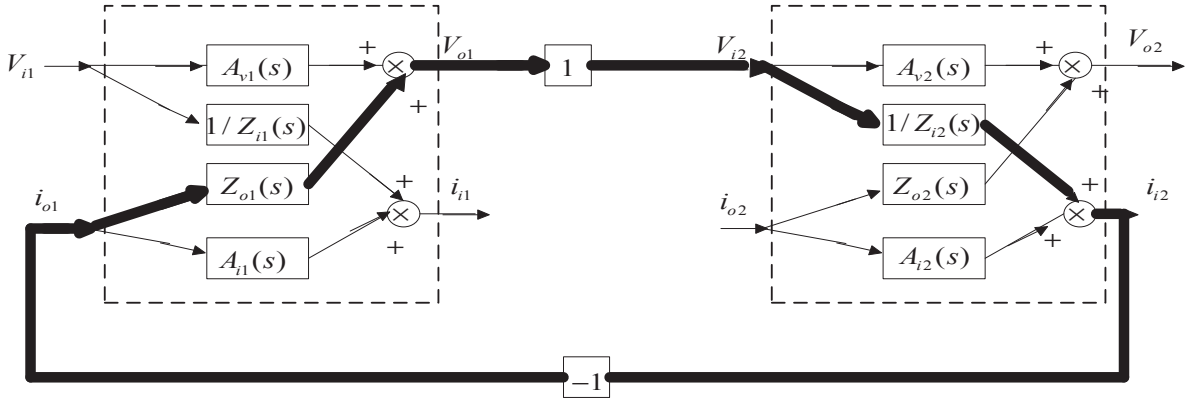


Fig 3.10: Minor loop gain Z_o/Z_i in block diagram.

In Fig 3.10, source and load modules are modelled as two- port networks, with four I/O parameters (transfer functions) A_v, A_i, Z_i, Z_o for each, as described by (3.37).

$$\begin{bmatrix} V_o \\ i_i \end{bmatrix} = \begin{bmatrix} A_v & Z_o \\ Z^{-1}_i & -A_i \end{bmatrix} \begin{bmatrix} V_i \\ i_o \end{bmatrix} \tag{3.37}$$

From above fig we can write obtained following equations

$$\begin{aligned} V_{o1} &= A_{v1}V_{i1} + Z_{o1}i_{o1} \\ i_{i1} &= \frac{A_{i1}}{Z_{i1}} + A_{i1}i_{o1} \end{aligned} \tag{3.38}$$

$$\begin{aligned} V_{o2} &= A_{v2}V_{i2} + Z_{o2}i_{o2} \\ i_{i2} &= \frac{A_{i2}}{Z_{i2}} + A_{i2}i_{o2} \end{aligned} \tag{3.39}$$

From fig 3.9 the following equations can be obtained

$$\begin{aligned} V_{o1} &= V_{i2} \\ i_{i2} &= -i_{o1} \end{aligned} \tag{3.40}$$

Apply super position theorem for calculating overall input to output transfer function in fig 3.10

$$i_{i1} = 0, i_{02} = 0 \tag{3.41}$$

$$\frac{V_{o2}}{V_{i1}} = \frac{A_{v2}V_{i2}}{V_{i1}} \tag{3.42}$$

Substitute 4.5 in 4.9

$$\frac{V_{o2}}{V_{i1}} = \frac{A_{v2}V_{i2}}{\left(\frac{V_{o1}-Z_{o1}i_{o1}}{A_{v1}}\right)} \tag{3.43}$$

$$\frac{V_{o2}}{V_{i1}} = \frac{A_{v2}A_{v1}V_{i2}}{\left(V_{o1}-Z_{o1}i_{o1}\right)} \tag{3.44}$$

$$\frac{V_{o2}}{V_{i1}} = \frac{A_{v2}A_{v1}V_{i2}}{\left(V_{o1}+Z_{o1}i_{i2}\right)} \tag{3.45}$$

$$\frac{V_{o2}}{V_{i1}} = \frac{A_{v2}A_{v1}V_{i2}}{V_{o1}\left(1+\frac{Z_{o1}i_{i2}}{V_{o1}}\right)} \tag{3.46}$$

$$\frac{V_{o1}}{i_{i2}} = \frac{V_{i2}}{i_{i2}} = Z_{in2} \tag{3.47}$$

$$\frac{i_{i2}}{V_{i2}} = \frac{1}{Z_{in2}} \tag{3.48}$$

$$\frac{V_{o2}}{V_{i1}} = \frac{A_{v2}A_{v1}}{\left(1+\frac{Z_{o1}}{Z_{in2}}\right)} \tag{3.49}$$

$$\frac{V_{o2}}{V_{i1}} = \frac{A_{v2}A_{v1}}{\left(1+T_m\right)} \tag{3.50}$$

Where $T_m = \frac{Z_{o1}}{Z_{i2}}$

According to Nyquist criterion, the basic requirements on Z_o/Z_i to ensure system stability is that it should not encircle (-1,0) point on the s-plane. In addition, sufficient stability margin is also needed so that both system stability robustness and dynamic performance are ensured. If this minor loop gain does not satisfy the Nyquist stability criterion condition, then the system will be unstable. Therefore, the measurement of minor loop gain becomes a fundamental technique for the analysis of the stability of the system.

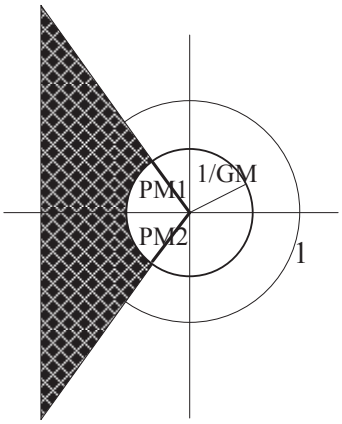


Fig 3.11 Forbidden region for loop gain T_m.

The forbidden region shown in Fig 3.11 corresponds to the shaded area determined by following two inequalities:

$$|Z_o| - |Z_{in}| > -GM \ [dB] \tag{3.51}$$

$$180^\circ - PM_1 < \angle Z_o - \angle Z_{in} < 180^\circ + PM_2 \tag{3.52}$$

CHAPTER 4

COMPENSATOR DESIGN FOR CASCADED CONVERTERS

CHAPTER 4

COMPENSATOR DESIGN FOR CASCADED CONVERTERS

4.1 Compensator design for cascaded converters

Analysis of the stability of feedback loops is based on the trial-and-error method. The results of a particular design can be easily obtained with the help of the computer modeling and CAD tools; it remains a difficult problem to design the circuit parameters to obtain the desired results for a particular circuit. This problem can be overcome by the use of the compensators, which are an op amp based amplifier. These amplifiers, together with a new mathematical concept called the K Factor, permits to choose a desired result to the circuit designer, i.e., a particular loop cross-over frequency and phase margin, and then the necessary component values can be determined to achieve the desired results by solving few algebraic equations.

4.2 Different types of compensator

Type I compensator:

Type I amplifier along with its transfer function is as shown in Figure 4.1. It has a single pole at the origin and it has a constant slope of –1 slope forever, and its magnitude plot crosses unity gain at the frequency where the reactance of C1 is equivalent to the magnitude to the resistance of R1.

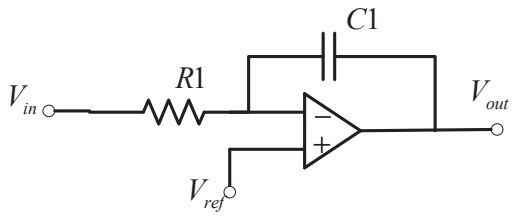


Fig 4.1: Type I compensator.

$$\frac{V_{out}}{V_{in}} = \frac{1}{R_1 C_1 s} \tag{4.1}$$

Type II compensator:

Type II amplifier along with its transfer function is as shown in Figure 4.2. Similar to Type I amplifier, Type II amplifier also has a pole at the origin, but it also has a zero-pole pair in addition. Because of this zero-pole pair there exists a zero gain slope region and therefore a phase "bump" (region of reduced phase shift) exists corresponding to it. However the phase shift of – 270 degrees exists throughout the region with a slope of –1 slope whereas in the region corresponding to zero magnitude, the phase shift rolls off to -180 degrees. The amount of decrement in the value of the

phase shift i.e. size of the "bump" depends on the width of the zero slope regions and it can have a maximum value of 90 degrees.

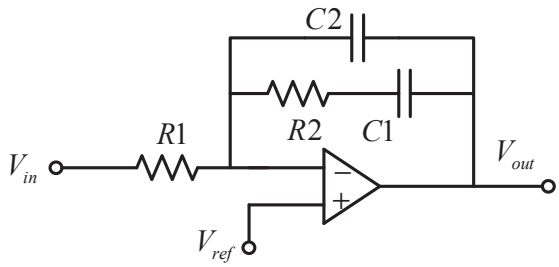


Fig 4.2: Type II compensator.

$$\frac{V_{out}}{V_{in}} = \frac{1}{R_1 C_2} \cdot \frac{\left(s + \frac{1}{R_2 C_1}\right)}{s\left(s + \frac{(C_1 + C_2)}{R_2 C_1 C_2}\right)} \tag{4.2}$$

Type III compensator:

Type III amplifier along with its transfer function is as shown in Figure 4.3. In addition to having a pole at the origin, Type III amplifier also have two zero-pole pairs. The two zeros coincides with each other as well as both the poles also coincides with each other, and hence it results in a region having the magnitude plot with +1 gain slope and the phase plots consists of a corresponding phase "bump", or region of reduced phase shift. However, the phase shifts of – 270 degrees exists throughout the region with a slope of –1 slope whereas in the region corresponding to +1 magnitude, the phase shift rolls off to -90 degrees. The amount of decrement in the value of the phase shift i.e. size of the "bump" depends on the width of the +1 slope region and it can have a maximum value of 180 degrees.

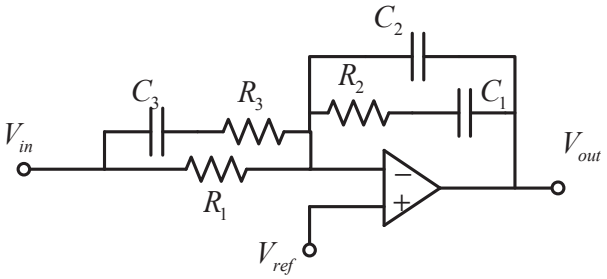


Fig 4.3: Type III compensator.

$$\frac{V_{out}}{V_{in}} = \frac{(R_1 + R_3)}{R_1 R_3 C_2} \cdot \frac{\left(s + \frac{1}{R_2 C_1}\right)\left(s + \frac{1}{(R_1 + R_3) C_3}\right)}{s\left(s + \frac{(C_1 + C_2)}{R_2 C_1 C_2}\right)\left(s + \frac{1}{R_3 C_3}\right)} \tag{4.3}$$

Type III amplifiers provide the maximum phase boost among any practical amplifier configuration. In practical, it is not possible to compensate for the phase lag of more than 180 degrees in the modulator portion. If the modulator's phase shift is greater than 180 degrees at the chosen cross-over frequency, steps should be taken so as to cross the loop (frequency with less phase lag), or otherwise the modulator circuit can be modified so that at the desired cross-over frequency the amount of phase lag gets reduced. The frequency response of Type III compensator network is as shown below.

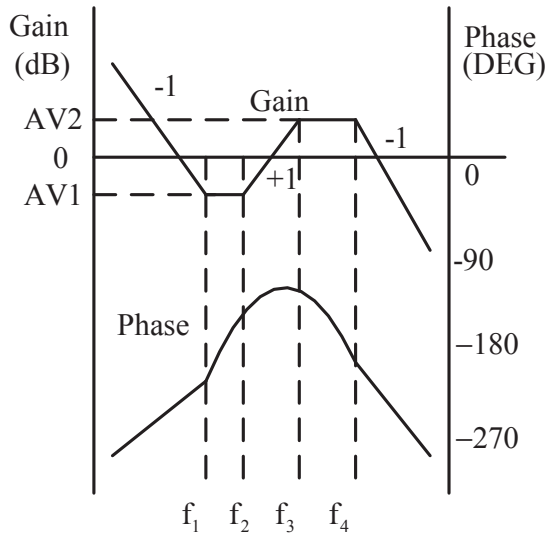


Fig 4.4: Frequency response of Type III compensator network.

4.3 Selection of compensator

Type I amplifier: The Type I amplifiers can be used when no boost is required. This is the case where a loop is crossed over before the frequency of the L-C corner, for example. This is the simplest among all other amplifiers and it requires only fewest parts.

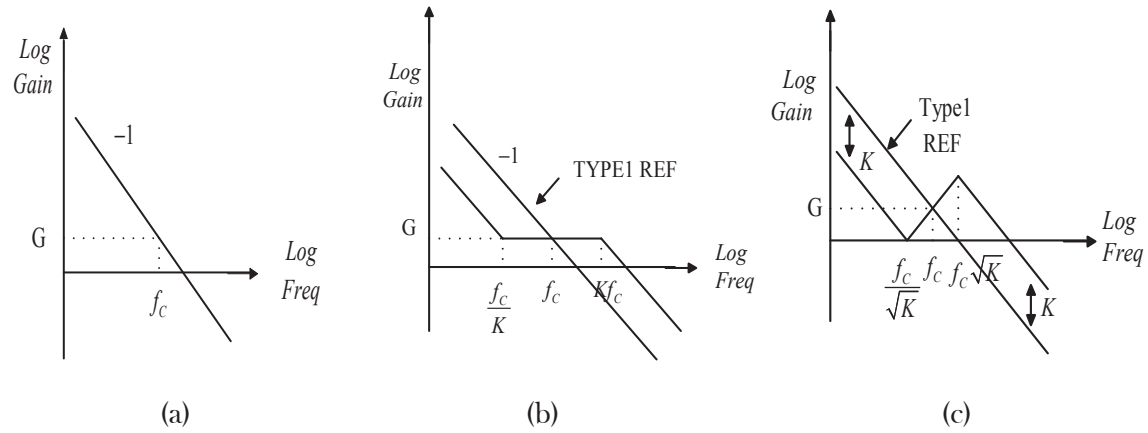
Type II amplifier: The Type II amplifier can be used when the required boost is lesser than 90 degrees, and is most practical conditions it is used where the desired boost is lesser than or about 70 degrees, because as the boost approaches 90 degrees, a very large K factor is required. It is mostly used for loops where the modulator gain curve falls off at a slope of about–1 slope, and the phase shift is about – 90 degrees. This is the case in current regulators, or in voltage regulators above the frequency of the ESR zero of the main filter capacitor.

Type III amplifier: The Type III amplifier can be used when a phase boost of lesser than 180 degrees is required. It provides the maximum boost among all other amplifiers for a given value of K factor but it requires the maximum no of the parts as well. The performance of the loop with a Type III amplifier will always be better than with a Type I or Type II amplifier. Here "better" means providing more low frequency gain and lesser high frequency gain for the given cross-over frequency and phase margin.

4.4 Introduction to the K FACTOR

The K Factor is a mathematical term introduced for facilitating the synthesis of amplifiers. It is defined as "the square root of the ratio of the pole frequency to the zero frequency for Type II amplifiers, or the ratio of the double pole frequency to the double zero frequency for Type III amplifiers" [11].

Figure 5.5 shows the pole-zero location as well as the loop crossover frequencies for all the three types of the amplifier. Since Type I amplifier consists of a single pole and no zero, therefore its K factor is always unity. However, for a Type II amplifier, there is a single pole and a zero and they exists at the position Kf and K/f respectively. Therefore, the geometric mean of the pole frequency and the zero frequency gives the value of f. The maximum phase boost due to the pole zero pair occurs at a frequency f, and therefore it is assumed that the amplifier is designed so that the f and the loop cross over frequency coincide. According to the definition, for a Type III amplifiers the frequency of the two coincident zero is given by the ratio of f and the square root of K where as the frequency of the coincident pole is given by the product of f and the square root of K. Hence, the geometric mean of the coincident zero frequency and the coincident pole frequency gives the value of frequency f. The maximum phase boost from the two coincident zeroes and poles is achieved at the frequency f and hence it is assumed that the amplifier is designed so that the loop cross over frequency coincides with the f.



(a) (b) (c)

Fig 4.5: The Bode plot characteristics of (a) the Type I compensation network, (b) Type II compensation network, and (c) Type III compensation network, in relation to the K factor.

4.4.1 Derivation K for Type III Amplifiers

Type III amplifiers have a double zero at the frequency having a value equal to the ratio of f and square root of K and a double pole at the frequency having a value equal to the product of f and square root of K. The phase boost provided by a single zero-pole pair at these frequencies can be given by the equation:

$$\text{Boost}=\text{Tan}^{-1}\sqrt{K}-\text{Tan}^{-1}(1/\sqrt{K}) \tag{4.4}$$

For a double zero-pole pairs, the two zeros coincides with each other and the two poles also coincides with each other, and hence the phase boost provided by the double zero-pole pair is twice as compared to a single zero-pole pair, therefore the phase boost from a Type III amplifier is the double of Type II and can be given by:

$$\text{Boost}=2\left(\text{Tan}^{-1}\sqrt{K}-\text{Tan}^{-1}(1/\sqrt{K})\right) \tag{4.5}$$

$$\text{W.K.T } \text{Tan}^{-1}x+\text{Tan}^{-1}(1/x)=90 \tag{4.6}$$

Incorporating the trigonometric identity given in (4.6) into (4.5),

$$\text{Boost}=2\left(\text{Tan}^{-1}\sqrt{K}+\text{Tan}^{-1}\sqrt{K}-90\right) \tag{4.7}$$

$$\text{Boost}=2\left(\text{Tan}^{-1}\sqrt{K}+\text{Tan}^{-1}\sqrt{K}-90\right)$$

$$\text{Boost}=2\left(2\text{Tan}^{-1}\sqrt{K}-90\right)$$

$$\text{Boost}=4\left(\text{Tan}^{-1}\sqrt{K}\right)-180 \tag{4.8}$$

Eq. (4.8) can be arranged to solve K

$$\text{Tan}^{-1}\sqrt{K}=\left(\text{Boost}+180\right)/4$$

$$=\left(\text{Boost}/4\right)+45 \tag{4.9}$$

$$\sqrt{K}=\text{Tan}\left(\left(\text{Boost}/4\right)+45\right) \tag{4.10}$$

$$K=\text{Tan}^{2}\left(\left(\text{Boost}/4\right)+45\right) \tag{4.11}$$

Equation (4.11) shows the relationship between the K factor and the required phase boost for a Type III compensators. The position of the double zero and double pole has been established. Certain preliminary steps that should been followed before synthesizing an amplifier using the K factor to stabilize a feedback loop is as follows:

4.5 Selection of cross-over frequency, phase margin and gain of the compensator

4.5.1 Select cross frequency

Select the frequency at which you would like the overall loop gain to be unity. This is f, the cross-over frequency. This is normally chosen to be as high as possible, since higher cross-over frequency normally means faster transient response, and "as high as possible" means where the modulator phase shift is still less than 180 degrees. If the circuit has to be built in volume, where there may be significant differences in component values from unit to unit, or if it will be subjected to wide extremes of line, load, and temperature, it is best not to push the loop to extremes.

4.5.2 Select the Phase margin

Choose the Desired Phase Margin Pick the amount of phase margin you would like to have at unity gain. A phase margin of 90 degrees means your system is stable as a rock. Phase margin of 60 degrees is a good compromise between fast transient response and stability. Phase margins of 30 degrees or less cause the system to have substantial ringing when subjected to transients, and little tolerance for component or environmental variations.

4.5.3 Determine Required Amplifier Gain

The fourth step is to determine the required amplifier gain at cross-over. The amplifier gain at cross-over must equal the modulator loss, therefore the amplifier gain = 1/modulator gain. If the gain is expressed in dB, then the amplifier gain is simply the negative of the modulator gain. Calculate Required Phase Boost Calculate the amount of phase boost required from the zero-pole pair in the amplifier from the formula:

Boost = M – P – 90

Where, M = Desired Phase Margin (degrees) and P = Modulator Phase Shift (degrees)

	Type III
R_1	User Selected
R_2	$\frac{\sqrt{K}}{K-1}GR_1$
R_3	$\frac{R_1}{K-1}$
C_1	$\frac{K-1}{2\pi f_C GR_1}$
C_2	$\frac{1}{2\pi f_C GR_1}$
C_3	$\frac{K-1}{\sqrt{K}}\frac{1}{2\pi f_C R_1}$

Table 4.1: Components for Type III compensator.

4.6 Results

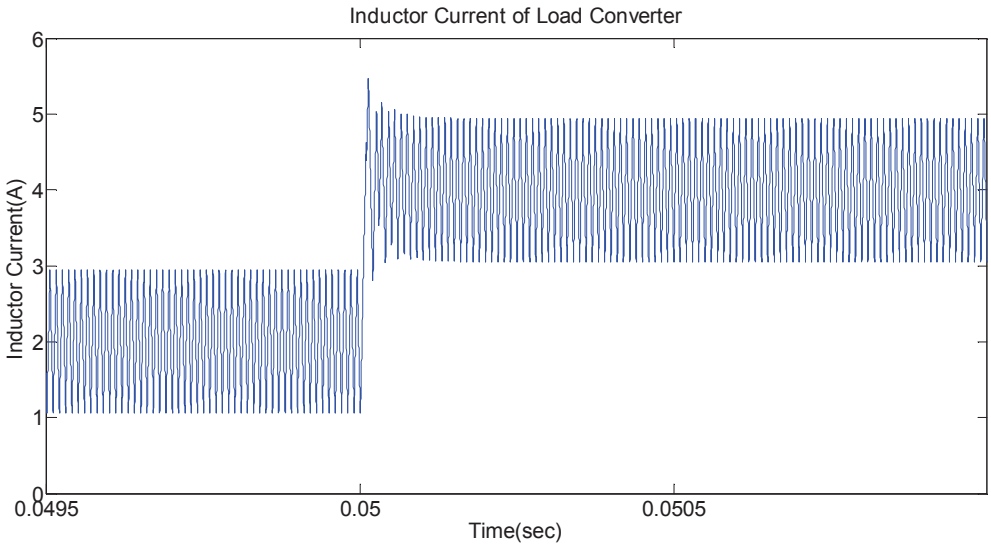


Fig 4.6: Inductor current of load converter.

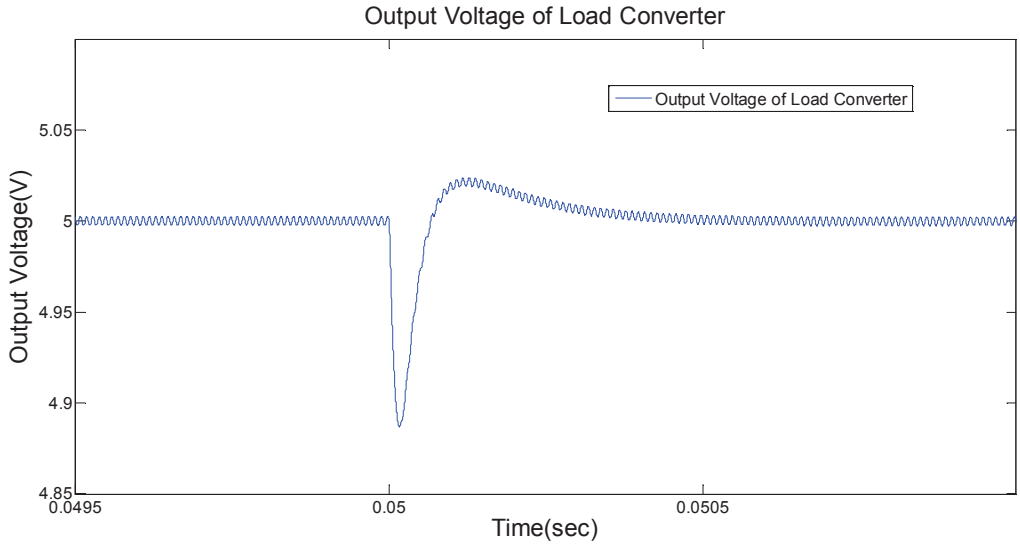


Fig 4.7: Output voltage of load converter.

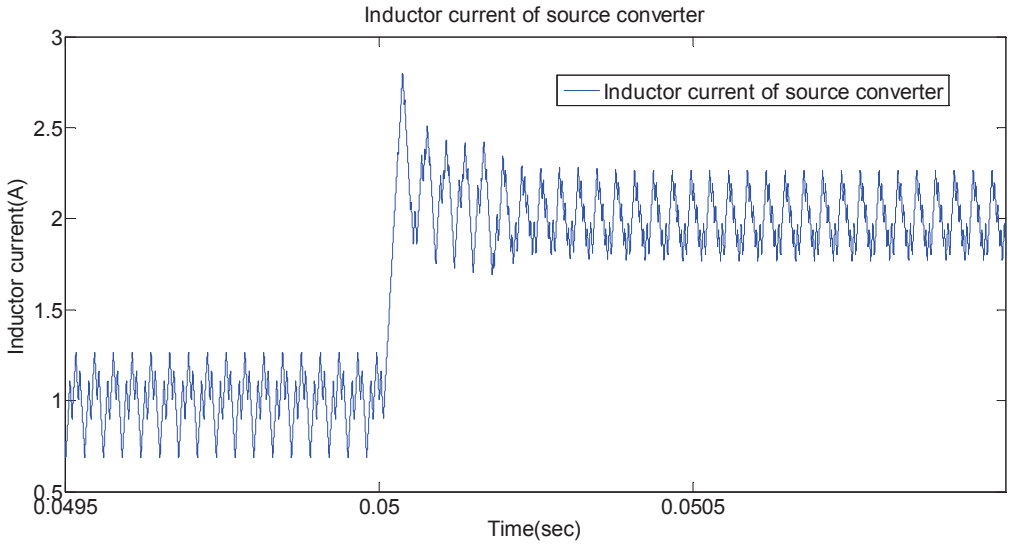


Fig 4.8: Inductor current of source converter.

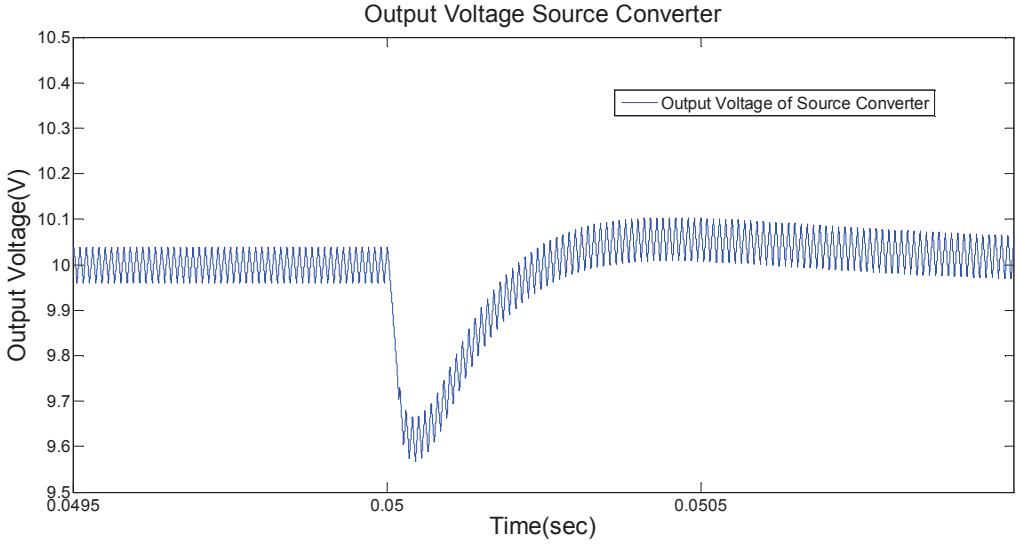


Fig 4.9: Output voltage of source converter.

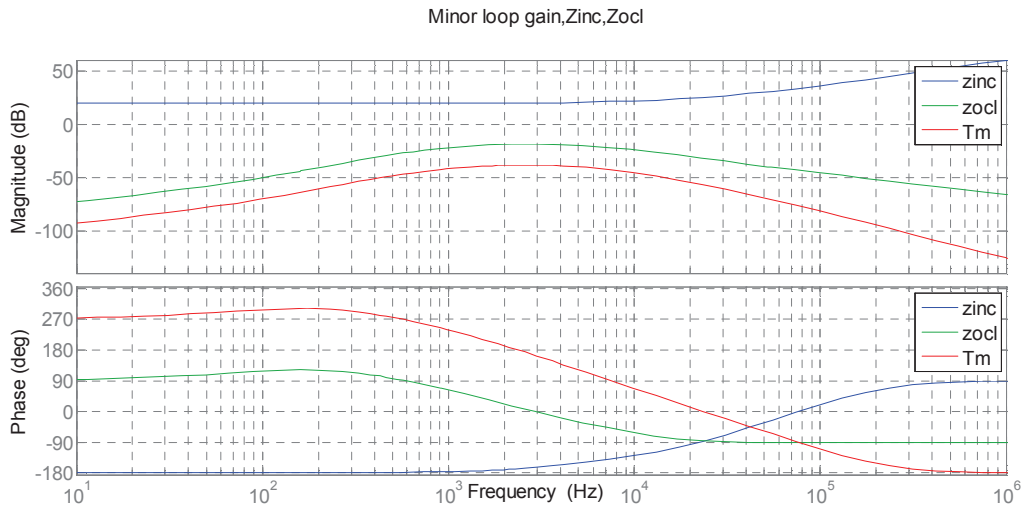


Fig 4.10: Input impedance of load converter, output impedance of source converter and minor loop gain.

CHAPTER 5

CONCLUSION AND FUTURE WORK

CHAPTER *5*

CONCLUSION AND FUTURE WORK

5.1 Conclusion

The basic DC/DC converters that operate in CCM and are loaded by CPLs have been analyzed. The negative equivalent resistance of the CPL can be compensated by the inductor resistance. Two port analysis of DC DC converters have been analyzed. Input impedance of closed loop converter has been studied by two methods and it's affect on the source converter also been studied. Compensator design for CPL has been analyzed by K factor method. Stability analysis has been studied by minor loop gain concept.

5.2: Future work

To stabilize the system using the current mode control on the basis of the input impedance of load converter as a load to the source converter. To design the compensator that satisfying GMPM and ESAC criteria. To extend the analysis done for the buck converter to boost converter stabilizing problem.

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