Investigation on Performance Metrics of Nanoscale Multigate MOSFETs towards RF and IC Applications

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Investigation on Performance Metrics of Nanoscale Multigate MOSFETs towards RF and IC Applications

A dissertation submitted in partial satisfaction of the requirements for the degree of

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by

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"Jay Jagannath Swami Nayana Patha Gami Bhaba Tume"

Dedicated
to
The Dreams and Sacrifices
of my Dear Ones
who Love me a Lot.

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Certificate

This is to certify that the thesis entitled **"Investigation on Performance Metrics of Nanoscale Multigate MOSFETs towards RF and IC Applications"** *by* **Sushanta Kumar Mohapatra** *is a record of an original research work carried out under my supervision in partial fulfillment of the requirements for the award of the degree of Doctor of Philosophy in* ***Electrical Engineering*** *during the session 2014-2015. I believe that this thesis fulfills part of the requirements for the award of degree of Doctor of Philosophy.The results embodied in the thesis have not been submitted for the award of any other degree elsewhere.*

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Declaration of Originality

I, Sushanta Kumar Mohapatra, Roll Number - 511EE306 hereby declare that this dissertation entitled "**Investigation on Performance Metrics of Nanoscale Multigate MOSFETs towards RF and IC Applications**" represents my original work carried out as a doctoral student of National Institute of Technology, Rourkela. To the best of my knowledge, it contains no material previously published or written by another person, nor any material presented for the award of any other degree or diploma of this and any other institution. Any contribution made to this research by others, with whom I have worked at this institution or elsewhere, is explicitly acknowledged in the dissertation. Works of other authors cited in this dissertation have been duly acknowledged under the section "References". I have also submitted my original research records to the scrutiny committee for evaluation of my dissertation.

I am fully aware that in case of any non-compliance detected in future, the Senate of the institute may withdraw the degree awarded to me on the basis of the present dissertation.

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Sushanta Kumar Mohapatra

Acknowledgment

This is the most relevant section of my thesis. A Ph.D. is never completed in isolation. So I owe many thanks to many people.

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Finally, I thank God, who has been kind enough to me to perform this work.

Now that I have found the gold mine, I would keep excavating it and make the most of it. It seems this thesis comes to the end. It is just the preliminary of my exploration.

Sushanta Kumar Mohapatra

Abstract

Silicon-on-Insulator (SOI) MOSFETs have been the primary precursor for the CMOS technology since last few decades offering superior device performance in terms of package density, speed, and reduced second order harmonics. Recent trends of investigation have stimulated the interest in Fully Depleted (FD) SOI MOSFET because of their remarkable scalability efficiency. However, some serious issues like short channel effects (SCEs) viz drain induced barrier lowering ($DIBL$), V_{th} roll-off, subthreshold slope (SS), and hot carrier effects (HCEs) are observed in nanoscale regime. Numerous advanced structures with various engineering concepts have been addressed to reduce the above mentioned SCEs in SOI platform. Among them strain engineering, high-k gate dielectric with metal gate technology (HKMG), and non-classical multigate technologies are most popular models for enhancement in carrier mobility, suppression of gate leakage current, and better immunization to SCEs.

In this thesis, the performance of various emerging device designs are analyzed in nanoscale with 2-D modeling as well as through calibrated TCAD simulation. These attempts are made to reduce certain limitations of nanoscale design and to provide a significant contribution in terms of improved performances of the miniaturized devices. Various MOS parameters like gate work function (ϕ_m), channel length (L), channel thickness (t_{Si}), and gate oxide thickness (t_{ox}) are optimized for both FD-SOI and Multiple gate technology. As the semiconductor industries migrate towards multigate technology for system-on-chip (SoC), system-in-package (SiP), and internet-of-things (IoT) applications, an appropriate examination of the advanced multiple gate MOFETs is required for the analog/RF application keeping reliability issue in mind.

Various non-classical device structures like gate stack engineering and halo doping in the channel are extensively studied for analog/RF applications in double gate (DG) platform. A unique attempt has been made for detailed analysis of the state-of-the-art 3-D FinFET on dependency of process variability. The 3-D architecture is branched as Planar or Trigate or FinFET according to the aspect ratio (W_{Fin}/H_{Fin}). The evaluation of zero temperature coefficient (ZTC) or temperature inflection point (TCP) is one of the key investigation of the thesis for optimal device operation and reliability. The sensitivity of DG-MOSFET and FinFET performances have been addressed towards a wide range of temperature variations, and the ZTC points are identified for both the architectures. From the presented outcomes of this work, some ideas have also been left for the researchers for design of optimum and reliable device architectures to meet the requirements of high performance (HP) and/or low standby power (LSTP) applications.

List of Acronyms

Acronym	Description
2-D	Two Dimenssion
3-D	Three Dimenssion
CLM	Channel Length Modulation
CMOS	Complementary Metal-Oxide Semiconductor
DG MOSFET	Double Gate Metal-Oxide Semiconductor Field Effect Transistor
DH	Double Halo
DI-DG	Dual Insulator Double Gate
$DIBL$	Drain Induced Barrier Lowering
DM	Dual Material
EDA	Electronic Design Automation
EDP	Energy Delay Product
EOT	Equivalent Oxide Thickness
FD-S-SOI	Fully Depleted Strained Silicon on Insulator
FoMs	Figures of Merit
GC-DG	Graded Channel Double Gate
GFP	Gain Frequency Product
GS-DG	Gate Stack Double Gate
$GTFP$	Gain Transconductance Frequency Product
HBT	Heterojunction Bipolar Transistor
HCEs	Hot Carrier Effects
HEMTs	High Electron Mobility Transistors
HKMG	High-k Metal Gate
HP	High Performance
IC	Integrated Chip
IIP_3	Input Intercept Point
IDM	Integrated Device Manufacture
IoT	Internet of Things
ITRS	International Technology Roadmap for Semiconductors
LAC	Lateral Asymmetric Channel
LP	Low Power
LSTP	Low Standby Power
MugFETs	Multiple Gate Mosfets
NNI	National Nanotechnology Initiative
PDP	Power Delay Product
RDF	Random Dopant Fluctuation
RF	Radio Frequency
SCEs	Short Channel Effects
SET	Single Event Transient
SEU	Single Event Upset

continued on the next page

List of Acronyms (*continued*)

Acronym	Description
SH	Single Halo
SiGe	Silicon Germanium
SiP	System on Package
SoC	System on Chip
SOI	Silicon on Insulator
SS	Sub-threshold Slope
TCAD	Technology Computer Added Design
TCP	Temperature Compensation Point
TFP	Transconductance Frequency Product
TFTs	Thin Film Transistors
TGF	Transconductance Generation Factor
TID	Total Ionization Dose
TM	Tri Material
UD-DG	Un-doped Double Gate
UTB	Ultra Thin Body
VI	Volume Inversion
VIP_2	Second order Voltage Intercept Point
VIP_3	Third order Voltage Intercept Point
ZTC	Zero Temperature Coefficient

List of Symbols

Symbol	Description
V_{th} *or* V_T	Threshold Voltage
V_{GS} *or* V_{gs}	Gate to Source Voltage
V_{DS} *or* V_{ds}	Drain to Source Voltage
I_{ds} *or* I_D	Drain Current
t_{ox} *or* T_{ox}	Gate-Oxide Thickness
t_b	Buried Oxide Thickness
L_g *or* L	Channel Length
W	Channel Width
N_A	Acceptor Doping Concentration
N_D	Donor Doping Concentration
t_{Si} *or* T_{Si}	Silicon Body Thickness
L_S/L_D	Source /Drain length
ϵ_{Si}	Permittivity of Silicon
ϵ_{ox}	Permittivity of Oxide
N_{Sub}	Substrate Doping
I_{on}	On-State Drive Current
I_{off}	Off-State Leakage Current
g_m	Transconductance
g_d	Output Conductance
E_v	Early Voltage
A_V	Intrinsic Gain
C_{gs}	Gate to Source Capacitance
C_{gd}	Gate to Drain Capacitance
f_T	Cut-off Frequency
C_T	Total Internal Capacitance
ϕ_m *or* ϕ_M	Metal Work Function
ϕ_{Si}	Silicon Work Function
V_{bi}	Built-in Potential
X	Germanium Mole Fraction
t_{s-Si}	Strained Silicon Thickness
E_C	Electron Affinity
E_G	Energy Band Gap

continued on the next page

List of Symbols *(continued)*

Symbol	Description
η	Body Factor
N_F	Interface oxide trapped charges
SiO_2	Silicon Dioxide
Si_3N_4	Silicon Nitride
HfO_2	Hafnium Oxide
Ta_2O_5	Tantalum Pentoxide
TiO_2	Titanium Dioxide
$T_k\ or\ T_{hk}$	Thickness of High-k Dielectric
φ_S	Surface Potential
v_{Sat}	Saturation Velocity
V_{FB}	Flat Band Voltage
η_i	Intrinsic Carrier Concentration
μ	Mobility
W_{Fin}	Fin Width
H_{Fin}	Fin Height
AR	Aspect Ratio

List of Used Constants with their Values

Constants	Values
Boltzmann Constant (k_B)	$1.38 * 10^{-23} J/K$
Electronic Charge (q)	$1.6 * 10^{-19} Coulomb$
Electron Mass (m)	$9.1 * 10^{-31} Kg$
Intrinsic Carrier Concentration (η_i)	$1.45 * 10^{10} cm^{-3}$
Permeability of Vacuum (μ_0)	$4\pi * 10^{-7} H/m$
Permittivity of Vacuum (ε_0)	$8.85 * 10^{-12} F/m$
Permittivity of Silicon (ε_{Si})	11.68
Permittivity of SiO_2(ε_{SiO_2})	3.9
Permittivity of Si_3N_4($\varepsilon_{Si_3N_4}$)	7.5
Permittivity of HfO_2(ε_{HfO_2})	24
Permittivity of Ta_2O_5($\varepsilon_{Ta_2O_5}$)	30
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Room Temperature (T)	300 K
Thermal Voltage (V_T)	26 mV

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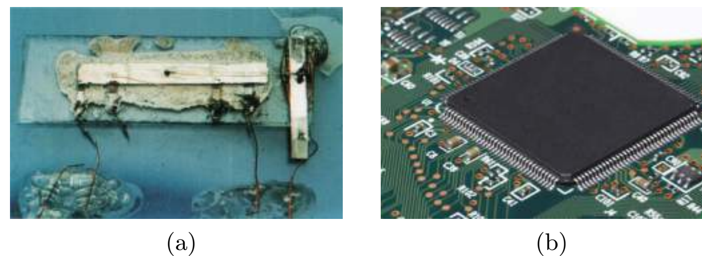
Chapter 1

Prologue

The explosive growth of mobile phone in our pocket, television at home, desktop computer to the space shuttle, cloud computing etc. have changed the life style of the people. It envisions a world of ubiquitous electronic devices and sensors of new exciting applications termed as "Internet of Things (IoT)". The development of the electronics industry is rapid above the substratum *semiconductor device* since mid-20th century. To meet the growing demands of this industry, there evolved the expansion and diversification in the field of research. The fabrication of various functionalities on a single semiconductor surface known as integrated circuits (ICs) or "chips" is so to say the beginning of the electronics era. Everywhere chips perform their operations satisfactorily. Each of these chips are quite diverse, designed to different specifications to perform various operations under several operating conditions. The fundamental technology used in chips is the CMOS (complementary metal-oxide semiconductor) technology.

The workhorse of CMOS technology is the MOSFET (metal-oxide-semiconductor field-effect transistor). These transistors are the most important element for high-density ICs such as microprocessors and semiconductor memories. The concepts of Field Effect semiconductor device was proposed and patented by Julius Edgar Lilienfeld in 1926 and by Oskar Heil in 1934 [1], and practically verified at Bell Laboratory in 1947. William Shockley, John Bardeen and Walter Brattain invented the first point-contact transistor on December 16, 1947 [2]. Robert Noyce [3], co-founder of Fairchild and Jack Kilby [4], electrical engineer of Texas Instruments invented the integrated circuit *aka* the microchip in between 1958 to 1959. That is made up of Electronic components such as transistors and resistors imprinted onto a tiny chip of a semiconducting material, such as silicon or germanium. Fig. 1.1 gives an idea of the developing technology since last 50 years. With the ongoing race of invention the first MOSFET was reported by Kahng and Atalla in 1960 [5].



(a) (b)

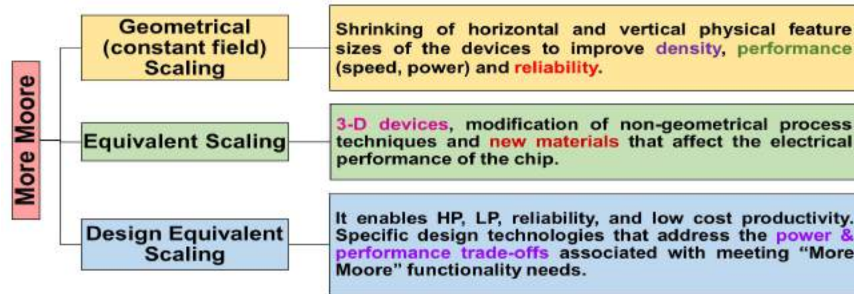
Figure 1.1: (a) 1st Integrated Circuit "*aka*" (b) Morden IC

In 1965, Gordon E. Moore, co-founder of the Intel Corporation observed and predicted that "*The number of transistors incorporated in a chip will approximately double in every 24 months.*" [6]. The reduction in transistor size and packing density continued according to Moore's prediction for which we enjoy the present innovations of electronics.

The art of making small or reduction in scale (Scaling) has been a constant challenge to improve the performance and complexity of the device. With the continuous innovations in the fabrication process, the semiconductor foundries (like Intel, ST Microelectronics, Global Foundries, SMIC, CEA-Leti etc.) entered from bulk

to Micro and proceed to Nanoelectronics.

The breakthroughs in semiconductor processing have allowed "Moore's Law" to hold its position today with modern IC chips containing more than a billion transistors. The International Technology Roadmap for Semiconductors [7] is the 15-year assessment of the semiconductor industry's future technological requirements. These features have created opportunities for the researches in academia or in R&Ds to come up with strategic plan for fulfilling the requirements of future needs. The Executive Summary of the ITRS provides a taxonomy of scaling in the traditional, " *More Moore*" sense. The proposed taxonomy are as follows:



Functional diversification of "*More-than-Moore* (MtM)" approach typically allows for the non-digital functionalities (e.g., Analog and RF communication, power control, passive components, sensors, actuators, etc.) to migrate from the system board-level to a particular package-level (SiP) or chip-level (SoC) for potential solution. The desire to integrate more and more functionality into the IC's results in a never-ending race of shrinking device dimensions. The benefits of miniaturization are higher packaging density, higher switching speed, and low power dissipation.

Innovations in the history of electronics have been possible because of the strong association between devices and materials research. The demand for high performance (HP), low power (LP), and low standby operating power (LSTP) etc. are the significant challenges for the engineering of sub 50nm gate length CMOS devices [8]. To overcome the with various issues, the ITRS offers two approaches leading to non-classical CMOS:

(1) The development of new materials with better carrier transport properties.

(2) The novel transistor structures with improved electrostatics and performance metrics.

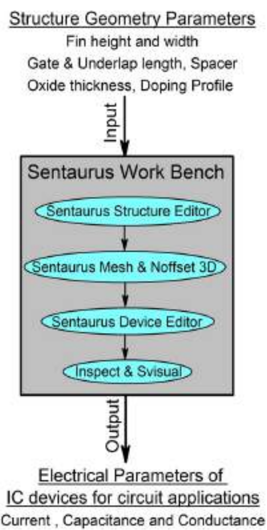


Figure 1.2: Flow chart for TCAD simulation

As semiconductor design becomes more and more complicated with devices getting ever smaller optimization of the device structure has emerged as a hurdle before the designers. Modeling and simulation have been slated to become the computing paradigm of the future. As a paradigm, it is a way of representing problems and thinking about them, as much as a solution method. That can be possible with the help of technology CAD.

Technology CAD (Computer Aided Design, or TCAD) is a branch of electronic

design automation that models semiconductor fabrication and semiconductor device operations. It considers both the physical configuration and related device properties and builds the links between the physics and electrical behavior models that support circuit design. TCAD tools used by the engineers in this group help them to understand and develop process recipes and structures for various devices. TCAD may even help them to predict their electrical, thermal and optical properties under different operating conditions without actual fabrication. The semiconductor companies like Intel-U.S., Samsung-South Korea, Toshiba-Japan, STMicroelectronics-Europe, Qualcomm-U.S., Sony-Japan etc. are using TCAD tools. It helps them to build semiconductor devices and simulate electrical, thermal, and optical characteristics under different bias conditions.

1.1 Motivation of the Work

A close association with technology and integration aspects in view of analog and RF device performance is essential. The corresponding trade-offs are paramount. The introduction of multi-gate devices with high-k/metal gate stack represents "revolutionary" changes in CMOS technology. Therefore, a close insight to analog and RF device behavior for circuit design issues are addressed.

A primary motivation for using TCAD is to study the feasibility of realizing concept devices to minimize these physical effects and improve the device performance by optimizing the device structure with the implementation of equivalent scaling.

1.2 Objective

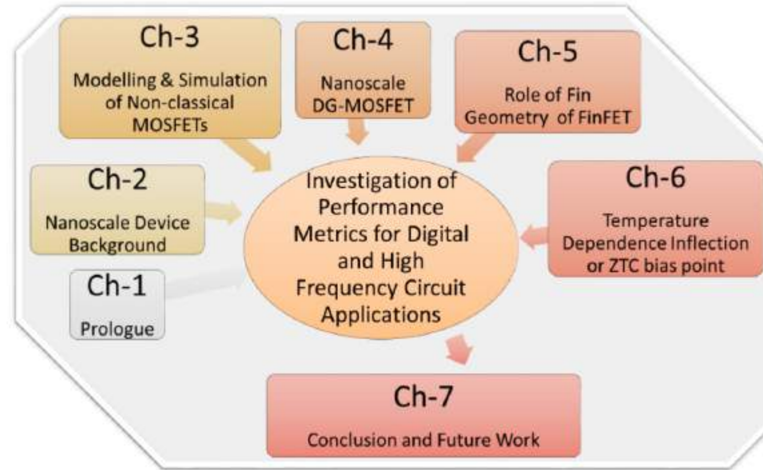
A significant challenge for microelectronic applications is the reduction of energy consumption while increasing performances. As pointed out by several researchers, performance will still improve at least by innovation at the device and system level with holistic design. The main objectives of this research work are:

- To model new devices for minimization of the SCEs with the application of different Engineering.
- To analyze the Static (DC) as well as Dynamic (AC) performances of the device.
- To investigate the important figures of merit (FoMs) of nanoscale MOSFETs for analog and RF circuit applications.

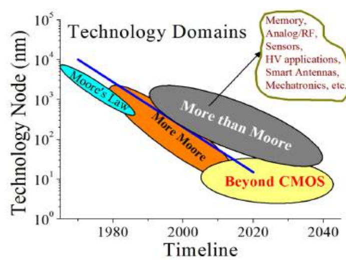
It is harder to control the electrostatic integrity and device variability without degrading circuit performance at the nanoscale regime. So device engineers have started transitioning from the conventional MOSFET towards MugFETs. Our primary objective is focused on a rigorous investigation of various performance measures using TCAD simulation to claim for the solutions of the limitations cited above along with some proposals to design novel devices.

1.3 Organization of the Thesis

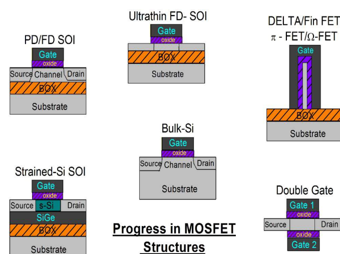
This work proposes a flow of systematic investigation of multigate MOSFETs at the nanoscale. The study of performances at device level with geometrical variation will essentially assist to the circuit designers. The insight of proposed work is an evaluation of static and analog/RF performances with various device designing guidelines. This report positively furnishes benefit for low power and high-performance circuit applications as an analog/RF gadgets.



The thesis is organized into seven chapters beginning with Prologue of thesis. The remaining structures of the thesis is as follows: -

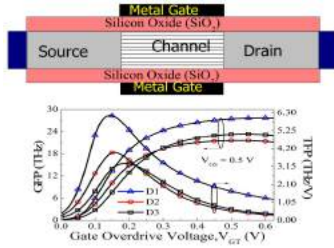


Chapter 2: (Device Background, Issues and Performance Metrics) covers the literature review with the motivation of the thesis work based on the investigation of various performance evaluation on nanoscale MOSFET for circuit application. Mainly the DG-MOSFET which is in turn known as FinFET (3-D structure) is considered in the study. Implementation of various device design engineering are done for the enhancement of performance. The significance of several performances (Static, Analog and RF, Linearity) are explored at the device level.

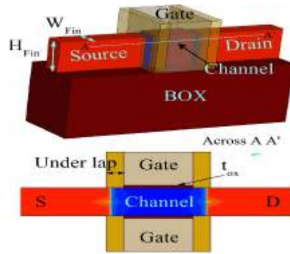


Chapter 3: (Modeling and Simulation of Non-classical MOSFETs) reviews the present scenario of SCEs through 2-D analytical modeling of single and double gate device. The impact of Germanium concentration in strain, silicon body thickness, metal gate work function, oxide thickness, channel doping, +ve and -ve interface trapped charges and gate dielectric permittivity are studied in view of surface potential and threshold voltage calculation. Electrostatic performances are examined in rare structural engineering like dual insulator (DI), graded channel (GC), lateral asymmetric channel (LAC), which termed as single and double halo (SH and DH), tri-material (TM) in gate metal and

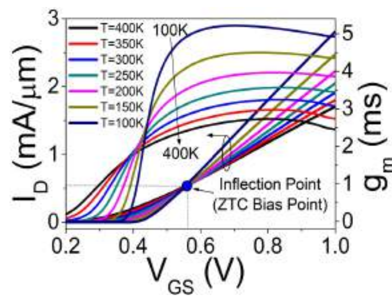
high-k as gate stack (GS) on DG-MOSFET.



Chapter 4: (A Perspective of the Nanoscale DG-MOSFET: Performance Appraisal) introduces Analog/RF figures of merit (FoMs) such as transconductance, early voltage, transconductance generation factor (TGF), intrinsic gain, cutoff frequency, gain bandwidth product for DG-MOSFET. The single oxide layer and the double oxide layer or gate stack (interfacial oxide + high-k layer) are examined for optimization in view of analog/RF performance measure. The impact of channel length, metal gate work function, and miscellaneous device designs are worked out for GS-DG-MOSFET with an extension towards linearity analysis.



Chapter 5: (Role of Fin Aspect Ratio in sub-20 nm SOI-FinFET) investigates a 3-D SOI-FinFET meticulously at sub-20 nm. The impact of Fin height and width on major performance metrics are exercised for the device. Eventually, circuit designers are still looking at PPA (Power, Performance and Area) trade off. The device is categorized through the aspect ratio ($AR = W_{Fin}/H_{Fin}$) as FinFET or Trigate or Planar MOSFET.



Chapter 6: (Temperature Dependence Inflection Point in Ultra-Thin Si directly on Insulator (SDOI) MOSFETs) discusses performances at a wide range of temperatures. For the desire of consumers in a variety of applications and the use the nanoscale transistors, it is important to analyze the dependency performances with respect to temperature. It is essential for digital and analog/RF circuit designers to bias the transistor correctly which show little or no variation with respect to temperature. So the inflection point which is typically known as temperature compensation point (TCP) or zero temperature coefficient (ZTC) is investigated for first time for nanoscale MOSFETs in view of static and analog/RF performance.

Chapter 7: (Conclusion and Future Work) summarizes the presented work in the thesis, and suggestions for areas that need more investigation. Prospectives are provided related to this work and more generally.

Chapter 2

Device Background, Issues and Performance Metrics

This chapter presents the reason behind the search of the non-classical MOSFETs and it's investigation towards device level performance measure. The role of Electronics in the Era of Nanotechnology is with the development of new technology nodes for various applications. The growth of different flavors of SOI and the MugFETs give the solution for the issues generated at the nanoscale device level.
The significance of the major performances of the semiconductor devices, which provide great importance to the circuit designers are enumerated. This chapter deals with several device design proposals that will put forward for improvement in performances through the virtual fabrication platform that is employed in the rest of the work.

2.1 Nanoelectronics in Nanotechnology

Nanotechnology refers to a revolution in science and technology, which covers the designed model with at least one characteristic dimension measured in nanometers (in the range of about $10^{-9}\,m$ to $10^{-7}\,m$ (1 to 100 nm)). According to *National Nanotechnology Initiative* (NNI), Nanotechnology is the ability to understand, control and manipulate matter at the level of $< 100\,nm$, in order to create materials, devices and systems with fundamentally new properties, functions and performance because of their small structure. The NNI is a United States federal government program for the science, engineering and technology research and development for nanoscale projects [9].

The transcript of *Dr. Richard P. Feynman* (Father of Nanotechnology) talk to the annual meeting of the American Physical Society at Caltech on December 29, 1959 is that "**There's Plenty of Room at the Bottom**": *An Invitation to Enter a New Field of Physics* [10]. Dr. Feynman started with a question "*Why cannot we write the entire 24 volumes of the Encyclopedia Britannica on the head of a pin?*". He could foresee the ultimate consequences of writing small and reading fast: which led to the creation of Internet. Internet browsing is not only the micro presentation of information but also the ability to browse through this information at very high speed. "Tyranny of large systems" which arises from the fact of scaling [9], where he speculated on the possibility and potentiality of nano-sized materials. His envision to etch lines that were a few atoms wide with beams of electrons, effectively predicting the existence of electron-beam lithography, which is used today to make silicon chips [11].

Nanoelectronics is a Nanotechnology applied in the context of electronic devices, circuits, and systems. There are several perspectives on the concept of Nanoelectronics as per the technology domains described in Fig. 2.1.

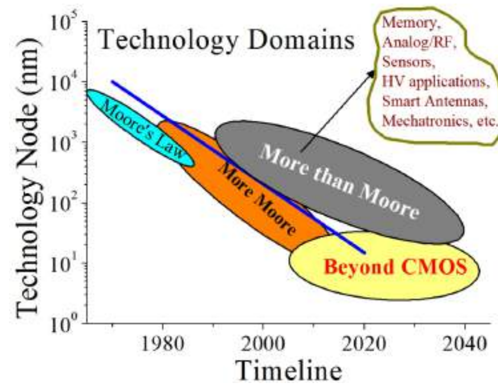


Figure 2.1: Technology Domain

- First is the nanoscale dimensions of Nanoelectronics components. This scaling feature can be described as the "**More Moore**" domain of development.
- Secondly Nanotechnology is diverse allowing the integration of purely electronic devices with mechanical devices, bio-devices, chemical devices, etc. Also, digital

systems can be combined with analog/RF circuits. This technology fusion can be described as the " **More than Moore**" domain of development [12, 13].

- Thirdly the traditional scaling has reached the limits of standard CMOS technology, so calling for fundamentally new nanoscale electronic devices. This development of Nanoelectronic components can be denoted the "**Beyond CMOS**" domain of development.

Among the great variety of transistor types, the two most important types are the *bipolar junction transistor, BJT*, and *field effect transistors, FET*. The most widely used transistor type today is the MOSFETs. As the transistors are the most important element of ICs, the MOSFETs prove its fundamental advantage over other semiconductor devices. MOSFET is one of the best option for ICs beacuse of its following properties:

- High switching speed.
- Majority carrier devices.
- Better Amplifier efficiency.
- Higher packaging density.
- High linearity.

The schematic structure of primary MOSFET and the symbol are shown in Fig. 2.2. It is the essential component of high frequency and switching applications across the electronics industry.

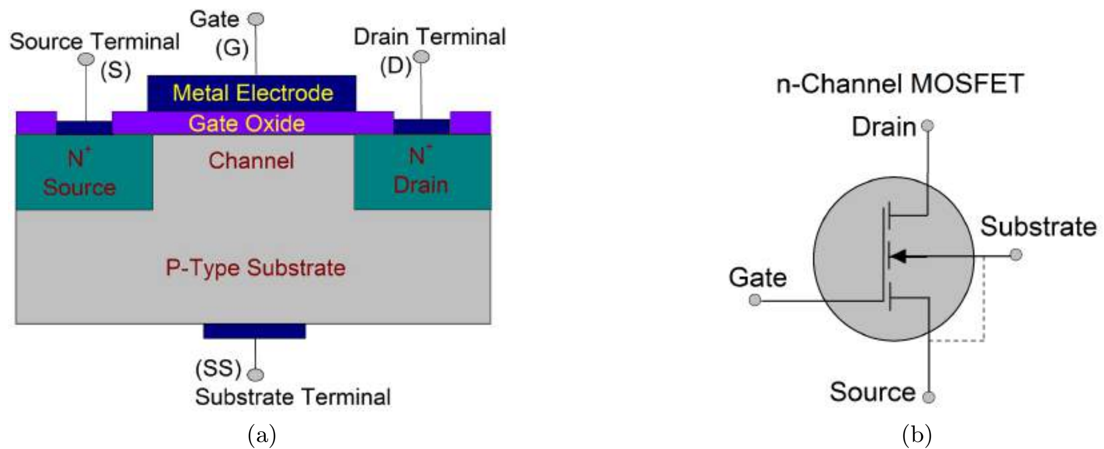


Figure 2.2: (a) Schematic structure (b) Symbol of Basic MOSFET

The IC processing techniques have led to the continuous reduction in both horizontal and vertical dimensions of the devices. To achieve low power, high performance and density, the devices have grown exponentially with the shrink of technological dimensions and fabrication cost of MOSFETs in scale of integration technology as reported by Taur *et al.* and Wong *et al.* [14, 15]. The miniaturization of Si-based bulk MOSFETs face many problems such as short channel effects (SCEs) induced loss of control on electrostatic integrity, high body doping induced high V_{th}

variation, and band-to-band tunneling induced high substrate leakage, etc. To overcome the aforesaid shortcomings, novel **Non-classical MOSFETs** have been intensively investigated which has led to the innovation of Strained Semiconductor, Silicon on Insulator (SOI), Ultra thin BOX (UTB) SOI, Schottky source/drain, multiple-gate MOSFETs (number of channels $>$2, side wall, planar and vertical conduction, tied and independent gates) and high mobility $III-V$ material based MOSFETs. The need for more performance and integration has accelerated the scaling trends in almost every device parameter, such as lithography, channel length, thickness of gate dielectric, body, substrate, varied doping level, supply voltage, device leakage, etc. which have approached their fundamental limits. Alternatives to the existing material and structures may need to be identified in order to continue further growth and fulfill the requirement.

2.2 Technology Node

The co-inventor of the FinFET, Chenming Hu has said "Nobody knows anymore what 16 nm or 14 nm means". The term "node" is the mile marker of Moore's Law. Each node marks a new generation of chip-manufacturing technology. The progression of node names over the years reflects the steady progress that both logic and memory chips have made: Smaller the number, small is the transistor that increase in packaging density, producing chips that are less costly on a per-transistor basis.

But the relationship between node names and chip dimensions is far from reality. Nowadays, a particular node name does not reflect the size of any specific chip feature, as it once did. Moore's Law, when reflected through the steady march of node names, might seem easy and inexorable. Technology Node is the minimum metal line width. In a new node, all features of the circuit reduce by 70% of the previous node. This practice of periodic size reduction is called Scaling. The term "Technology Node" is very often used by ITRS projected data. The ITRS demands are classified as discussed below.

2.2.1 Low Power (LP)

The power consumption has become an important aspect of nanodevice applications in the advent of the mobile era. Among the many key features for future applications like low power consumption, high speed, and high density are all equally significant but one/two become dominantly important depending on applications [16, 17].

Low-power circuit design is a three-dimensional problem involving area, performance and power trade-offs [18–21]. The need for low-power synthesis is driven by battery life and efficiency, device reliability and demand for portable systems. In low-power design, the reduction of peak power, peak power differential, cycle difference power, average power and energy are essential [22]. These forms of power dissipation affects different attributes of a CMOS circuit and needs to be optimized for meaningful low-power design. Various interrelated terms of the power dissipation profile are total energy consumption, static and dynamic power dissipation, delay, power delay product (PDP), energy delay product (EDP) etc. [22, 23], which are carefully investigated in this work.

2.2.2 High Performance (HP)

The devices having high V_{th} have less leakage and greater delay, whereas low V_{th} devices have less delay and high leakage. The threshold voltage dictates the transistor switching speed, i.e. less the threshold voltage higher the switching speed of transistor for an active state. It is required to design the device for HP application in such a manner that provides low V_{th}, which consequently give high drive current [24–26].

2.2.3 Low Standby Power (LSTP)

Due to supply voltage (V_{DD}) scaling, the power consumption remains under control. Hence, the transistor threshold voltage (V_{th}) has to be commensurately scaled to maintain a high drive current and to achieve performance improvement. However, the threshold voltage scaling results in the substantial increase of the subthreshold leakage current [19, 27]. As per Hu the issue - **"OFF" is not Totally "OFF"** [28]. In a typical example– Suppose I_{off} is 100 nA per transistor and a cell phone with 100 million transistor would consume 10 A even in standby. Then the battery will drain in a minute without receiving and transmitting any call. So for low standby operating power, the desirable device need to be of high V_{th}.

2.3 Issues of miniaturization of Device

This section enumerates some of these challenges given due to conventional scaling of MOSFET towards nanoscale -

- High electric fields: causes "avalanche breakdown", in turn current surges and progressive damage to nanodevices. This effect is assignable to applied bias voltage in nanoelectronic devices.

- Heat dissipation: causes malfunction of transistors (and other switching devices) in high-density circuits. This is because of the limited thermodynamic efficiency of nanodevices, which limits their density in circuits.

- Vanishing bulk properties: and non-uniformity of doped semiconductors on small scales. This can only be overcome either by not doping at all (accumulating electrons purely using gates, as in a GaAs heterostructure) or by making the dopant atoms to form a regular array. Molecular Nanoelectronics is one path to the latter option.

- Shrinkage of depletion regions: until they are too thin to prevent quantum mechanical tunneling of electrons from source to drain when the device is supposed to be turned off. The function of nanoelectronic devices is not similarly impaired, because it depends on such tunneling of electrons through barriers.

- Shrinkage and unevenness of the thin oxide layer beneath the gate that prevents electrons from leaking out of the gate to the drain. This leakage through thin spots in the oxide also involves electron tunneling.

To understand the direction for future technology of semiconductor device, the key technologies and design issues including critical technical barriers and corresponding solutions will be reviewed in terms of density (scalability), performance, and power consumption.

With the idea of the projection of ITRS, to continue the Moore's law, desire and development of applications in nanoscale, the generation of critical issues; the study enters towards the research and development of non-classical CMOS Technology.

2.4 Non-classical CMOS Technology

Young [29] in 1989 has clearly documented the major issues SCEs, which are commonly faced by MOSFETs at nanoscale regime. The improvement in performance and reduction of cost can be achieved through geometrical scaling of the transistor in each next technology node, as reported by the research group of Chang *et al.* [30] in 2003. Hence people are searching for new technologies /methodologies. The on going new research gives rise to two paths. One is the introduction of new materials into the classical single gate MOSFETs that is strain [31], and III-V material in the channel which improves the carrier mobility and drive current. Second is the development of non-classical Multigate MOSFETs (Mug-FETs) which is a very good concept for further scaling of the device dimensions as per review of Chaudhry *et al.* [32]. Kumar *et al.* [33] had shown the effect of strain/Ge mole fraction on the threshold voltage for a single gate MOSFET. They have discussed the variations of threshold voltage according to mole fraction, gate length, S/D junction depth, substrate (body) doping, strained silicon thin film thickness and gate work function. The research group of Dunga *et al.* [34] have presented different approaches/technologies under single gate MOSFETs and the advantages of Multigate MOSFETs. The occurrence of an increase in mobility because of implementation of strain in channel demonstrated by them. Besides, the advantage of taking two different materials under strain technology in single and double gate MOSFET has been discussed by Jin *et al.* [35, 36]. Hence an initial observation, several nanoscale device cases with strain engineering are considered under study, for analysis of electrostatic and short channel parameters.

Si-based non-classical MOSFETs mainly point to all kinds of multiple-gate MOSFETs (MugFETs), which have been proposed by Colinge in 2004 to scale down CMOS technology more aggressively, because of its better control of short-channel effects (SCEs) [37]. MugFETs are classified as double-gate (DG) MOSFETs, surrounding-gate (SG) MOSFETs, quadruple-gate (QG) MOSFETs, triple-gate (TG) MOSFETs, cylindrical gate MOSFETs, and so on. Besides the benefits of electrostatic integrity, MugFETs also have some other potential promises.

Another category of non-classical MOSFETs is based on new materials such as III-V group and Germanium (Ge), which are used as other channel materials instead of Si. III-V materials and Ge have been used in transistors, such as SiGe BJTs, heterojunction bipolar transistors (HBTs), and high electron mobility transistors (HEMTs). However, primarily because of the bad quality of dielectric/semiconductor interface, they were not

considered as good candidates for CMOS used in logic circuits [38].

2.4.1 Various Flavors of SOI Platform and it's Advantages

Silicon-on-insulator (SOI) technology features a low capacitance, which enables high-speed operation. The supply voltage can be lowered to cut power consumption while adequate speed is provided. It includes good radiation hardness, the ability to withstand high temperatures; enables the fabrication of micro-electro-mechanical systems (MEMS) for control systems and the ability to handle high voltages. SOI has moved into the mainstream, where it provides important enabling enhancements in circuit performance [39].

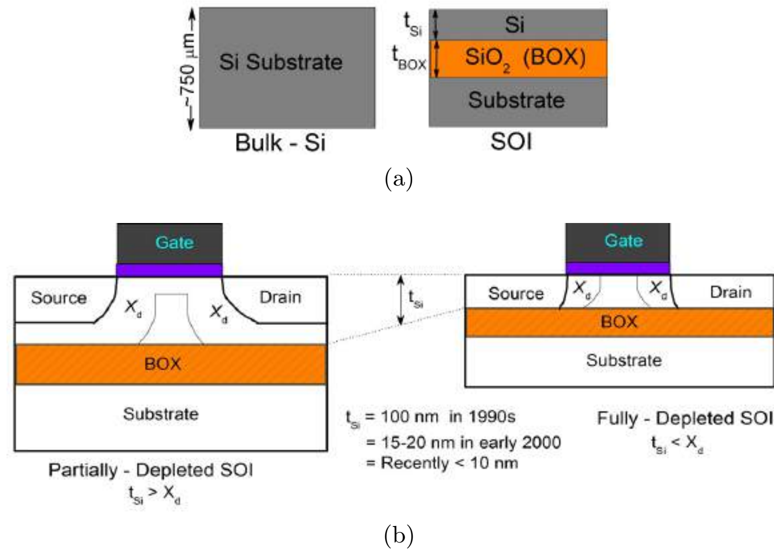


Figure 2.3: Schematic Structures of (a) Bulk-Si and SOI substrates (b) PD and FD SOI

Fig. 2.3 compares the structures of bulk-Si and SOI substrates. The key feature of the SOI structure is the layer of silicon dioxide just below the surface. It is called the buried oxide (BOX) and is made by the oxidation of Si or oxygen implantation into Si, as described later. Regarding the thin Si film on the BOX, if it is single crystal, the MOSFETs made in it are called SOI devices; but if it is polycrystalline, then they are called thin-film transistors (TFT), which is a different category of devices. This film is called the top Si layer, the SOI layer, or just the Si film. The Si substrate beneath the BOX is called Si substrate or supporting substrate or handle wafer, or base wafer. The terms "Si body" and "SOI body" refer to the part of the SOI layer that constitutes the body of a MOSFET.

Devices fabricated on SOI substrates offer superior characteristics over bulk MOS devices documented by Cristoloveanu and Hu in 2001 [40, 41]. Compared to bulk Si, SOI CMOS can run at 20% to 50% higher switching speeds or with a 2 to 3 times lower power consumption for the same speed. Advantages of SOI platform are reduced junction capacitance, increased channel mobility, suppressed short channel effect and reduced second order effects [42]. In 2004, Colinge revealed that the SOI technology furthermore has the flexibility to enable the fabrication of radiation-hardened non-planar (3-D) integrated circuits [37, 43]. The advantages of SOI over bulk are heightened when

the devices are fabricated in thin films. The improvements with thin films leads to increased subthreshold slope, elimination of the kink effect, increased saturation current and transconductance and reduction in hot electron effect. A two-dimensional model for potential distribution and threshold voltage for fully depleted single gate SOI MOSFET has been developed by Aggarwal *et al.* in 1994-95 [44, 45].

Among various SOI MOSFETs, ultra-thin body (UTB) and Multi-gate (MugFET's, Double Gate, Tripple Gate, FinFET's, etc.) represent a promising alternative architecture for future nano-CMOS technology generations. This is due to their superior immunity to short channel effects, lower leakage current and higher drive current as reported in 2002 by Park *et al.* [46].

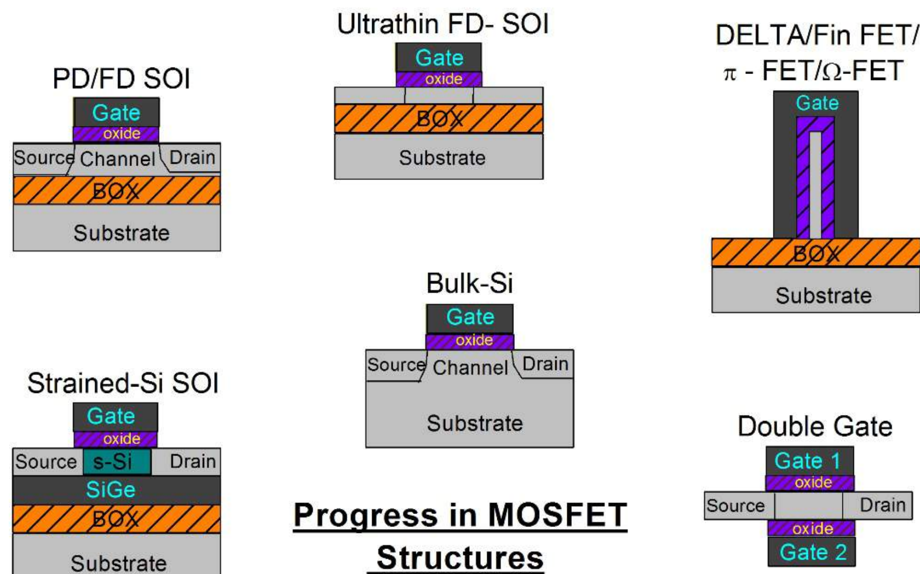


Figure 2.4: Various SOI devices: From Bulk to FinFET

2.4.2 Transport Enhancement through Strain

Strain (lattice-mismatched heterostructure) proposed to enhance mobility and has been studied extensively over past few decades [47–50]. The strain was first proposed in 1950s and since then strain engineering has been one of the most crucial technological innovations. Strain Engineering in semiconductors has been introduced to push the limits of electronic device performance. In 1992, the strained silicon was first used as the MOSFET channel and 70% improvement in mobility as compared to the unstrained counterpart as observed by Welser *et al.* [51, 52]. Enhancement in mobility will further increases the drain current.The strain in crystalline solid is due to the relative displacement of atoms in the lattice. The strain creates proportional distortion in key material properties of semiconductors including reduced energy gap and effective mass of an electron, consequently enhance the mobility. Hence, the creation of strain in the region of the transistor in which mobility of electrons has an effect determining its performance will result in the faster switching transistor [53, 54]. Common methods to generate strain includes strain-graded buffer layers, which creates uniaxial, and biaxial strains. The two can provide dislocation-free materials. The mobility degradation and

the high defect levels associated with current Silicon-Germanium (SiGe) are based on biaxially strained silicon or strained Silicon on Insulator (s-SOI) as published by Paskiewicz *et al.* [55]. Several chip manufacturers including Intel and Texas Instruments, have successfully demonstrated the significant benefits of uniaxial strain at the transistor level. Intel pioneered the use of uniaxial strain-enhanced transistor technology and is already using it in its 90 nm process.

2.4.3 Double Gate (DG) MOSFET

Double-gate (DG) SOI MOSFETs have two symmetrical interconnected gates. Three possible orientations of a double-gate MOSFET can be planar, vertical, or mixed-mode (vertical film with side gates and horizontal transport) as reported by Taur *et al.* [14] which is shown in Fig. 2.5. The fabrication of such devices has been achieved with the delta process, [56] epitaxial lateral overgrowth, [57] wafer bonding, [58, 59] Fin process, [60] and tunnel epitaxy, [61].

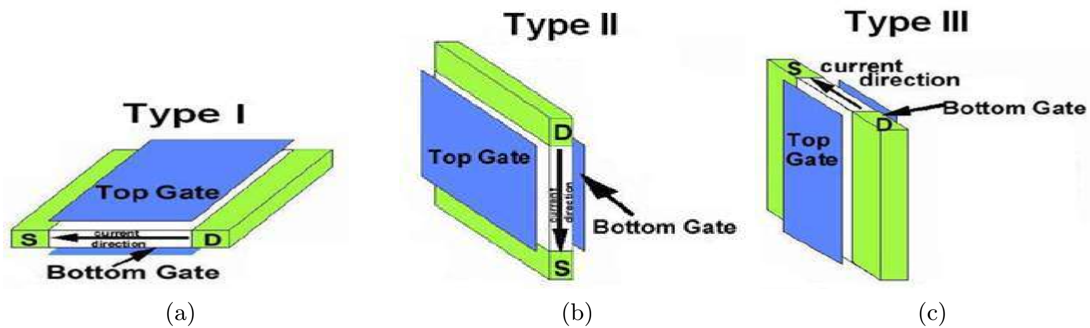


Figure 2.5: Schematic Structures of DG-MOSFET with different layout(a) planar (b) vertical (c) mixed-mode

The DG concept was initially demonstrated back in 1987 by Balestra *et al.* [62] on conventional SOI MOSFETs with simultaneously biasing the front and back gates of a FD transistor. The Si film is of DG-MOSFET have to be thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of this device is similar to that of two conventional MOSFETs connected in parallel. However, if the Si thickness is sufficiently reduced, the whole silicon film is depleted and an important degree of interaction takes place between the two potential wells. In such conditions, the inversion layer is formed not only at the top and bottom of the silicon slab (i.e., near the two silicon-oxide interfaces), but throughout the entire silicon film thickness. The device is then said to operate in volume inversion, i.e., the carriers are no longer confined to one interface but are distributed throughout the entire silicon volume. The formation of the front and back inversion channels are caused by continuity and volume inversion (VI) in thin SOI films. The minority carriers flow in the middle of the film and experience less surface scattering; hence the mobility, transconductance, drive current, and $1/f$ noise are improved. The two gates exert ideal control on the potential and inversion charge, so that SCEs (charge sharing, DIBL, fringing field, and punch through) are highly reduced. This is because the

intrinsic length λ_{DG} is much lower in DG MOSFETs, as compared to single gate (SG) transistors. They are now considered as the final metamorphosis of the MOS transistor as reported by Frank *et al.* in 1992 [63]. Several authors have claimed that volume inversion presents a significant number of advantages, such as:

- an enhancement of the number of minority carriers;
- an increase in carrier mobility and velocity due to reduced influence of the scattering associated with oxide and interface charges and surface roughness;
- as a consequence of the latter, an increase in drain current (I_D), and transconductance (g_m);
- a decrease in low-frequency noise;
- a great reduction in hot carrier effects ($HCEs$);
- a steep subthreshold slope (SS) [64, 65].

In addition, like other dual gated devices, DG-MOSFETs are claimed to be more immune to short channel effects (SCEs) than bulk silicon MOSFETs and even than single-gate fully depleted SOI MOSFETs [66]. Wind *et al.* have circulated in 1996 the fact that the two gate electrodes jointly control the carriers, thus screening the drain field away from the channel [67]. And Wong *et al.* added in 1998 that this characteristic would permit a much greater scaling down of these devices than ever imagined for conventional MOSFETs [61].

Along with the growth DG MOSFETs, it also suffer from considerable short channel effects in the sub 100 nm regime. A new device structure triple metal (TM) DG MOSFET is developed to improve the device immunity against the short channel effects and therefore improve the device reliability in high performance circuit applications as reported by the research group of Razavi *et al.* in 2008 and Tiwari *et al.* in 2010 [68, 69]. This new structure gives an improving SCEs such as drain induced barrier lowering (DIBL), hot carrier effects (HCEs) and reducing channel length modulation (CLM). It also improves the drive current (I_{on}), sub threshold slope (SS), leakage current (I_{off}) and transconductance (g_m). Three laterally contacted materials with different work functions have been taken for gate electrode of the device. Material work functions will be selected in such a way that work function near the source will be highest and near the drain will be lowest for n-channel MOSFET. As a result, the electric field and electron velocity along the channel suddenly increase near the interface of the two gate materials, resulting in increased gate transport efficiency. The low work function near the drain side reduces the peak electric field at the drain side and reduces the hot carrier effect when compared to single material gate structure as per study of Goel *et al.* and Chen *et al.* in 2009 [70, 71]. A large number of alternative dielectric materials such as $Si_3N_4, HfO_2, TiO_2, La_2O_3, LaAlO_3$ and $SrTiO_3$ with high dielectric constants are developed for gate stack engineering (i.e one thick layer of high-k dielectric is taken over one thin layer of low-k dielectric). Although the full

potential of emergent phenomena has not yet been realized for oxides grown on silicon, the marriage between conventional semiconductors and oxides clearly promises to combine semiconductor electronics with correlated electronic systems. While we are taking the high dielectric materials over the SiO_2 layer, the effective oxide thickness (EOT) is given by:

$$\text{Equivalent high-}k = T_k(k_{SiO_2}/k_{high-k})$$
$$EOT = \text{Equivalent } SiO_2 + \text{Equivalent high-}k$$

Where, T_k is the physical thickness of the high-k material and k_{SiO_2}, and k_{high-k} are permittivity of SiO_2 and high-k material respectively. From the above relation, films with high-k value are thicker than SiO_2 film and still have the same control over the MOSFET.

It has already been verified by device simulation that the use of high-k gate dielectrics directly on silicon wafer would degrade the short channel performance. This degradation is mainly caused by the fringing fields either from the gate to the source/drain regions or from the source/drain to the channel region, which weakens the gate control [72, 73]. But these issues to some extent can be taken care of by gate stack (GS) configurations i.e. high-k dielectrics over silicon dioxide layer [74]. A thick layer of dielectric material over a thin SiO_2 layer keeping EOT constant significantly reduces the gate tunneling current.

Current research creates a platform for the study of analog and RF performance for the nanoscale devices. It is known from various research groups like Colinge in 1998, Razavi in 1999, Kilchytska *et al.* in 2003, Mohankumar *et al.* in 2010, Sarkar *et al.* in 2012 and Sharma *et al.* in 2012 that for analog and RF circuits, intrinsic gain, cut off frequency, linearity and noise figure constitute the performance criteria [75–80]. Extensive simulations have been carried out to study various important electrostatic and dynamic parameters of MugFETs with HKMG technology.

The SCEs [81] tend to degrade analog figures of merit (FoMs) such as transconductance (g_m), early voltage (V_{EA}), g_m/I_D ratio which is the transconductance generation factor (TGF) and the intrinsic dc gain (g_m/g_d). Moreover, V_{EA} and TGF which are the key analog FoMs of a technology, show the efficiency of the devices to convert DC power into AC frequency and the gain performance. To resolve this issue, the role of asymmetric channel doping like single halo (SH) and double halo (DH) on various performance metrics has been reported in 2004 by Kranti *et al.*, Reddy *et al.* and in 2007 by Li *et al.*, Chakraborty *et al.* [82–85]. In continuation to their work, a systematical study has been done to analyze the gate and channel engineering on various performance metrics.

The development of non-classical Multigate MOSFETs (Mug-FETs) which is a very good candidate at nanoscale dimensions as documented by Colinge [86]. However, the Integrated Device Manufacturer (IDM), foundries and Electronic Design Automation (EDA) companies give more investments and emphasis on most promising 3-D FinFET technology. The FinFET technology is becoming more widespread as feature sizes within integrated circuits fall and there is a growing need to provide much higher levels

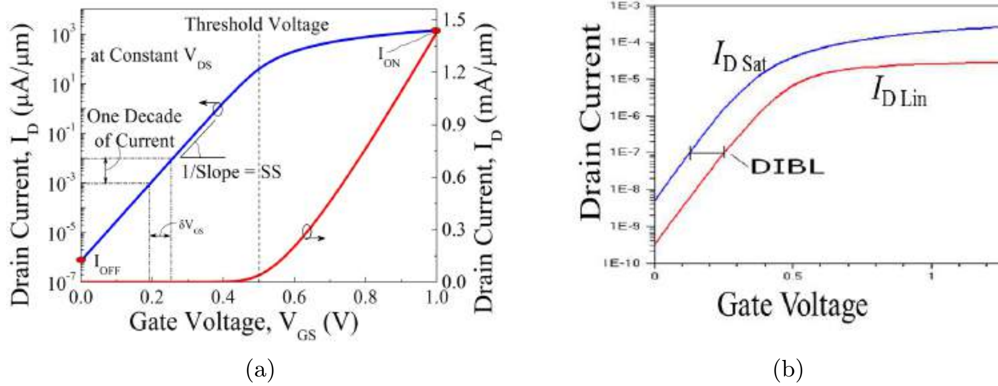
of integration with less power consumption within integrated circuits. FinFETs are not available as discrete devices. So, it is essential to simulate the Fin based devices for studying the performance variation in view of analog and RF circuit application. In continuation of our previous study on DG-MOSFET (2-D perspective of FinFET), an extended attempt has been made to present a deep analysis of process variability dependency on various performance metrics of 3D FinFET.

2.5 Device Performance metrics

The importance of performance analysis at device level is studied minutely. From the above literature study, the investigation move towards the SCEs by using non classical MOSFET structures such as ultra thin SOI, DG-MOSFET and FinFETs. Adjustment of threshold-voltage of the device for HP application is a challenging requirement, which is achieved by tunning the metal gate work function. The highest possible gate overdrive at a given Ioff and reducing the parasitic capacitances are another challenge. Non-planar structures, such as DG-MOSFET and FinFETs, with various device engineering to optimize the device structure in view of better performance metric using 3-D simulations are needed.

2.5.1 Static Performances

Drain induced barrier lowering ($DIBL$) and sub-threshold swing (SS) are important short channel parameters, and is essential to analyze these parameters in nanoscale device design. In a short-channel device, the source-drain potential have a strong effect on the band bending over a significant portion of the device. Therefore, the threshold voltage, and consequently the sub-threshold current of short-channel devices, are varied with the drain bias. This effect is referred to as $DIBL$ and can be calculated as Eq. 2.1. $DIBL$ occurs when the depletion regions of the drain and the source interact with each other near the channel surface to lower the source potential barrier.



(a) (b)

Figure 2.6: (a) Demostration of Subthreshold Slope (SS), Leakage Current (I_{off}), On Current (I_{on}), and Threshold Voltage (V_{th}) in $I_D - V_{GS}$ characteristics (b) $DIBL$

$$\text{DIBL} = \frac{\Delta V_{th}}{\Delta V_{DS}} = \frac{V_{th1} - V_{th2}}{V_{DS2} - V_{DS1}} \tag{2.1}$$

The CMOS standby power is affected by the subthreshold current. MOSFETs designed for low power consumption and high-speed nanoscale digital applications are mainly operated in the subthreshold regime. The subthreshold current has a major influence on the dynamic circuits. Hence, a steep subthreshold slope (SS) is required for switching operation. This parameter is mathematically represented as Eq. 2.2 [87].

$$\mathrm{SS} = \left[\frac{\partial \log_{10}(I_D)}{\partial V_{GS}} \right]^{-1} \tag{2.2}$$

Switching Performance

Essential components to achieve high-performance levels in the amplifier are the minimization of power loss, time delay and voltage supply to as much as possible. Therefore, a ideal device needs low voltage drop, fast on and off switching times and low parasitic inductance. Amplifier efficiency is related to MOSFET by total power losses. These power losses of MOSFET are the resultant of conduction loss, losses due to switching and Gate charge. MOSFET conduction loss is directly related to R_o (Output-Resistance) parameter. Conduction loss can be calculated as follows:

$$P_{CONDUCTION} = (I_D)2 \times R_o = I_D \times V_{DD}$$

R_o is temperature-dependent that increases with increase in junction temperature. Proper care must be taken during the thermal design to avoid thermal runaway effect. These conduction loss is inversely proportional to the size of the MOSFET; the larger the switching transistor, the lower its R_o and, therefore, its conduction loss. Therefore, lower R_o results in lower MOSFET conduction loss and consequently gets better amplifier efficiency. This is illustrated as below.

$$\text{Lower } R_o \Longrightarrow \text{Lower } P_{CONDUCTION} \Longrightarrow \text{Better efficiency}$$

For ultralow-power systems, the V_{DD} must be lowered without diminution of the operating speed. It can be achieved by reducing the threshold voltage of the MOSFETs. The power dissipation is mainly of two types (i) dynamic power dissipation involved in total capacitance and (ii) static power dissipation is due to the subthreshold leakage current. The relationship between the two is shown in Fig. 2.7. Low-V_{th} transistors with a small leakage current are useful for making suitable low-voltage analog switches. At higher supply voltages, the dynamic power dissipation is dominant, and the total

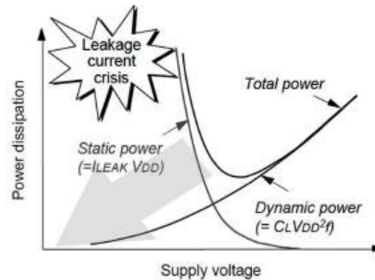


Figure 2.7: Power Dissipation versus Supply Voltage

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power decreases in proportion to the square of the supply voltage. But, when the supply voltage drops below a certain point, the threshold voltage of the MOSFETs must be minimized. It causes the static power dissipation due to the leakage current to increase exponentially; so, the total power dissipation also increases. Hence, the suppression of the leakage current is the main issue in the nanoscale device.

Intrinsic Delay

When new device structures are explored, we rely on International Technology Roadmap for Semiconductors (ITRS) projections and aim to meet the required I_{on} for the specified supply voltage, I_{off} , electrostatic integrity, and parasitic components [7]. The projected drive current in ITRS is to fulfill the requirement of the intrinsic transistor delay based on the CV/I metric, which is an optimistic figure of merit for the performance.

The transistor delay is simply approximated by $C_{tot}V_{DD}/I_D$, where V_{DD} is the supply voltage and I_D is the drain current at $V_{GS} = V_{DS} = V_{DD}$. Here C_{tot} represents the total capacitance of the MOSFET. Increasing of the capacitance is a viable approach to increase the drive current and, thereby, decrease the transistor delay. The higher drive current gives high voltage drop across the source series resistance. In other words, the effective velocity is the main lever for reducing the delay.

2.5.2 Analog & RF Performance

The analog and RF circuits with a CMOS technology suffers from many challenges. Moreover, the technology is optimized for digital design, and the devices are characterized by the current drive and gate delay. For System on Chip (SoC) and System in Package (SiP) applications, optimization of the devices become more challenging [7, 12, 13]. Here SiP refers to a semiconductor device that incorporates multiple readily available chips into a single package while SoC refers to a device that includes a system of differently functioning circuit blocks on a single silicon chip. So it is required to enhance the performance for digital and analog/RF circuit applications [76–80, 88–90]. Major semiconductor companies such as IBM, RFMD, Honeywell, OKI, etc., have already produced several products for the telecommunication market based on SOI RF technologies.

More electrical systems are being integrated on chips with the development of technology. As the need for analog, interfaces is increasing along with advances in networking, so the importance of analog and RF performance is being felt as essential.

Analog Performance

Most analog circuits employ a combination of three basic analog functions [91]:

- Conversion from gate voltage to drain current (V-to-I). The coefficient is the transconductance (g_m).
- Conversion from the drain current to drain voltage (I-to-V). The coefficient is the drain resistance (r_d).

- Conversion from gate-to-source voltage to drain-to-source conductance (V-to-G). The coefficient is the on-conductance (G_{on}).

The ratio of transconductance to drain current ($TGF = g_m/I_D$) is a very important figures of merit (FoMs) as far as analog circuits concerned. Transconductance Generation Factor (TGF) demonstrates the efficient use of the current to achieve a desired value of transconductance. The high value of TGF is advantageous to realize analog circuits that are operating at low supply voltages. The mathematical relation among DC gain, TGF and early voltage ($V_{EA} = I_D/g_d$) can be expressed as Eq. 2.3.

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\Delta I_D}{g_d}.\frac{1}{\Delta V_{in}} = \frac{g_m}{g_d} = \frac{g_m}{I_D}.V_{EA} \tag{2.3}$$

where g_d is the output drain conductance and V_{EA} is the early voltage [92]. This equation tells larger is the g_m/I_D ratio better is the analog device. On the other hand, there are two types of g_m/I_D ratio as given in Eq. 2.4, 2.5 [75,93]-

For weak inversion:

$$\frac{g_m}{I_D} = \frac{\partial I_D}{I_D.\partial V_G} = \frac{\ln(10)}{S} = \frac{q}{nkT} \tag{2.4}$$

Strong inversion:

$$\frac{g_m}{I_D} = \sqrt{\frac{2\mu C_{ox}W/L}{\eta I_D}} \tag{2.5}$$

The factor η, which is related to the body coefficient, is a measure of the coupling between the gate voltage and the surface potential. It is also known as process parameter.

The SCEs [81] tend to degrade analog FoMs such as transconductance (g_m), early voltage (V_{EA}), g_m/I_D ratio or transconductance generation factor (TGF) and the intrinsic dc gain (g_m/g_d). Moreover, V_{EA} and TGF are the key analog FoMs and show the efficiency of the devices to convert DC power into AC frequency and the gain performance. In view of this, a systematic estimation of analog and RF performance measure are presented in this work with different engineering approaches for better results.

RF Performance

The three primary RF characteristics are:

- Cut-off frequency (f_T), which is the frequency at which the current gain is equal to unity;
- Maximum oscillation frequency (f_{max}), which is the frequency at which the power gain is equal to unity; and
- Minimum noise figure (NF_{min}), which is given by Fukui's approximation with K as a fitting factor [94].

The formulae for these parameters are:

$$\begin{aligned} f_T &= \frac{g_m}{2\pi(C_{gs}+C_{gd})} \\ f_{\max} &= \frac{f_T}{2\sqrt{(R_g+R_i)(g_d+2\pi.f_T.C_{gd})}} \\ NF_{\min} &= 1 + K.\frac{f}{f_T}.\sqrt{g_m(R_g+R_s)} \end{aligned} \tag{2.6}$$

where g_m: Transconductance, C_{gs}: Gate-source capacitance, C_{gd}: Gate-drain capacitance, R_g: Gate resistance, R_i: Real part of the input impedance due to non-quasi-static effects, R_s: Source resistance, g_d: Drain conductance.

The downscaling of CMOS devices has resulted in significant improvements in the RF performance of bulk and SOI MOSFETs [95–97]. It is evident from Eq. 2.6 that increase in f_T is possible by reduction in the gate length, f_{max} depends strongly not only on g_m and g_d, but also on parasitic components. Research are now under way to investigate and optimize the device structures to improve the RF FoMs.

2.5.3 Linearity Performance

Most of the useful output power is wasted, if the MOSFET shows non-linear behavior. Moreover, the second order and third order transconductance terms i.e. g_{m2} and g_{m3} are especially major concern for RF systems. Higher orders of g_m are crucial for linearity analysis of the circuit. These are much more important for applications like mobile communications where mobile receivers are extensively analyzed and designed for high linearity. There are numerous closely existed bands, nearby unwanted bands also get processed with desired ones only because of higher order g_m. The higher order transconductance terms should be minimal for high linearity to make the circuit work in the real time environment. Further some important linearity FoMs like VIP_2 (2nd order voltage intercept point), VIP_3 (3rd order voltage intercept point), IIP_3 (3rd order input intercept point) , and $1-dB$ compression point are used to estimate the distortion characteristics from dc analysis. Here VIP_2 represents the input voltage at which the first and second harmonic voltages are equivalent. Similarly, VIP_3 can be explained as the input voltage where the first and third order harmonic voltages are same. Where IIP_3 serves as the input power at which first and third order harmonic powers are equal. VIP_2, VIP_3 and IIP_3 should be as high as possible for better performance [98]. The linearity FOMs are g_{m1}, g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3 and $1-dB$ compression point and defined as in Eq. 2.7, 2.8, 2.9, 2.11 respectively [99, 100]:

$$g_{mn} = \frac{\partial^n I_{ds}}{\partial V_{gs}^n} \qquad n = 1, 2, 3 \tag{2.7}$$

$$VIP_2 = 4\frac{g_{m1}}{g_{m2}} \tag{2.8}$$

$$VIP_3 = \sqrt{24\frac{g_{m1}}{g_{m3}}} \tag{2.9}$$

$$\begin{aligned} &IIP_3 = \tfrac{2}{3}\tfrac{g_{m1}}{g_{m2}R_S} \\ &Where\ R_S = 50\,\Omega\ for\ most\ analog\ and\ RF\ applications. \end{aligned} \tag{2.10}$$

$$1-dB\ compression\ point = 0.22\sqrt{\frac{g_{m1}}{g_{m3}}} \tag{2.11}$$

2.6 Enhanced Performance at Device level using various Engineering

2.6.1 Gate Stack

Reduction in the gate length of the device increases drive currents while it also necessitates a decrease of the gate oxide thickness (t_{ox}) to maintain electrostatic control of the charges induced in the channel. One of the major limitations in scaling of CMOS devices is the gate dielectric thickness [30, 101–105]. The conventional silicon dioxide (SiO_2) as gate dielectric has reached the level where the film thickness is only a few atomic layers thick. At these dimensions or below 1.5 nm, direct tunneling of carriers dramatically increases the leakage current that consequently increases the static power and affects the circuit operation [32, 106]. The high-k dielectrics have been introduced by depositing it directly on the silicon wafer or on the silicon dioxide layer for avoiding the critical problem. While keeping the equivalent oxide thickness (EOT) constant, high-k dielectrics permit the increase in physical thickness (by a factor of k_{high-k}/k_{SiO_2}) of the gate oxide to inhibit gate tunneling [107, 108].

High-k is used as the non-conventional architecture for improving electron transport efficiency of the device. In 45 nm technology node and beyond, the high-k dielectrics (mostly HfO_2) are used in gate stacks to achieve a low equivalent oxide thickness (EOT) with the aim to reduce the gate leakage current, the threshold voltage and supply voltage [7]. However, one of the key issues is the process induced defect that degrades device mobility resulting in poor performance and reliability [109–113].

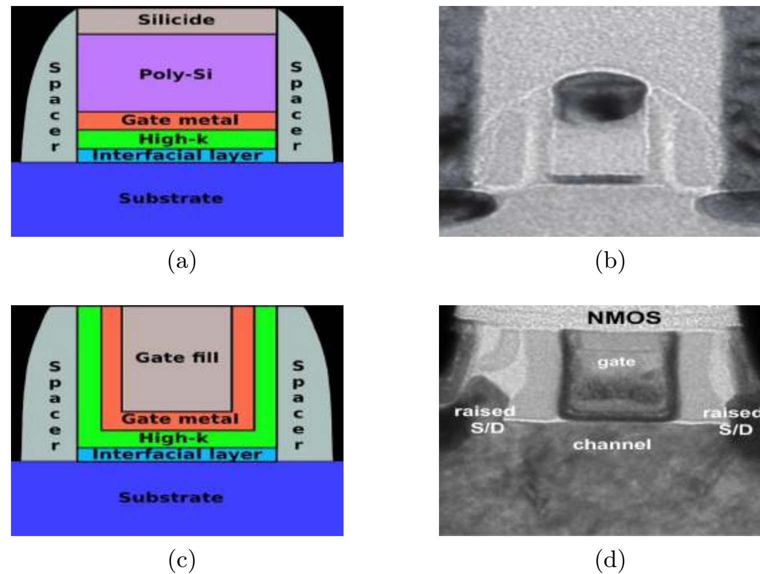

Figure 2.8: (a) Schematic view of the high-k/metal gate stack in a gate-first integration scheme and (b) Cross-section of a gate-first MOSFET manufactured by IBM, (c) Schematic view of the high-k/metal gate stack in a gate last integration scheme and (d) Cross-section of a gate last MOSFET manufactured by Intel.

However, the continual gate oxide scaling requires high-k gate dielectrics, for suppressing the leakage current induced by the thin gate oxide layer. Similarly, the concept of gate oxide stack (i.e. a thick layer of high-k oxide is sandwiched with a thin

layer of SiO_2) has been proposed by Hu and Wong [106, 114, 115]. The high-k gate stack also improves SCEs like drain induced barrier lowering (DIBL), hot carrier effects (HCEs), channel length modulation (CLM) and increases the drive current to leakage current ratio (I_{on}/I_{off}) in sub-100 nm DG-MOSFETs as reported by Inani *et al.* [116].

The introduction of high-k dielectrics in manufacturing has required the concurrent integration of metal gate technology, because of the observed incompatibility of high-k dielectrics with conventional poly-Si gate electrodes, resulting in thermodynamic instability, difficulties in setting the threshold voltage and mobility degradation. Therefore, the two technologies are usually considered together and are referred to as high-k/metal gate technology (HKMG), i.e. the gate-first and gate-last integration schemes [117] Fig. 2.8 is reproduced from Greene *et al.* [118] and Packan *et al.* [119].

2.6.2 Gate Metal Work Function Engineering

According to the ITRS High Performance (HP) strategy, metal gate is the efficient high-performance booster due to its small EOT and may dominate the market. But the selection of a proper gate metal with appropriate work function (ϕ_m) is necessary. The metal work function, ϕ_m is a crucial consideration in the selection of gate materials for device integration because it directly affects the V_{th} and the performance of a transistor. Several high melting point refractory metals e.g., tungsten (W), titanium (Ti), tantalum (Ta), molybdenum (Mo), rubidium (Ru) etc. have been investigated [32, 120]. Various types of metal gate electrodes have been studied as a replacement for poly-Si, such as Mo, Ta, TaN, TiN etc.. Two separate metals with appropriate work function are needed to obtain symmetric devices for CMOS, compatibility.

Metal gates are used for the V_{th} control of UTB devices and show reduced SCEs. Further, metal gates are more compatible with high-k gate dielectrics than poly-Si gates. A Large reduction in gate leakage and sub-threshold swing projects the high-k metal gate technology as a reliable alternative to future nanoscale MOS devices.

2.6.3 Channel Engineering

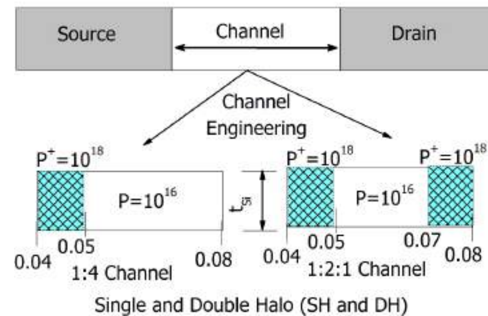

Figure 2.9: Lateral Asymmetric Channel (LAC) in the device

The doping concentrations of the source and drain side are changed to get the asymmetric channel in MOSFET. It is otherwise termed as halo doping (single and double halo), which provides in transition channel potential due to non-uniformity. It also creates an impact on the mobility of the carriers in the channel. This channel

engineering shown in Fig. 2.9 is used to boost the performance of the device in view of analog/RF FoMs.

2.7 TCAD - Technology Computer Aided Design

Downscaling of MOS devices makes the physical dimensions of the transistors to reach a point where simple physical models of dopant distribution and device behavior are not valid any longer. It is necessary to understand the coupling between process conditions, the static and dynamic behavior of the devices, and the required performance of the resulting integrated circuit. Thus, as more ambitious devices were designed and fabricated, it became apparent that computer simulations would play a crucial role in the development of this new technology. Computer simulations made it possible to understand the related process and device effects. Furthermore, their significant advantages compared to the experimental approach are the rapid turn-around time and the much lower cost.

Computer experiments based on suitable and adjusted models can be carried out much faster than manufacturing expensive test structures and they enable to find many properties of the devices in an early stage of the development process of new technologies. Furthermore, the understanding of the physical processes that occur during the fabrication and the operation of the devices are depended. Hence, using predictive simulations, devices can be optimized in an early phase and the manufacturing processes can be improved not only with respect to the quality of the resulting devices but also with respect to manufacturing throughput.

TCAD is purely physics-based simulation. TCAD tools model the behavior of semiconductor devices using fundamental physical models like the current continuity (drift-diffusion), carrier energy transport (hydrodynamic model), Poisson equations and quantum mechanical wave equations. TCAD tools typically operate at the device level. Tools that go beyond simple models and integrate TCAD with SPICE (Simulation Program with Integrated Circuit Emphasis) models are usually referred to as "mixed-mode" simulators [121, 122]. The two major components of a TCAD design process are process simulations and device simulations. Current major suppliers of TCAD tools include Synopsys, Silvaco, and Crosslight. Nowadays, TCAD simulations are an paramount activity for the IC industry since it makes it possible to explore technologies and concepts that do not yet exist in reality. TCAD simulations also provide information about the inner workings of devices, thus simplifying improvements on existing technologies are possible. A complete TCAD simulation involves the following steps:

- Virtual fabrication of the device using a process simulator or a device editor.
- Creation of a mesh suitable for device simulation.
- Device simulation that solves the equations describing the device behavior.
- Post processing, i.e., generation of figures and plots.

2.7.1 Silvaco (ATLAS)

Atlas is a tool under the TCAD. It enables device technology engineers to simulate the electrical, optical, and thermal behavior of semiconductor devices. Atlas provides a physics-based models, easy to use, modular and extensible platform to analyze DC, AC and time domain responses for all semiconductor based technologies in 2 and 3 dimensions. It accurately characterizes as physics-based devices in 2D or 3D for electrical, optical, and thermal performance without costly split-lot experiments. It also solves, yields the process variation problems for optimal combination of speed, power, density, breakdown, leakage, luminosity, or reliability of semi-conducting devices.

Tonyplot and Extraction of Parameters

TonyPlot is a powerful tool designed to visualize TCAD 1-D and 2-D structures produced by Silvaco TCAD simulators. Tonyplot provides visualization and graphic features such as pan, zoom, views, labels and multiple plot support. Tonyplot also provides many TCAD specific visualization functions such as HP-4154 emulation, 1-D cut lines from 2-D structures, animation of markers to show vector flow, integration of log or 1-D data files and fully customizable TCAD with distinct colors and styles.

2.7.2 Device Design through Sentaurus

The TCAD process and device simulation tools support a broad range of applications such as CMOS, power, memory, image sensors, solar cells, and analog/RF devices. In addition, Synopsys TCAD provides tools for interconnect modeling and extraction, providing critical parasitic information for optimizing chip performance [123]. Sentaurus Device is an advanced multidimensional device simulator capable of simulating electrical, thermal, and optical characteristics of silicon-based and compound semiconductor devices. It is a new-generation device simulator for designing and optimizing current and future semiconductor devices. It explores new device concepts for which fabrication processes are not yet defined.

Sentaurus Structure Editor is a 2-D and 3-D device structure editor, and a 3-D process emulator based on CAD technology. The boundaries and materials should describe the device structure. This step can be performed in two different ways. The first and easiest one is to use a device editor. This program is very much like a drawing program; the structure is created and edited using the mouse or a script. The other approach involves actual computer simulations of each process step; this procedure is called process simulation. The generation of a device using a device editor is similar to making a drawing of the device; several basic geometrical elements are available like rectangles, cuboid and lines. Each of these geometrical elements is also defined in terms of materials (aluminum, silicon, oxide, polysilicon, etc.). To perform a device simulation, an accurate mesh suitable for the device simulation is needed, since it is a finite element method (FEM), simulation. Extra refinements of the grid are also involved particularly near interfaces between different materials.

Chapter 3

Modeling and Simulation of Non-classical MOSFETs

The Non-classical MOSFETs at sub-100 nm is the best choice for HP and LP applications. However, serious issues are SCEs, the need to control V_{th}, and the steeper SS. Thus, the performance of new device designs with various engineering must be analyzed in the nanoscale regime. This attempt will indeed make a significant contribution towards the application of the miniaturized devices.
This chapter describes a preliminary study of various SOI non-classical MOSFETs in the nanoscale regime. This case studies are helpful to understand the issues of Nanodevices and motivate to perform various performance analysis that is also needful towards the circuit application, discussed in the rest of the chapters.

In the last 50 years, with advancement in miniaturization of the devices, the size of structures in applied physics has shrunk from the centimeter scale in electrical engineering, through electronics and microelectronics, to less than 100 *nm* in nanoelectronics. With the transistor miniaturization, the undesirable SCEs generated, and need to be minimize. One of the approaches to solve this problem is to provide a new improved transistor architectures [124].

SOI offers moderate speed or power improvements over bulk technology as IBM, AMD, and other semiconductor companies are producing devices using SOI technology. The role for SOI is to provide a novel MOSFET structures whose gate lengths can be scaled down to 25 *nm*, where bulk MOSFET scaling is very difficult [41]. Strain engineering in SOI substrate is very popular for enhancing the carrier mobility. An analytical modeling study of strained channel MOSFET that discusses the SCEs in view of surface potential and threshold voltage is given below.

3.1 Single Gate Strained Channel MOSFETs

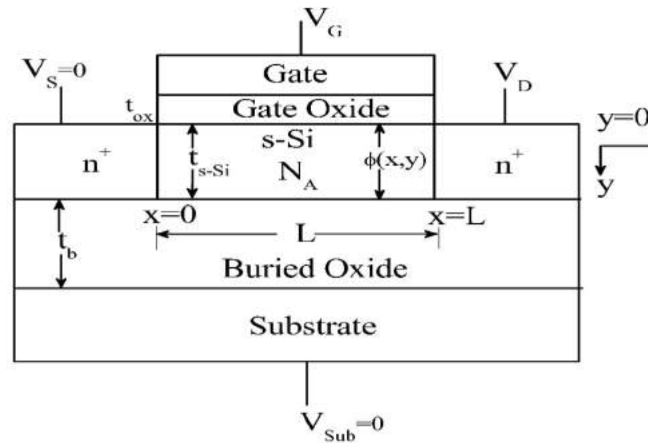

Figure 3.1: Schematic structure of FD-s-SOI MOSFET

A Fully Depleted-Strained-SOI MOSFET by varying the channel length (100 *nm*,60 *nm* and 30 *nm*) is considered. The Schematic structures of FD-s-SOI MOSFET is shown in Fig. 3.1 and device dimensions as given in Table 3.1.

Table 3.1: Description of FD-s-SOI

Attributes	**Values**
Channel Length (L_g)	100 nm, 60 nm, 30 nm
Channel thickness (t_{sSi})	20 nm
Thickness SiO_2 (t_{ox})	2 nm
Channel Doping (N_A)	1×10^{17} cm^{-3}
S/D Doping (N_D)	1×10^{20} cm^{-3}
Thickness of BOX (t_b)	100 nm
Strain coefficient (x)	0.2
Substrate thickness	100 nm
Gate Work Function	4.8 eV

The primary aim is to analysis a physics based 2-D model for surface potential, threshold voltage and electric field for a Fully Depleted Strained Silicon on Insulator

(FD-s-SOI) MOSFET by solving the 2-D Poisson's equation (details as per appendix-A 7.1). The model specifies the role of the device parameters like strain (equivalent Ge mole fraction in the relaxed SiGe buffer), gate length scaling, body doping density, gate metal work function, strained silicon thickness, gate oxide thickness on the surface potential, electric field and threshold voltage is studied.

3.1.1 Impact of various parameters on Surface Potential

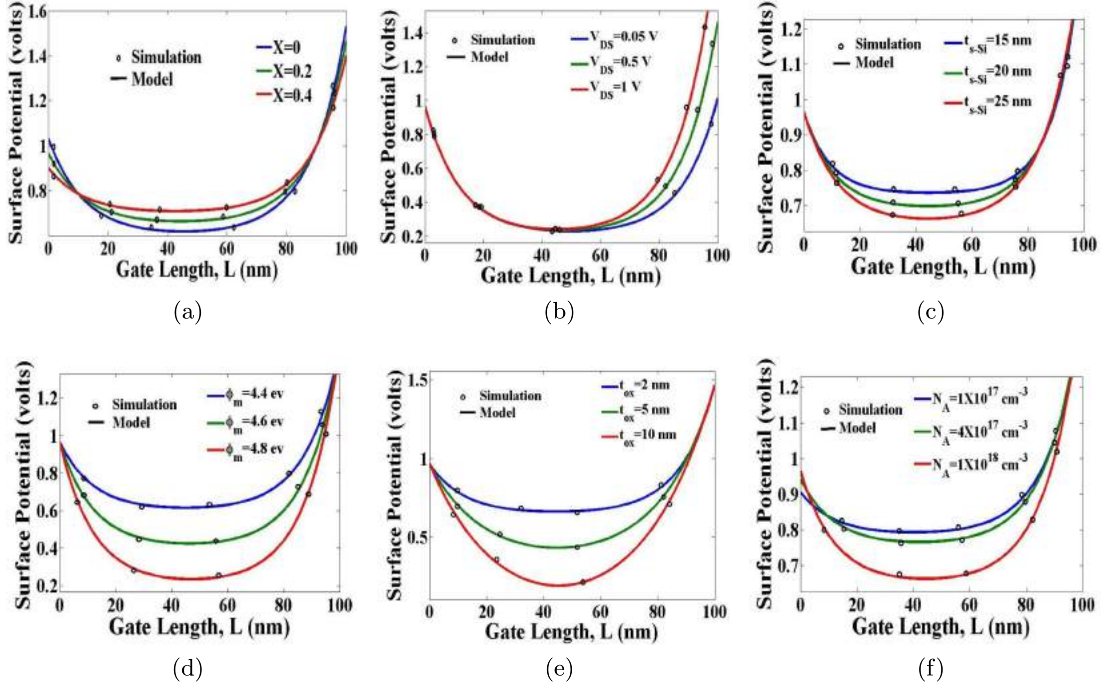

Figure 3.2: Surface potential as function of channel lenghth (L) with impact of (a) Ge concentration x (b)drain to source voltage V_{DS} (c) strain silicon thickness t_{s-Si} (d) metal gate work-function ϕ_M (e) oxide thickness t_{ox} (f) channel doping N_A. Otherwise the parameters used are as follows: $V_{sub} = 0\,V, N_A = 1 \times 10^{18}\,cm^3, t_{s-Si} = 25\,nm, t_{ox} = 2\,nm, t_b = 100\,nm, V_{DS} = 0.5\,V, x = 0.2$, and $\phi_M = 4.35\,eV$.

It can be seen from Fig. 3.2 (a) that the potential barrier is increasing with an increase in x but decreases at source and drain end. From the Fig. 3.2 (b) no significant change in the potential at the source end and a very minute change at the drain end found due to the presence of Ge mole fraction. As a consequence, V_{DS} has only a very small influence on drain current after saturation and it is evident from the figure that there is a negligible shift in the point of minimum potential irrespective of the applied drain bias. Therefore, DIBL is considerably reduced. When the silicon film thickness is reduced, the controllability of the gate over the surface channel becomes stronger in comparison to the influence exerted by the source/drain as shown in Fig. 3.2 (c). It can be seen from Fig. 3.2 (d), higher the metal gate work function leads to a better control of the channel potential minima. The controllability of the gate increases when the oxide thickness is reduced, but at the same time it becomes more prominent to SCEs as per Fig. 3.2 (e). Tunneling through the oxide and hot-carrier effects decrease the reliability of the device when oxide thickness reaches a certain level. Fig. 3.2 (f) concludes as the

doping concentration increases the surface potential minimum decreases in the channel region, but it is quite constant in drain side. Hence, DIBL decreases and the immunity to control the SCEs are increased.

3.1.2 Electric Field and Threshold Voltage

The electric field at the drain side considerably reduces with increase in x value as shown in Fig. 3.3. This reduction of the electric field experienced by the carriers in the channel can be interpreted as the reduction of the hot-carrier effect at the drain end. Fig. 3.3 (b) shows the variation of the threshold voltage along the channel for three different work function values of gate metal ϕ_M. As it can be seen from the figure, choosing a gate metal M with a higher work function leads to a better control of the V_{th} value.

It is observed from Fig. 3.3 (c) that SCEs become apparent when the channel length is below $50-60\ nm$ and is marked by sharp decrease in the V_{th} value. The gate-source/drain (S/D) charge is sharing and source-body/drain-body built-in potential barrier lowering due to an overlap of the lateral source body and drain body depletion regions becomes significant for such short channel lengths. Fig. 3.3 (d) shows the variation of the threshold voltage along the channel for different strained-Si thin film thicknesses. V_{th} reduces as strained-Si thin film thickness decreases. This is because of the decrease in the total depletion charge under the gate, leading to an early onset of inversion. Thus, increasing in thickness of the strained-Si thin film leads to higher V_{th}.

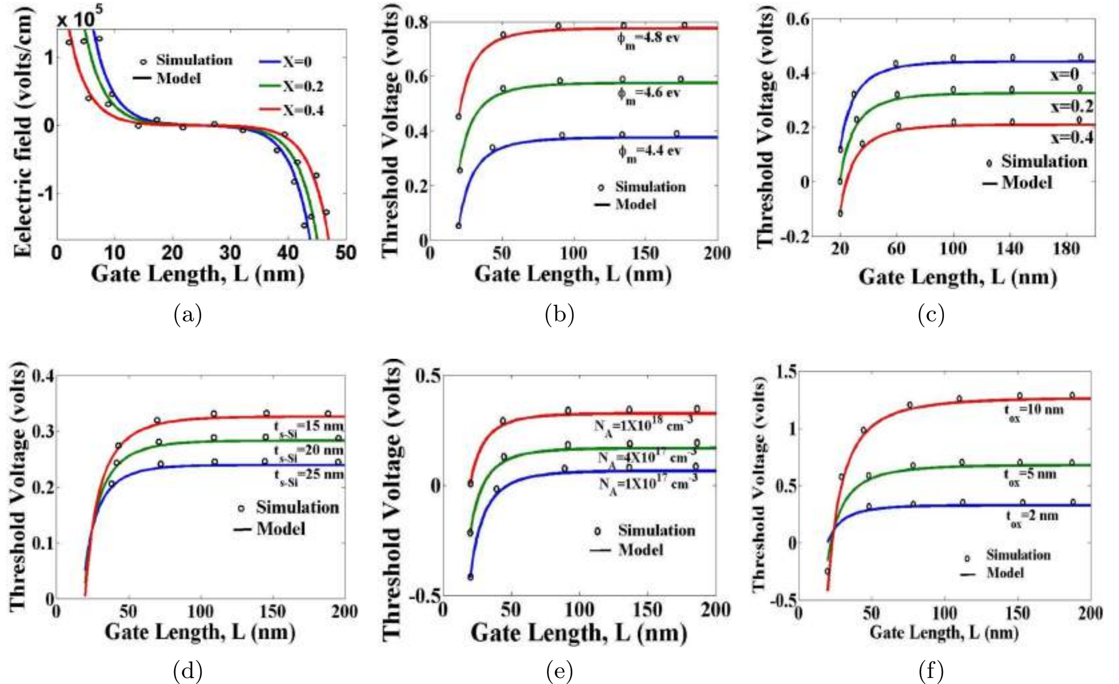

Figure 3.3: (a) Variation of Electric Field along the channel for different values of x. Threshold Voltage as function of channel length (L) with impact of (b) metal gate work-function ϕ_M (c) Ge concentration x (d) strain silicon thickness t_{s-Si} (d) channel doping N_A (e) oxide thickness t_{ox}. The parameters used are as follows: $V_{sub} = 0\ V, N_A = 1 \times 10^{18}\ cm^3, t_{s-Si} = 25\ nm, t_{ox} = 2\ nm, t_b = 100\ nm, V_{DS} = 0.5\ V, x = 0.2$, and $\phi_M = 4.35\ eV$.

As shown in the Fig. 3.3 (e), the threshold voltage increases with increased body doping and a "roll-up" in the characteristics is observed at lower channel lengths. Hence, the scaling of the device can go to some more extent without any further increase in SCEs by increasing the body doping concentration. The reduction in gate oxide thickness (t_{ox}), decreases the threshold voltage that is the requirement for a faster device as Fig. 3.3 (f). Therefore, continuous scaling down of the oxide thickness gives rise to faster devices but on the other hand, oxide thickness cannot be scaled down to nanoscaleÂăvalues because tunneling through the thin oxide and hot carrier effects become prominent.

There is a significant drop in threshold voltage with increasing strain and decreasing channel length. The rise in strain, i.e., equivalent Ge content, enhances the performance of s-SOI MOSFETs in terms of improved transconductance and speed because of an increase in the carrier mobility. However, as demonstrated by our results, there are undesirable side effects with increasing equivalent Ge content such as a roll off in V_{th}, which may affect the device characteristics and performance significantly.

With the knowledge of SCEs and the dependence of the device parameters, the investigation continues towards MugFETs. Now the study in next section follows on the device double gate (DG) MOSFET with an implementation of rare structural Engineering.

3.2 Various Structural Engineering on DG-MOSFET

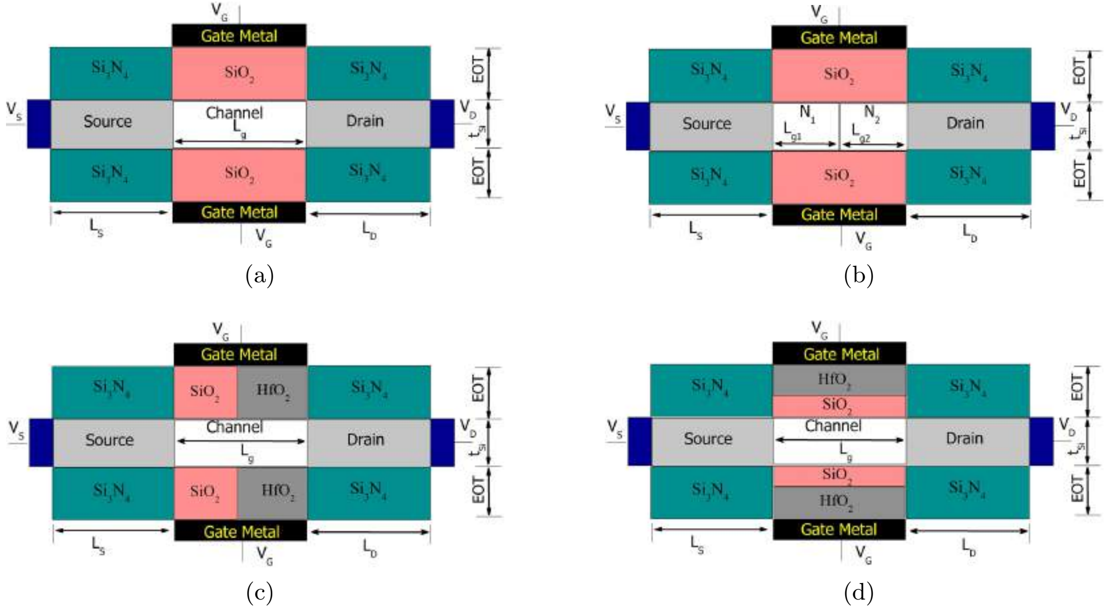

Figure 3.4: Schematic structure of (a) UD-DG (b) GC-DG (c) DI-DG (d) GS-DG MOSFET

Different structures are considered for the comparative study on the performance of Double Gate (DG) MOSFET with different channel and gate engineering. The schematic structures of Fully Doped DG MOSFET (FD-DG-MOSFET), Un-Doped DG MOSFET (UD-DG-MOSFET), Graded Channel DG MOSFET (GC-DG-MOSFET), Dual Insulator DG MOSFET (DI-DG-MOSFET) and Gate Stack DG MOSFET

(GS-DG-MOSFET) are shown in Fig. 3.4. In all structures channel length (L_g) is fixed as 40 nm as well as Source/Drain length (L_S/L_D). The silicon thickness (t_{Si}) as 10 nm and a uniform doped of $N_D = 10^{20}\ cm^{-3}$ is taken. The channel is doped $N_A = 10^{18}\ cm^{-3}$ in FD-DG, FD-DI-DG, FD-GS-DG, for UD-DG it is $10^{15}\ cm^{-3}$ and for GC-DG a high low profile of doping is taken as $10^{18}\ cm^{-3}$ and $10^{17}\ cm^{-3}$. The oxide thickness $t_{ox} = 2\,nm$ for all structures except FD-GS-DG where a high-k (HfO_2) gate stack of $3\,nm$ is chosen over SiO_2 layer. In all structures a low-k spacer (Si_3N_4) is taken for improvement of the device performance. The work function for the gate materials is assumed as $4.77\,eV$.

3.2.1 Analysis of Results

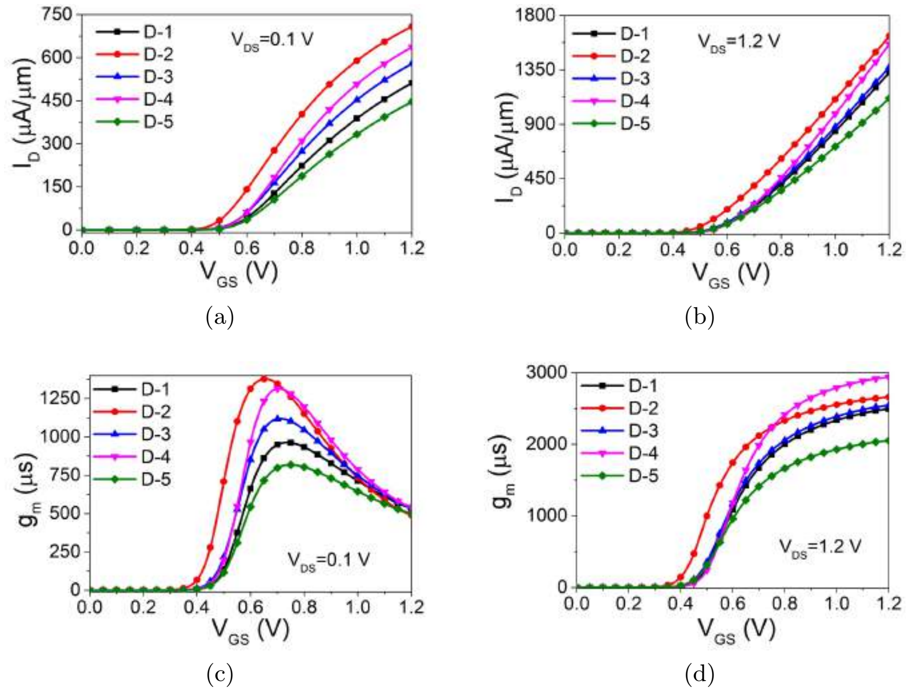

Figure 3.5: Behavior of Drain Current (I_D) and variation of transconductance (g_m) as a function of Gate Voltage(V_{GS}) (a),(b) $V_{DS} = 0.1V$ (d), (e) $V_{DS} = 1.2V$ for all structures.

The Fig. 3.5 gives a clear picture of $I_D - V_{GS}$ transfer characteristics curve and transconductance (g_m) as a function V_{GS} for all the structures.

The surface potential and E-field of the five devices $V_{DS} = 0.1\ V$ and $1.2\ V$ is given in Fig. 3.6. As seen from the figure the DI have more uniform electron drift through the channel. It is clearly visible from the figure the different in the value of the permittivity of the gate oxide material for DI-DG results one additional peak. The peak value of the electric field at drain side minimizes the HCE and impact ionization.

Threshold voltage (V_{th}) is also a crucial parameter for higher on state current which improves the circuit speed. The V_{th} is extracted by calculating the maximum slope of the $I_D - V_G$ curve, finding the intercept with the x-axis and then subtracting half of the applied drain bias as given in Table for drain bias of $0.1\ V$ and $1.2\ V$. Fig. 3.5 shows sub-threshold slope of all structures in both low and high gate bias. The UD-DG shows

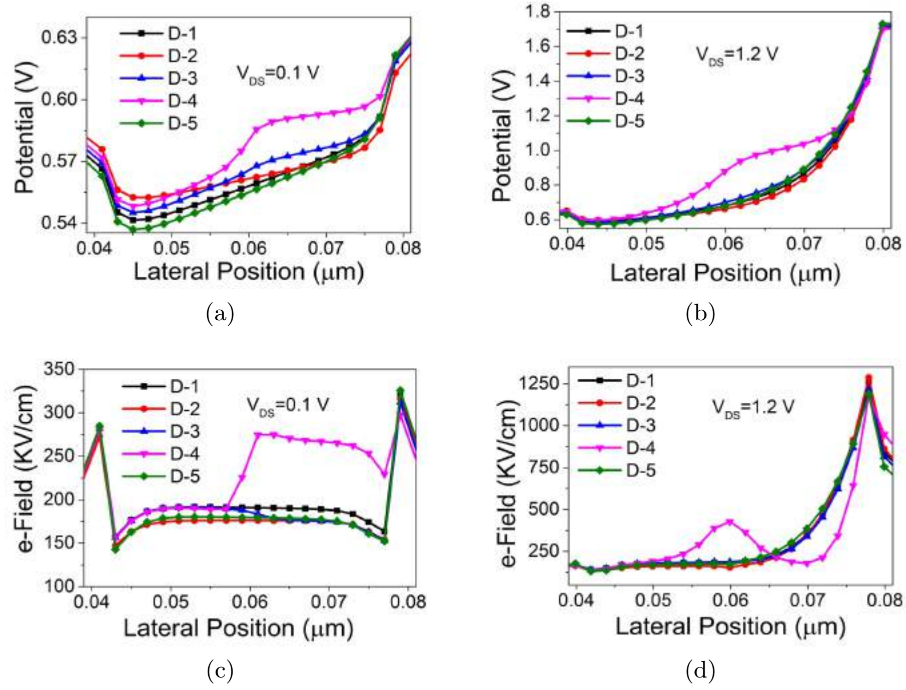

Figure 3.6: Surface Potential and Electric Field along the channel for different models at (a), (c) $V_{DS} = 0.1\,V$ (b), (d) $V_{DS} = 1.2\,V$.

a lowest V_{th}. And GC-DG gives lower among others because of the high-low doping profile taken for Graded Channel; V_{th} is directly related to the doping profile. However, the doping profile being same for DI-DG and FD-DG MOSFETs, the DI-DG MOSFET exhibits a lower V_{th} than FD-DG MOSFET, which enables its speed of operation. The increment of g_m leads to higher intrinsic gain that gives better RF application.

Table 3.2: Extraction of V_{th} and max I_D from Fig. 3.5.

Model	as	Threshold Voltage		Max Drain Current	
		V_{th} at $V_{DS} = 0.1\,V$	V_{th} at $V_{DS} = 1.2\,V$	$I_D(mA)$ at $V_{DS} = 0.1\,V$	$I_D(mA)$ at $V_{DS} = 1.2\,V$
FD-DG	D-1	0.518	0.367	0.511	1.32
UD-DG	D-2	0.448	0.312	0.708	1.62
GC-DG	D-3	0.503	0.306	0.578	1.37
FD-DI-DG	D-4	0.511	0.268	0.636	1.56
FD-GS-DG	D-5	0.521	0.256	0.446	1.11

After simulating variety of structural Engineering, our focus continues toward gate stack (GS) DG-MOSFET. The investigation is extended with the implementation of lateral asymmetric channel (LAC) with tri material (TM) in GS-DG-MOSFET.

3.3 Implementation of LAC with TM (Triple Material) in GS-DG MOSFET

An investigation is made on the SCEs of TM-DG MOSFET in comparison with the conventional DG MOSFET. A new device structure triple material (TM) double gate

(DG) MOSFET is developed to improve the device immunity against the SCEs. The work function for the gate materials is assumed:for single material DG MOSFET $\phi_{m1} = 4.8\,ev, \phi_{m2} = 4.8\,ev, \phi_{m3} = 4.8\,ev$ and for triple material (TM) DG MOSFET $\phi_{m1} = 4.8\,ev, \phi_{m2} = 4.6\,ev, \phi_{m3} = 4.4\,ev$. A performance comparison is done between between Gate Stack Double Gate (GS-DG), GS-DG-Single Halo (SH), GS-DG-Double Halo (DH), GS-DG Tri-material (TM), GS-DG TM-SH and GS-DG-TM-DH MOSFETs as shown in Fig. 3.7. The above structures are renamed as D-1, D-2, D-3, D-4, D-5 and D-6 respectively. The channel length (L_g) and Source/Drain length (L_S/L_D) is kept as 40 nm. The silicon thickness (t_{Si}) as 10 nm and a uniform density N_D as $10^{20}\,cm^{-3}$ is taken. The channel is doped with impurity concentration of $N_A = 10^{16}\,cm^{-3}$. In each case, the effective oxide thickness is 1.1625 nm. The thickness of SiO_2 and equivalent HfO_2 are 1 nm, 0.1625 nm respectively. To get the equivalent thickness of the high-k as 0.1625 nm, the physical thickness is calculated as 1nm. The channel engineering SH and DH was implemented in GS-DG models in a ratio of 1:4 and 1:2:1 respectively with $N_A = 10^{18}\,cm^{-3}$ as shown in Fig. 3.7 (b) . The control gate M1 (toward the source side) and screening gates M2 and M3 (toward the drain side) are the gate electrodes with lengths LM1, LM2 and LM3 (LM1: LM2:LM3 = 1:2:1).

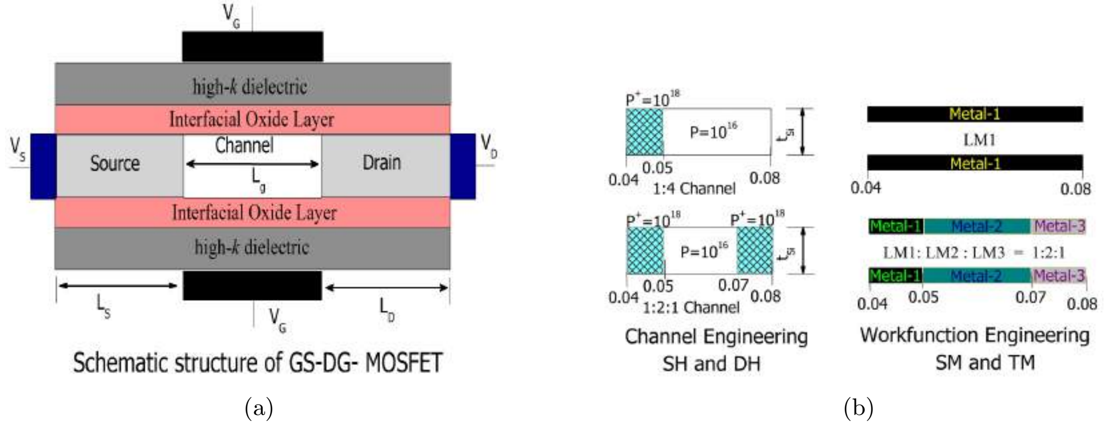

Figure 3.7: Schematic structure of (a) GS-DG (b) Implementation of channel and work function Engineering in GS-DG MOSFET.

3.3.1 Analysis of Electrostatics Parameters

Fig. 3.8 shows the simulated electron mobility, electric field and surface potential along the channel position for various configurations at $V_{DS} = 0.1V$. In the GS-TM technology, the work function difference between M1, M2 and M3 causes an abrupt change in the conduction band energy at the silicon surface. This generates two steps in the electric field peak profile that give rise to two peaks in the channel with a high electric field at the source side as shown in Fig. 3.8 . Thus, for the GS-DG-TM MOSFETs, the electric field at the drain end is reduced and the source carrier injection into the channel is enhanced. But the models with halo doping gives high electron mobility as they show low electric field in the channel region because electron mobility is inversely proportional to the electric field. In Fig. 3.9 (a), (b) $I_D - V_{GS}$ transfer characteristics have been shown on linear scale for all six different device structures and have been compared for

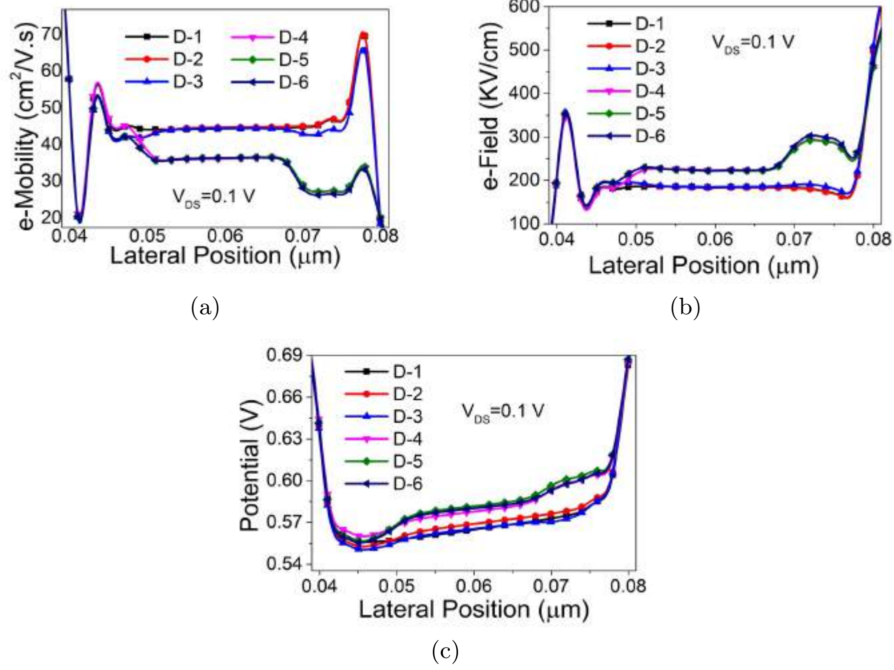

Figure 3.8: (a) Electron Mobility (b) Electric Field (c) Surface Potential at $V_{DS} = 0.1\,V$ along the channel (cutline at Y=4 nm) for different models

$V_{DS} = 100\,mV$ and $1\,V$. The GS-DG-TM provides higher drain current in comparison to all other configurations. The halo doping on both, the source and drain end, show a lower drain current because higher doping concentration reduces the surface mobility. The g_m versus V_{GS} characteristics have been compared for all six device structures in Fig. 3.9 (c) and (d) for $V_{DS} = 100\,mV$ and $1\,V$. Fig. 3.10 shows the threshold voltage and transconductance variation for all device configurations. The threshold voltage (V_{th}) is extracted by calculating the gate to source voltage V_{GS} at $I_D = 1 \times 10^{-6}\,A/\mu m$. The value of g_m is extracted by taking the derivative of the $I_D - V_{GS}$ curve. All the values are summarized in Table 3.3.

Table 3.3: Extracted Parameters for GS-DG-TM

Name	V_{th1} (V)	$SS1$ $(mV/Decade)$	g_{m1} (mA/V)	I_{on1} (mA)	V_{th2} (V)	$SS2$ $(mV/Decade)$	g_{m2} (mA/V)	I_{on2} (mA)
	$V_D = 0.1\,V, V_g = 0\,V - to - 1.2\,V$				$V_D = 1\,V, V_g = 0\,V - to - 1.2\,V$			
D-1	0.49	62.14	1.78	0.63	0.11	62.33	3.51	1.37
D-2	0.5	62.19	1.62	0.59	0.13	62.5	3.45	1.26
D-3	0.5	62.17	1.45	0.55	0.13	62.42	3.44	1.26
D-4	0.38	67.86	1.69	0.7	0.04	68.27	3.82	1.77
D-5	0.41	70.33	1.53	0.64	0.07	70.63	3.74	1.6
D-6	0.41	70.25	1.5	0.63	0.07	70.57	3.73	1.6

A close comparison of various design engineering such as the channel and gate engineering on the DG-SOI MOSFETs are studied. The GS Engineering along with the halo implantation i.e. GS-DG-SH and GS-DG-DH configurations have demonstrated significant improvements in the device characteristics such as SS value, electron

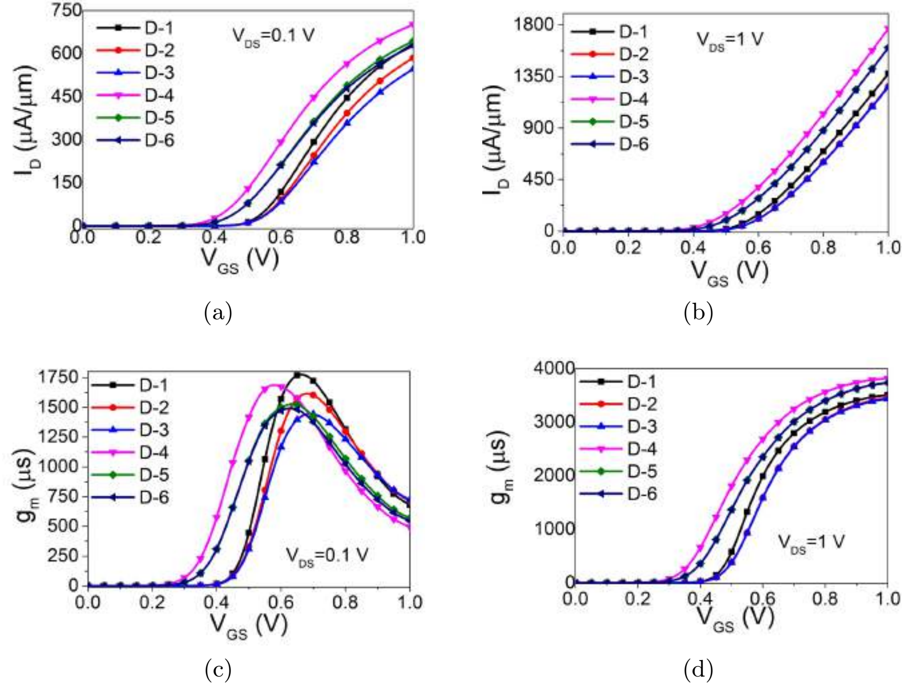

Figure 3.9: Drain Current (I_D) as a function of Gate Voltage (V_{GS}) at (a) $V_{DS} = 0.1\,V$ (b) $V_{DS} = 1\,V$ and Variation of g_m as a function V_{GS} (c) $V_{DS} = 0.1\,V$ (d) $V_{DS} = 1\,V$ for all models.

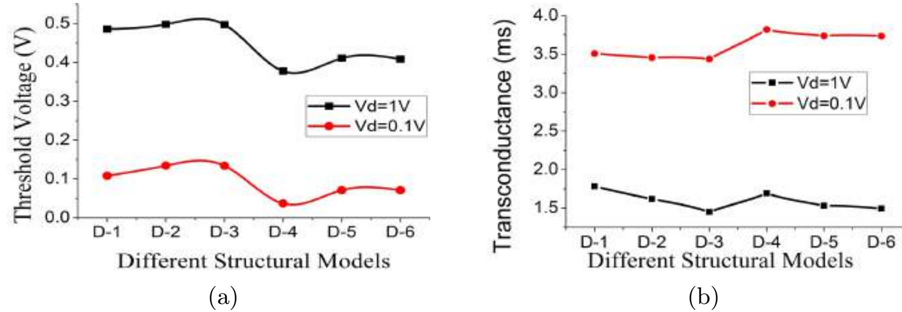

Figure 3.10: (a) Threshold Voltage (V_{th}) (b) Transconductance (g_m) variation of different models

mobility and leakage current. On the other hand by applying gate engineering with halo implantation i.e. GS-DG-TM-SH and GS-DG-TM-DH exhibits a higher value of drain current, the peak transconductance and a lower value of $DIBL$.

Due to higher electric field the generated hot carriers may also be trapped in the oxide region of MOSFETs, leading to interface-trap buildup and the trapping of carriers in the oxide. Thus, trapped charges in the oxide region of MOSFETs change the potential profile of the channel and have adverse effects like shifting the threshold voltage. They may compromise the operation of the device by generating charged defects in the oxide layer, and by degrading the oxide and the $Si - SiO_2$ interface. These effects constitute a reliability problem. Hot carriers also generate unwanted current components. Hence, analysis of hot carriers [125, 126] becomes one of the most crucial tasks in nanoscale MOSFETs. So the impact of interface trapped charges are investigated as follows.

3.4 Analytical Modeling of nanoscale DG-MOSFET with Interfaced Trapped Charges

An analytical modeling for surface potential and threshold voltage of Fully Depleted (FD) DG-MOSFET is studied by solving the 2-D Poisson's equation. The degradation due to the hot carrier effect is investigated in short-channel devices. The developed surface potential model includes the effect of both positive as well as negative interface charges. The calculated minimum surface potential is used to develop the threshold voltage model. Based on the model, the interdependence of the device parameters, such as the silicon film thickness (t_{Si}), oxide thickness (t_{ox}), channel length (L) are investigated. The parabolic potential approximation method is utilized while solving the two-dimensional (2D) Poisson's equations along with the assumption that the interface charge distribution is uniform along the channel [127, 128]. The details of mathematical modeling given in Appendix 7.1. The simulation results from Sentaurus are utilized to verify the obtained model.

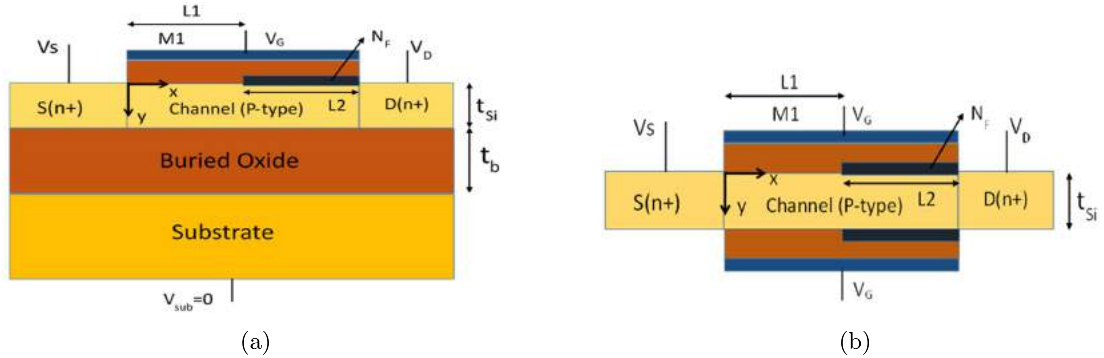

Figure 3.11: Schematic Structure of UTB (a) Single Gate and (b) Double Gate, Fully Depleted Silicon on Insulator MOSFET with Damaged Region

The schematic diagram of the ultra-thin body (UTB) single gate (SG) and double-gate (DG) MOSFET structures are used for modeling and simulation as shown in Fig. 3.11. The device has uniformly doped source-drain with doping concentration of $N_D = 1 \times 10^{20}\ cm^3$. The channel is kept lightly doped with doping concentration of $N_A = 1 \times 10^{16}\ cm^3$. The gate oxide thickness, buried oxide thickness and the silicon are $t_{ox} = 2\ nm, t_b = 50\ nm$ and $t_{Si} = 10\ nm$, respectively. Damaged region due to the interface oxide trapped charges (N_F) is shown in Fig. 3.11 with black line and labeled as distance L_2.

3.4.1 Analysis of Hot Carrier Induced Degradation in DG-MOSFET

Fig. 3.12 (a) shows an analogy of surface potential between SG and DG by maintaining all the parameters at a constant value. From the figure it can be clear that the DG device has more control over the channel as compared to SG device. This is because of two gates i.e. front and back gates in case of DG.

Fig. 3.12 (b) shows the surface potential variation along the channel length for different amount and polarity of interface trapped charges in the oxide for SG and DG.

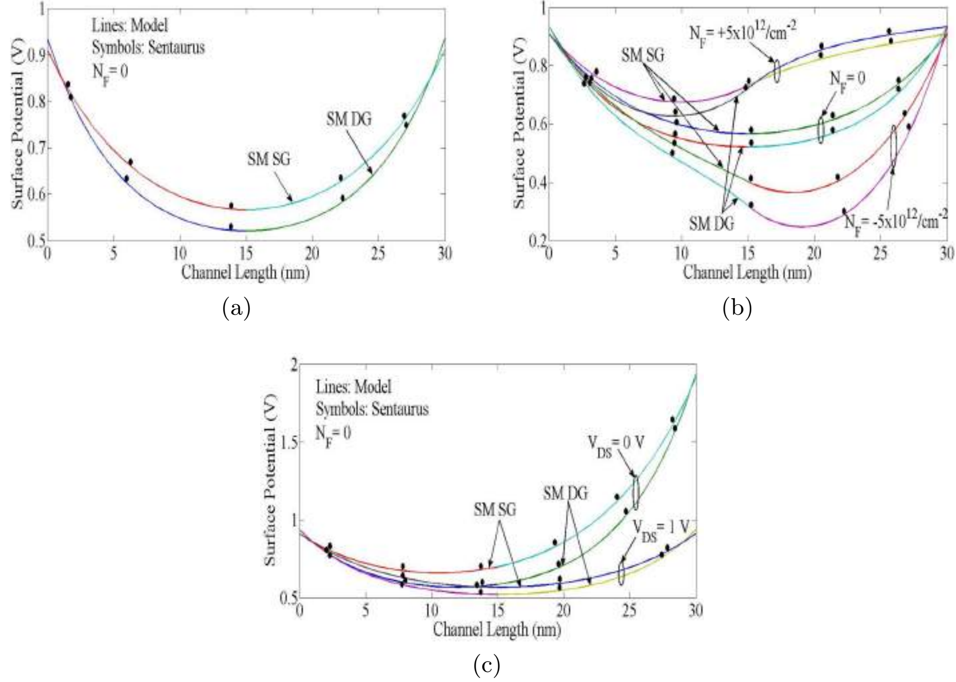

Figure 3.12: Comparison of Surface potential for Single and Double Gate (a) without trapped charges , (b) with different trapped charge (c) for unlike V_{DS}. Parameters used $\phi_M = 4.6\,eV, N_A = 1 \times 10^{16}\,cm^3, t_{Si} = 10\,nm, L = 30\,nm, t_{ox} = 2\,nm, V_{DS} = 0\,V$ and $V_{GS} = 0.1\,V$.

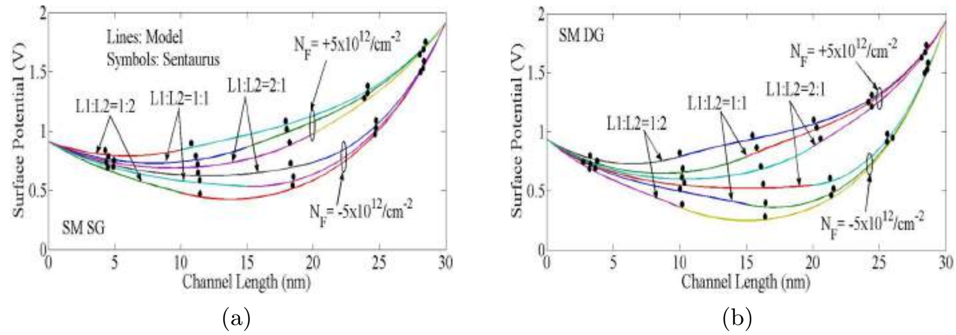

Figure 3.13: Surface Potential variation along the channel length for interface charge variations for different damaged region length ratios ($L1/L2$=1:2, 1:1, 2:1) of (a)Single Gate, (b) Double Gate device. Parameters used $\phi_M = 4.6\,eV, N_A = 1 \times 10^{16}\,cm^3, t_{Si} = 10\,nm, L = 30\,nm, t_{ox} = 2\,nm, V_{DS} = 0\,V$ and $V_{GS} = 0.1\,V$.

The minimum of the surface potential is at the channel center for the device having $N_F = 0$ and moves towards the source and drain side for positive and negative interface charge cases respectively. Positive interface charge will cause higher SCEs on the device than its counterparts due to lower barrier height. However, the device having negative interface charges will cause more $DIBL$ as the minimum potential point shifts towards the drain side. So both +ve and -ve interface charges are undesirable for the device performance. It can be observed that DG device has higher barrier height with less prominent to interface trap charges. Fig. 3.12 (c) demonstrates the variation of channel potential minima with respect to drain voltage is much smaller in case of DG than SG

which minimizes the $DIBL$ effect.

Fig. 3.13 (a) and (b) depict the surface potential variation along the channel length. In case of positive interface charges, with increase in the length of damaged region i.e. $L2$, minimum surface potential raises and shifts it towards the source side. The position of the minimum surface potential is closer to source for a greater length of $L2$. This indicates a higher SCEs in the device as the $L2$ extends more. It further lower the source channel barrier height and hence a higher threshold voltage roll-off. However, in case of negative interface charges, the increase of the length of $L2$ region decreases the minimum surface potential. It gives a higher source-channel barrier height and hence a lower V_{th} roll-off. The shifting of the minimum surface potentials is opposite as in case of the positive interface charge i.e. the minimum surface potential point shifts towards drain side with shorter $L2$.

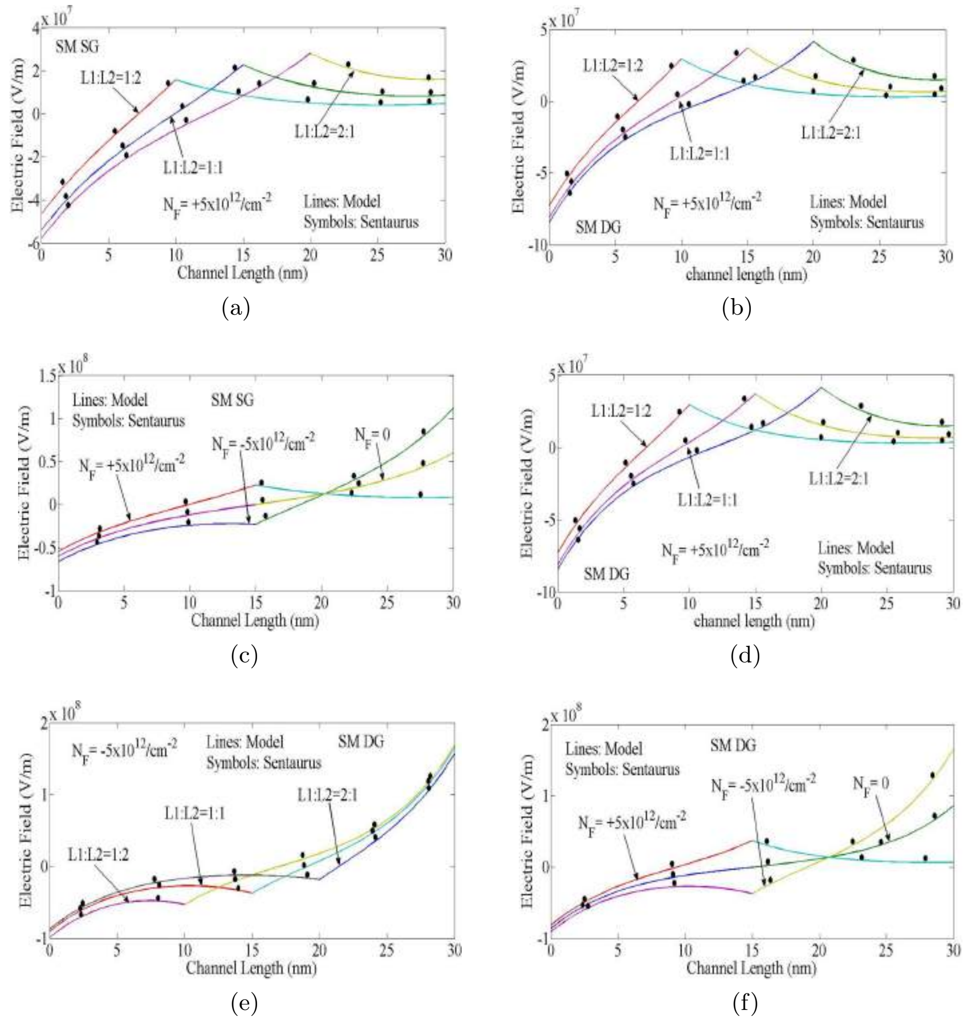

Figure 3.14: (a)- to -(f) Analysis of Electric Field variation along the channel length for interface charge variations for both SG and DG MOSFET. Parameters used $\phi_M = 4.6\ eV, N_A = 1 \times 10^{16}\ cm^3, t_{Si} = 10\ nm, L = 30\ nm, t_{ox} = 2\ nm, V_{DS} = 0\ V$ and $V_{GS} = 0.1\ V$.

The variation of the electric field distribution along the channel for different gate

length ratios has been shown in Fig. 3.14 considering both +ve and -ve interface trapped charges for SG and DG devices. It is observed that as the length of the damaged region i.e. L_2 decreases, the peak of the electric field shifted towards the drain side. By comparing between positive and negative interface charge cases, the device having positive interface charge will give maximum electric field peak as compared to $N_F = 0$ and N_F negative cases. So, positive interface charge case will cause higher short channel effect on the device than its negative charge counterparts due to the high electric field.

From the Fig. 3.14 (c) and (f), the inflection point of the electric field lies at the interface of the damaged and undamaged regions. The device having positive interface charge will give maximum electric field peak as compared to $N_F = 0$ and N_F negative cases. So, positive interface charge case will cause higher short channel effects on the device than its negative charge counterparts due to the high electric field. However, from the observation a lower electric field in case of DG from SG is found.

Table 3.4: Effect of different Structural Engineering on various performance metrics

Structures	Observations
Strain in channel	Drop in V_{th} Improved g_m Higher carrier mobility V_{th} roll-off
Dual Insulator (DI)	Lower leakage (I_{off}) Improved e.field
UD-DG	Higher on current (Ion) Improved g_m
SH & DH	near ideal SS Improvement in e-mobility Lower leakage (I_{off})
TM-SH & TM-DH	Higher on current (I_{on}) Higher peak g_m Lower DIBL
Increasing the ratio ($L1/L2$)	DIBL & HCE effects are controlled Less shift of V_{th}

The table 3.4 shows the comparison of performance metrics for different structures studied in this chapter.

3.5 Summary

This chapter showed the SCEs in search of MOSFETs at the nanoscale with better performance. In this era of Nanotechnology, the non-classical MOSFETs behavior are investigated on single and double gate devices. As shown in device background the DG-MOSFET was proposed in three decades ago, still an enormous amount of unexplored effects. The effect of strain on the channel, various structural approach (Channel, high-k as gate stack and metal gate work function Engineering), +ve and -ve interface trapped charges are investigated.

The following technical topics and contributions are presented in this chapter:

- *Study on SCEs on SG-s-SOI MOSFET through Analytical Modeling (Section 3.1)*

  To meet high performance (HP) and low power (LP) circuit requirements, increased channel mobility is required to boost the transistor drive current and/or reduce V_{DD} for lower power dissipation without performance penalty. Strain Engineering on the SOI platform provides solutions for technology nodes of 32 nm and beyond. A study on the performance of the 2-D analytical model of the single layer fully depleted s-SOI MOSFET is described with an investigation of 1) the surface potential; 2) the Threshold voltage of the device. The analysis is done for understanding of the SCEs and sub-threshold performance in Nanoelectronics application. Numerical simulation verifies the model. There is a significant drop in V_{th} with increasing strain and decreasing channel length. The rise in equivalent Ge content, enhances the performance of s-SOI MOSFETs in terms of improved g_m and speed because of an increase in the carrier mobility. However, as demonstrated by our results, there are undesirable side effects with increasing equivalent Ge content such as a roll-off in V_{th}, which may affect the device characteristics and performance significantly.

- *Various Structural Engineering on DG-MOSFET (Section 3.2)*

  A comparative study on the performance of DG-MOSFET with different channel and gate engineering have done with five structures and analyzed by keeping constant channel length. The short channel parameters like threshold voltage (V_{th}), transconductance (g_m), Electric Field and Surface Potential are studied and compared between FD-DG, UD-DG, GC-DG, Dl-DG, and GS-DG MOSFET structures. The DI configuration has demonstrated momentous improvements in terms of I_{off}, surface potential, and the E-field of the device.The UD-DG exhibits highest on current, transconductance, but it experiences subthreshold leakage issue. On the other hand, GC and GS architectures predict overall reasonable performances in all respect. This work will extensively provide a device that gives rise to a high performance in circuit application.

- *Implementation of LAC with TM in GS-DG MOSFET (Section 3.3)*

  A comparative performance values of six different structures GS-DG, GS-DG-SH, GS-DG-DH, GS-DG-TM, GS-DG-TM-SH and GS-DG-TM-DH MOSFETs have been proposed and analyzed keeping channel length constant. The short channel parameters like subthreshold swing (SS), transconductance (g_m), electric field, leakage current (I_{off}), electron mobility (μ_n) and $DIBL$ are studied. The GS Engineering along with the halo implantation i.e. GS-DG-SH and GS-DG-DH configurations have demonstrated significant improvements in the device characteristics such as SS value, electron mobility, and leakage current. On the other hand by applying gate engineering with halo implantation i.e. GS-DG-TM-SH and GS-DG-TM-DH exhibits a higher value of drain current, the peak g_m and a lower value of $DIBL$. This work extensively provides the device structures that may be applicable for high-speed switching and LP application.

- *Analytical Modeling of DG-MOSFET with Trapped Charges (Section 3.4)*

  This work focuses on the physics and modeling of nanoscale UTB single and double gate MOSFETs. The surface potential and threshold voltage modeling is proposed by parabolic potential approximation by solving the 2-D Poisson's equation. The developed model includes the degradation due to the hot carrier effects like the effect of both +ve and -ve interface charges. Based on the model, the interdependence of the device parameters, such as the silicon film thickness (t_{Si}), oxide thickness (t_{ox}), channel length (L) are investigated. Due to the additional gate introduction in DG device, there is more control over the channel region and that will be the important factor for the suppression of HCE and $DIBL$. The device performance is going to deteriorate in the presence of the interface trap charges in the oxide. The deterioration in the V_{th} may be improved by increasing the length of $L1$ i.e. decreasing the damaged region. The $DIBL$ and HCE can be controlled effectively by increasing the gate length ratio ($L1/L2$), which can be achieved by proper fabrication methodologies.

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List of Contribution

1. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Investigation of dimension effects of FD-S-SOI MOSFET in nanoscale," in *Proceedings of IEEE* 1st *International Conference on Emerging Technology Trends in Electronics, Communication and Networking*, Surat, Gujarat, India, Dec., 2012, pp. 1-4.

2. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Effect of channel & gate Engineering on Double Gate (DG) MOSFET-A comparative study," in *Proceedings of IEEE International Conference on Emerging Electronics*, IIT, Bombay, India, Dec. 2012, pp. 1-3.

3. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Investigation of Prefabrication Models of Double Gate MOSFETs in Nanoscale for High Performance Circuit Application," *Nano Trends: A Journal of Nanotechnology and Its Applications*, vol. 13, pp. 40-44, Oct. 2012.

4. K. P. Pradhan, P. K. Agarwal, P. K. Sahu, and **S. K. Mohapatra**, "Role of high-k materials in Nanoscale TM-DG MOSFET: A simulation study," in 1st *National Conference on Recent Developments in Electronics*, University of Delhi, South Campus, New Delhi, India, Jan. 2013, pp. 1-3.

5. K. P. Pradhan, **S. K. Mohapatra**, P. K. Agarwal, P. K. Sahu, D. K. Behera, and J. Mishra, "Symmetric DG-MOSFET with gate and channel engineering: A 2-D simulation study," *Microelectronics and Solid State Electronics*, vol. 2, no. 1, pp. 1-9, Feb. 2013.

6. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Some Device Design Considerations to Enhance the Performance of DG-MOSFETs," *Transactions on Electrical And Electronic Materials*, vol. 14, no. 6, pp. 291-294, Dec. 2013.

7. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "A new nanoscale DG MOSFET design with enhanced performance a comparative study," in *Signal Processing and Information Technology, Ser. Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering, V. Das and P. Elkafrawy, Eds. Springer International Publishing*, 2014, vol. 117, pp. 76-81.

8. P. K. Sahu, K. P. Pradhan, and **S. K. Mohapatra**, "A Study on SCEs of FD-S-SOI MOSFET in Nanoscale," *Universal Journal of Electrical and Electronic Engineering*, vol. 2, no. 1, pp. 37-43, 2014.

9. M. R. Kumar, P. K. Agarwal, G. S. Pati, K. P. Pradhan, **S. K. Mohapatra**, and P. K. Sahu, "Modeling of Nanoscale Double-Gate MOSFET and Its Physical Analysis," *International Journal of Scientific & Engineering Research*, vol. 5, no. 5, pp. 11-16, May. 2014.

10. **S. K. Mohapatra**, K. P. Pradhan, G. S. Pati, and P. K. Sahu, "Relative appraisal of Ultra-Thin Body MOSFETs: An analytical modelling including hot carrier induced degradation," *Informacije Midem-Journal of Microelectronics Electronic Components and Materials*, vol. 45, no. 1, pp. 57-65, Jan. 2015.

Chapter 4

A Perspective of the Nanoscale DG-MOSFET: Performance Appraisal

Nowadays SOI technology is becoming a contender for low-power system-on-a-chip (SoC), including microwave applications. So, an investigation of the impact of device options on the analog and RF performance of SOI MOSFETs is needed. As the semiconductor industries migrate towards multi-gate technology with different device engineering for the enhancement of performance, a systematic estimation of analog and RF performance measure is presented here for nanoscale DG-MOSFET under study.

4.1 Investigation of Various High-k Dielectric on DG-MOSFET

Nowadays, high-k dielectrics have been investigated as an alternative to Silicon dioxide (SiO_2) based gate dielectric for nanoscale semiconductor devices. The high-k metal gate (HKMG) DG-MOSFET is considered by varying the dielectric material as oxide layers. From the two different types of structural models first model is a single oxide layer and the second one with double oxide layer or gate stack(interfacial oxide + high-k layer) with lateral spacers covering source and drain regions. The structure has been calibrated to meet the requirement of international technology roadmap for semiconductors (ITRS) [7] for 45 nm node. The proposed structure considers the high-k

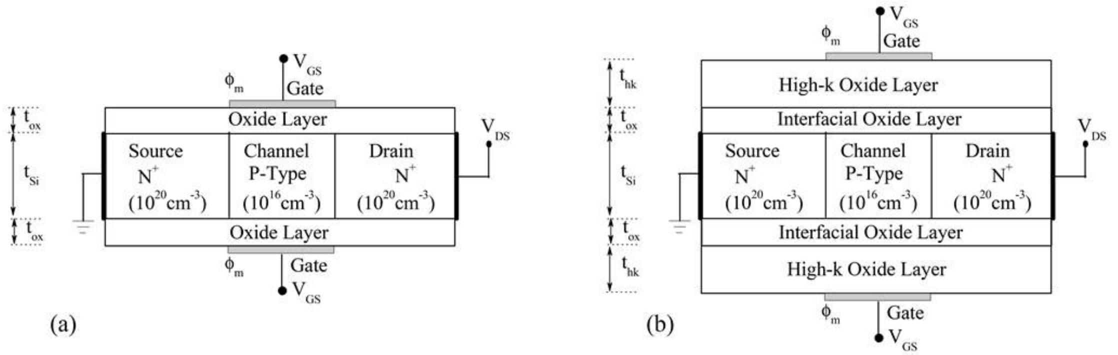


Figure 4.1: Schematic cross sectional structures of n-channel DG-MOSFET with different high-k device cases having $L_g = 40\,nm - 20\,nm$, $t_{Si} = 10$ nm and $EOT = 1.1\,nm$. (a) Device cases for D1, D2, D3 and D4 (b) Device cases for D5, D6 and D7.

dielectrics as Si_3N_4, HfO_2 and Ta_2O_5 [74,105,106]. Different device structural cases are maintained with electrical oxide thickness (EOT) as 1.1 nm as shown in Table 4.1. The schematic cross sectional view of a planar n-channel DG-MOSFET is shown in Figure 4.1. In all the cases the gate work function is tuned between $4.5\,eV - 4.7\,eV$ to obtain the threshold voltage (V_{th}) of $0.2\,V$ at drain to source voltage V_{DS} of $0.1\,V$.

Table 4.1: Structural device cases considered in study

Device	Interfacial layer		High-k Layer		EOT (nm)
	T_{ox} (nm)	ϵ_{ox}	T_{hk} (nm)	k	
D1	1.1	3.9	–	–	
D2	2.1	7.5	–	–	
D3	6.8	24	–	–	
D4	8.5	30	–	–	1.1
D5	0.6	3.9	0.96	7.5	
D6	0.6	3.9	3.08	24	
D7	0.6	3.9	3.85	30	

4.1.1 Impact on SCEs

The SCEs like $DIBL$ and SS for different configurations are tabulated in Table 4.2. By comparing those values, it is clear that, with increasing high-k dielectric permittivity for

Table 4.2: Calculated DIBL and SS for GS-DG

Device	DIBL (mV/V)	$SS(mV/decade)$	
		$V_{DS} = 0.1\,V$	$V_{DS} = 0.5\,V$
D1	20.71	62.29	62.31
D2	21.12	62.37	62.47
D3	37.24	65.72	65.81
D4	49.88	67.86	68.03
D5	19.69	61.21	61.32
D6	20.28	62.19	62.56
D7	21.65	62.67	62.76

the single oxide layer, SS value has increased and reached a maximum 68.03 $mV/decade$ in case of device D4. However in GS configurations with an increase in dielectric constant (k) shows near ideal values of SS. A steep sub-threshold slope (SS) is an important measure of the turn off characteristic of the device [87]. It is observed from Table 4.2 that for single oxide layer configuration, the $DIBL$ value increases with increasing dielectric permittivity and attains a maximum value at $k = 30$, whereas the same decreases for double oxide layer configurations. It is observed that the device D5 is considered to offer better immunity to SCEs.

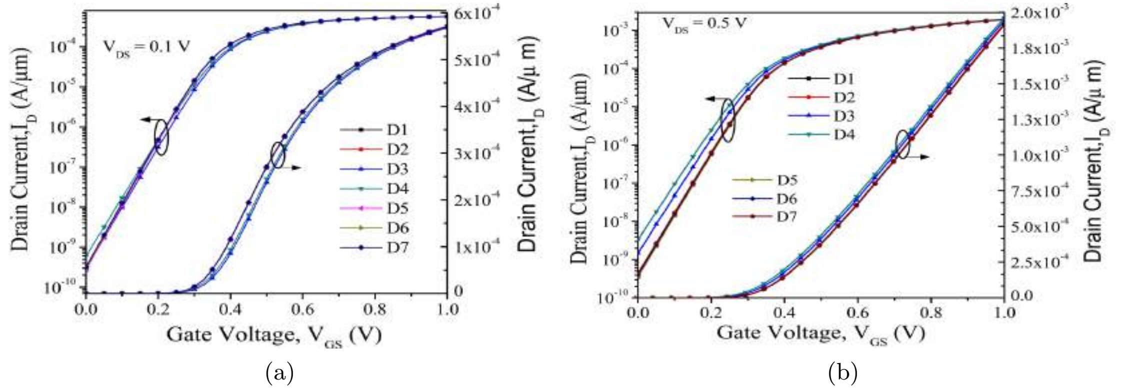


Figure 4.2: Drain current (I_D) versus gate to source voltage (V_{GS}) for different cases (a) with $V_{DS} = 0.1\,V$ and (b) with $V_{DS} = 0.5\,V$.

The $I_D - V_{GS}$ transfer characteristics both in linear and log scales have been shown in Figure 4.2 for different configurations. The V_{th} is maintained a constant value for all the device cases at $V_{DS} = 0.1V$ as a consequence of the leakage current is quite constant. One can notice, leakage current (I_{off}) is varying in between $10^{-9}\,A/\mu m$ and $10^{-10}\,A/\mu m$ for all cases. However, with increasing high-k dielectric permittivity in single oxide layer configuration, the on current as well as leakage current increases due to the fringing field effect. In the device cases of high-k with interfacial oxide (SiO_2) layer, the gate leakage current reduces. The capacitive coupling due to gate increases that decrease the leakage current [74]. The CMOS standby power is affected by the subthreshold current or leakage current.

It is observed that devices that have single oxide layer gate dielectric Si_3N_4 i.e. D2 and devices with gate stack i.e. D5, the DIBL is improved by 6.77% and SS value is

decreased by 1.85%.

After the study on the scalability of the devices, the Analog & RF figures of merit (FoMs) (important for circuit applications) which are investigated in the next subsection for the same device cases.

4.1.2 Impact on Analog & RF FoMs

The g_m and TGF parameters are defined and calculated by 4.1, 4.2. TGF demonstrates the effective use of the current to achieve a desired value of transconductance. The high value of TGF is advantageous to realize analog circuits that are operating at low supply voltage.

$$g_m = \partial I_D / \partial V_{GS} \tag{4.1}$$

$$TGF = g_m / I_D \tag{4.2}$$

The variations of the transconductance and transconductance generation factor with

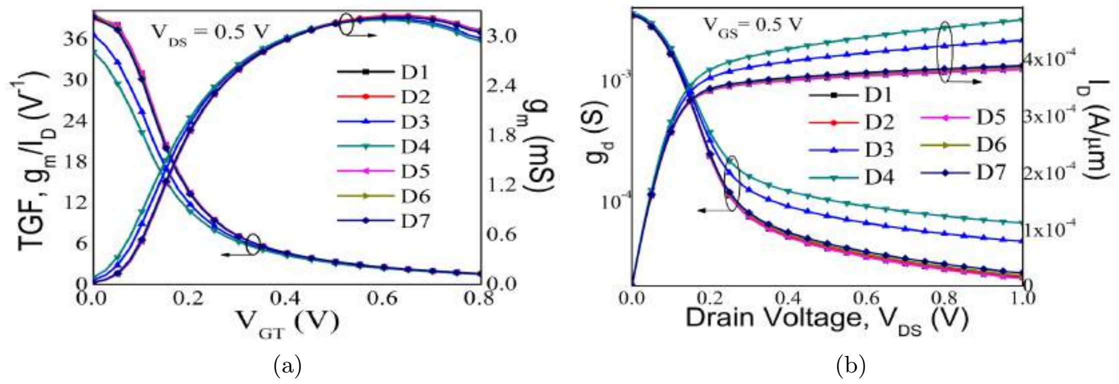


Figure 4.3: (a)Trans-conductance generation factor (TGF) and transconductance (g_m) as a function of gate over drive voltage (V_{GT}) for $V_{DS} = 0.5\,V$, (b)Output conductance (g_d) and drain current (I_D) with respect to drain to source voltage (V_{DS}) for $V_{GS} = 0.5V$.

V_{GT} for $0.5\,V$ are shown in Fig. 4.3 (a) for the devices. It is clear that the double layer structures with high dielectric materials exhibits higher TGF as compared to single layer structures. In single layer structures, as the dielectric permittivity increases the g_m/I_D ratio decreases and it becomes worst at $k = 30$. Higher TGF is not good for high linearity microwave systems as lower TGF is not a drawback since the power consumption in the subthreshold region is very less. Drain current (I_D) and output conductance (g_d) against drain to source voltage (V_{DS}) for different cases are presented in Fig. 4.3 (b) . The output conductance g_d is calculated as in Eq. 4.3.

$$g_d = \partial I_D / \partial V_{DS} \tag{4.3}$$

The drain current is increasing with increase in high-k dielectric permittivity for single layer configurations which in turn makes; the g_d high for these configurations. CMOS Analog circuits require transistors with low output conductance (g_d) to achieve high gain. High g_d means, low output resistance which resulting an increase in I_D with V_{DS} in saturation regime. The components are associated with this increase, namely channel length modulation (CLM) and DIBL. The maximum value of $g_m, g_d, V_{EA}, A_V, TGF$ were

Table 4.3: Analog performance of GS-DG devices for $V_{DS} = 0.5\,V$

Device	Trans-conductance,	Output Conductance,	Early Voltage,	Gain,	TGF
	g_m (S)	g_d (S)	V_{EA} (V)	A_V (dB)	(V^{-1})
D1	3.07×10^{-3}	2.33×10^{-5}	16.304	42.402	39.09
D2	3.06×10^{-3}	2.40×10^{-5}	15.954	42.105	38.95
D3	2.98×10^{-3}	4.69×10^{-5}	9.205	36.077	36.65
D4	2.95×10^{-3}	6.61×10^{-5}	7.069	32.984	34.14
D5	3.17×10^{-3}	2.27×10^{-5}	16.897	43.436	39.58
D6	3.05×10^{-3}	2.45×10^{-5}	15.698	41.921	39.43
D7	3.05×10^{-3}	2.57×10^{-5}	15.065	41.489	39.22

tabulated in Table 4.3. By comparing all the extracted parameters in Table 4.3, the device with high-k gate dielectric as Si_3N_4 i.e. device D5 shows a better result in terms of gain, V_{EA} and TGF.

The important high frequency or RF circuit parameter includes cut-off frequency (f_T), transconductance frequency product (TFP), gain frequency product (GFP) and gain transconductance frequency product ($GTFP$). The intrinsic capacitances (gate to source capacitance, C_{gs} and gate to drain capacitance, C_{gd}) as a function of V_{GT} shown in Fig. 4.4 (a). The C_{gs} and C_{gd} values of the device increase with k. This is caused by the increased fringing field density in the single layer high-k devices. However, GS configurations demonstrate better values for intrinsic capacitances. It is observed that both the C_{gs} and C_{gd} starts increasing as V_{GT} increases until saturation. After saturation, both the values become constant, as expected, as the additional V_{DS} can not affect the junction. Cut-off frequency f_T is one of the most important parameters for evaluating the RF performance of the device. Generally, f_T is the frequency when the current gain is unity. The f_T can be defined as Eq. 4.4 [79].

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1 + 2\frac{C_{gd}}{C_{gs}}}} \approx \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{4.4}$$

It can be seen from the Fig. 4.4 (b) that f_T decreases as k increases in case of single layer

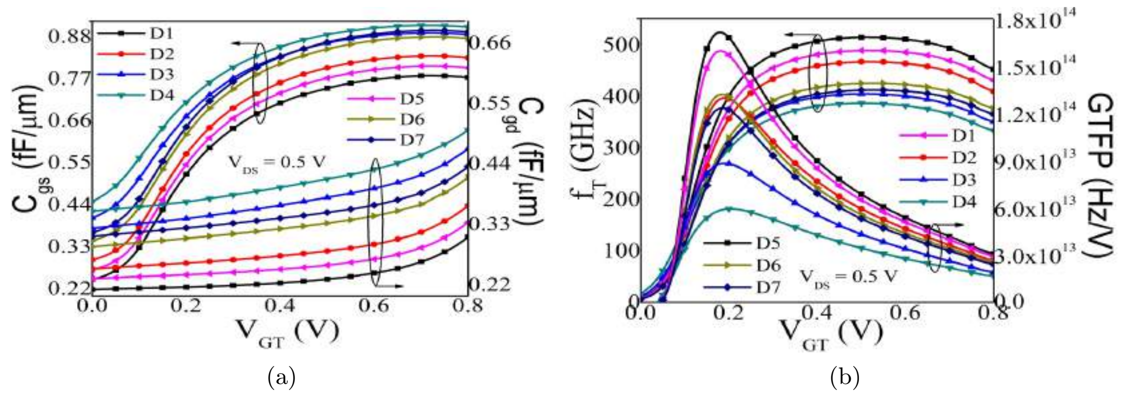


Figure 4.4: (a) Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) (b) Cut off frequency (f_T) and gain trans-conductance frequency product ($GTFP$) as a function of gate over drive voltage (V_{GT}) for $V_{DS} = 0.5\,V$

structures. However, it displays required values for GS configurations. The difference in f_T is mainly due to the difference in g_m, as observed in Fig. 4.3 (a), and partially due to the higher value of total capacitance ($C_{gs} + C_{gd}$), as observed in Figure 4.4 (a). The peak point of f_T corresponds to the point between the minimum gate-drain/source capacitance and the peak of transconductance. It is also clear from Fig. 4.4 (b) that f_T is highest for the device D5 reflecting superior gate controllability and hence higher transconductance and lower parasitic gate capacitances as compared to other devices considered in our study. A unique figure of merit for analog/RF performances is the gain transconductance frequency product ($GTFP$) as given in Eq. 4.5 is also plotted in Fig. 4.4 (b) by both the switching speed and the intrinsic gain. The peak value of GTFP is achieved at $V_{GS} = 0.375\,V$ for all the configurations, where the level of drain current (I_D) is quite low, i.e. $I_D \approx 10^{-5} A\,\mu m$. It is interesting that the voltage corresponds to V_{GS} just above $175\,mV$ of the threshold voltage of the device. This allows the circuit designer to determine the best region of operation by trading off for gain, transconductance and speed. Here also device D5 shows higher $GTFP$ as compared to other configurations. This is because of higher f_T, g_m and lowÂăg_d value of D5 device.

$$GTFP = (g_m/g_d) \times (g_m/I_D) \times f_T = A_V \times TFP \tag{4.5}$$

The maximum value of RF FoMs like $f_T, GFP, TFPandGTFP$ are calculated. From the tabulated values in Table 4.4 for different device cases, the configuration having Si_3N_4 gate oxide as gate stack i.e. D5 shows optimum results than its counterparts in terms of f_T, GFP, TFP and $GTFP$.

Table 4.4: RF performance of different devices for $V_{DS} = 0.5\,V$

Device	C_{gs} (fF)	C_{gd} (fF)	f_T (GHz)	GFP (GHz)	TFP (GHz/V)	$GTFP$ (GHz/V)
D1	0.798	0.334	489.18	2.02×10^4	5.54×10^3	1.60×10^5
D2	0.825	0.365	467.63	1.91×10^4	5.21×10^3	1.28×10^5
D3	0.885	0.467	404.92	1.42×10^4	3.89×10^3	0.87×10^5
D4	0.905	0.502	386.65	1.24×10^4	3.43×10^3	0.58×10^5
D5	0.772	0.308	515.55	2.12×10^4	5.93×10^3	1.72×10^5
D6	0.874	0.416	425.8	1.73×10^4	4.62×10^3	1.32×10^5
D7	0.892	0.436	412.89	1.67×10^4	4.41×10^3	1.23×10^5

4.2 Impact of Channel Length on GS-DG MOSFET

A planar DG SOI n-channel transistor is considered for this study. Four different channel lengths ($L = 60\,nm, 50\,nm, 40\,nm$, and $30\,nm$) are chosen for the device to analyze the device performance. The schematic simulated structure is shown in Fig. 4.5, where the silicon channel is surrounded above and below by two layers of oxide, SiO_2 and HfO_2. To achieve a constant V_{th}, the work function of the metal gate is tuned in between $4.6\,eV$ to $4.7\,eV$ while varying the channel length of the device. We assumed an undoped channel with heavily doped source, drain (n-type $10^{20}\,cm^{-3}$). For a better comparison of analog/RF FoMs, the V_{th} is maintained at a constant value $0.2\,V$ while varying the

metal gate work function at $V_{DS} = 0.1\,V$.

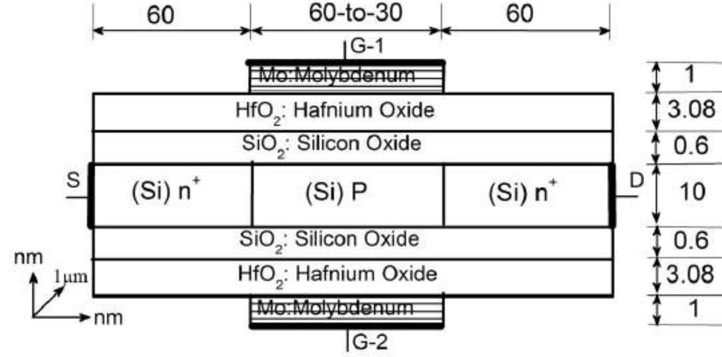


Figure 4.5: Schematic structure of GS-DG-MOSFET with variation of Channel Length

4.2.1 DC Performance

The $I_D - V_{GS}$ transfer characteristics both in linear and log scales have been shown in Fig. 4.6 (a) for different configurations at $V_{DS} = 0.5\,V$. The leakage current (I_{off}) is quite constant for three different channel length except $L = 30\,nm$. In the short channel device, the I_{off} increases due to random motion of charge carriers. As channel length decreases, it gives rise to high drain current because of the relation $I_D \propto 1/L$. However, from the log scale, the leakage current is also prominent for lower channel lengths.

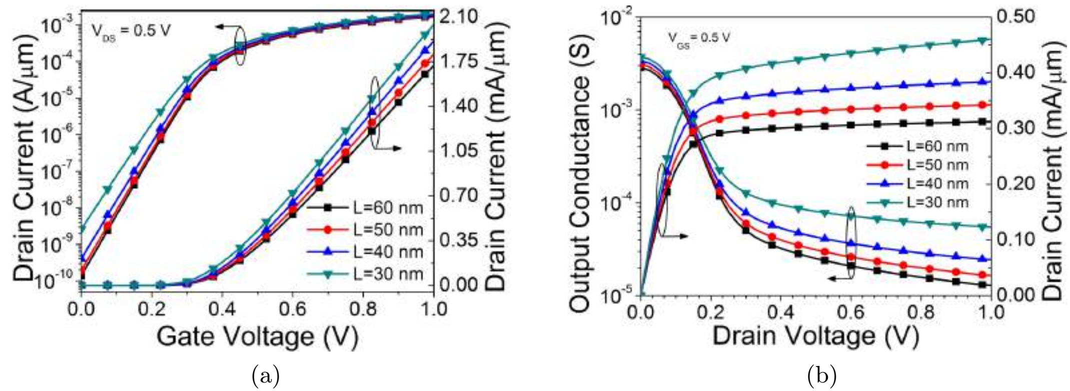


Figure 4.6: (a) Drain current (I_D) in both linear and log scale as a function of gate to source voltage (V_{GS}) (b) Output conductance (g_d) and drain current (I_D) with respect to drain to source voltage (V_{DS}) for different channel lengths.

Drain current (I_D) and output conductance (g_d) against drain to source voltage (V_{DS}) for different cases at $V_{GS} = 0.5\,V$ are presented in Fig. 4.6 (b). The drain current is increasing with decrease in channel length which in turn makes; the g_d high for lower L devices as $g_d = \Delta I_D / \Delta V_{DS}$. As we know from the literature that gain and early voltage are inversely proportional to output conductance, so the device having lower L gives higher g_d which comprises lower gain and early voltage of the device.

Transconductance generation factor ($TGF = g_m/I_D$) and transconductance (g_m) as a function of V_{GS} are presented in Fig. 4.7 (a). It is clear that as the channel length decreases the g_m value is increasing because of high drain current. As shown in the figure, g_m/I_D is maximized towards the subthreshold region of device operation. From

the Fig. 4.7 (a), it is clear that the structure has channel length 60 nm shows higher g_m/I_D ratio as compared to others and it decreases as channel length decreases. Fig. 4.7 (b) shows the variation of the early voltage (V_{EA}) and intrinsic gain (A_V) as a function of V_{GS} for different channel lengths. For better analog performance, the V_{EA} and A_V should be as high as possible. An enormous improvement is observed in V_{EA} for channel length $L = 60\,nm$ as compared to others.

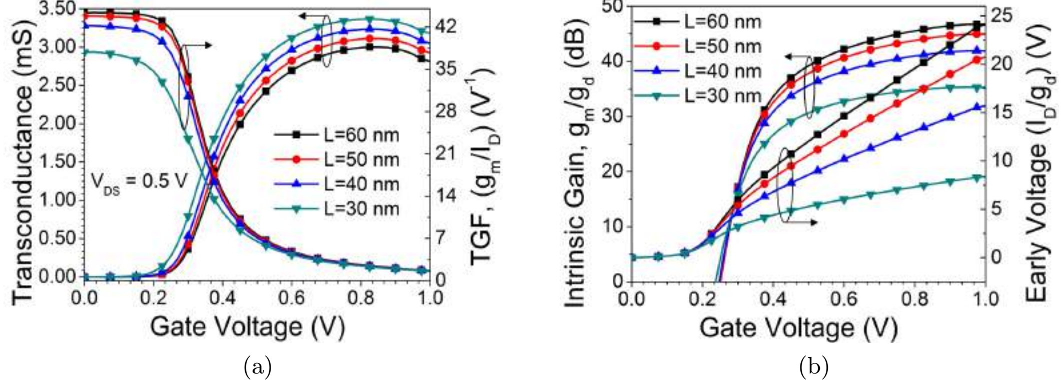


Figure 4.7: (a) Transconductance generation factor (TGF) and transconductance (g_m) (b) Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of (V_{GS}) for different channel lengths.

The intrinsic gain ($A_V = g_m/g_d$) is a valuable figure of merit for operational transconductance amplifier. From the Fig. 4.7 (b), the intrinsic gain of the device having channel length 60 nm gives the highest gain from others, and it decreases as the channel length decreases. Both the extracted values of SS and calculated values of $DIBL$ for different channel lengths are tabulated in Table 4.5. It is clear that the SS value increases as channel length decrease, and it is high for channel length 30 nm. Similarly, the DIBL value also increases as channel length decreases, and it gives a maximum value for a channel length of 30 nm. These two parameters are crucial for short channel effects, which should be minimized. The maximum values for $g_m, g_d, V_{EA}, A_V, TGF$ are also tabulated in Table 4.5. I_D increases for lower channel length devices which consequently increases g_m values for devices having a lower value of L. However, because of high g_d, the V_{EA}, and A_V becomes lower as L decreases. Coming from $L = 60\,nm$ to $30\,nm$, the $DIBL$ and SS values are more prominent for lower channel length devices and also the TGF and Gain are decreases as L decreases.

Table 4.5: Electrostatic Performances for different values of channel lengths at $V_{DS} = 0.5\,V$

Channel Length, (nm)	$DIBL$, (mV/V)	SS, $(mV/decade)$	g_m (mS)	g_d (μS)	V_{EA} (V)	A_V (dB)	TGF, (V^{-1})
L=60	20.71	62.31	2.81	12.94	24.13	46.74	43.63
L=50	21.12	63.12	2.93	16.57	20.73	44.96	42.84
L=40	37.24	65.95	3.05	24.53	15.78	41.92	40.63
L=30	49.88	68.35	3.18	54.84	8.49	35.45	34.669

4.2.2 Analog and RF Performance

Fig. 4.8 (a) shows the intrinsic capacitance parameters increase swiftly in the superthreshold region. This is because of the increase in the fringing field lines emanating from the gate edges. The device having channel length 60 nm shows higher values of intrinsic capacitances (both C_{gs} and C_{gd}) and it decreases as channel length decreases.

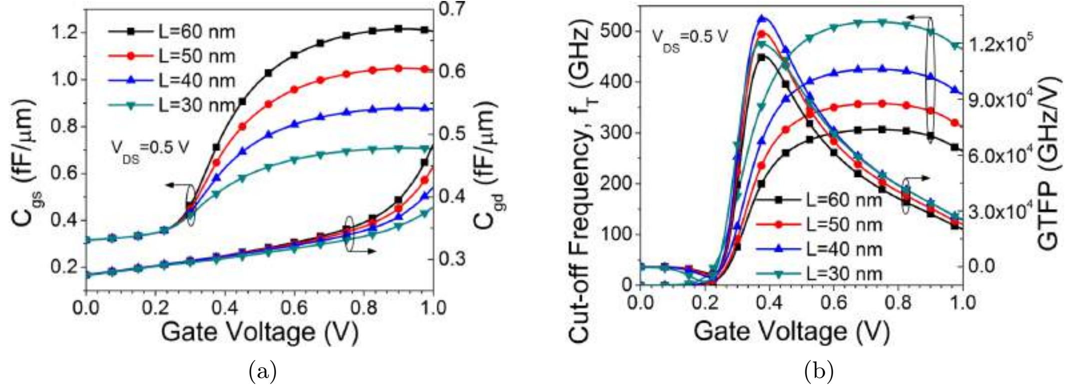


Figure 4.8: (a) Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) (b) Cut off frequency (f_T) and gain trans-conductance frequency product ($GTFP$) as a function of (V_{GS}) for different channel lengths.

From Fig. 4.8 (b), the variations of cut-off frequency ($f_T = g_m/2\pi(C_{gs} + C_{gd})$) and gain transconductance frequency product ($GTFP = A_V \times TGF \times f_T$) can be observed for different values of channel lengths. Here, the value of f_T obtained for the device having low channel length is higher and it gradually decreases as the channel length decreases. f_T is inversely proportional to the intrinsic capacitances (C_{gs} and C_{gd}). So, f_T value is low due to high capacitance values for higher channel length devices. It is interesting to see that the device having channel length $L = 40\,nm$ shows a higher $GTFP$ value as a comparison to others. This is due to the reduction in peak electric field, lower output conductance of the device having channel length 40 nm. The $GTFP$ value is very low for $L = 30\,nm$.

Table 4.6: RF performances for different values of channel lengths

Channel Length (nm)	C_{gs} (fF)	C_{gd} (fF)	f_T (GHz)	GFP (GHz) $\times10^3$	$TFP(GHz/V)$ $\times10^3$	$GTFP$ (GHz/V) $\times10^5$
L=60	1.207	0.484	306.78	4.57	3.69	1.12
L=50	1.041	0.449	358	5.27	4.22	1.25
L=40	0.874	0.416	425.8	6.12	4.76	1.33
L=30	0.706	0.384	518.79	7.02	5.03	1.2

All the extracted values for analog/RF FoMs are plotted in Table 4.6 for different values of channel lengths. While the gate length is reduced the RF FoMs like f_T, GFP and TFP are also increased because of high drain current which results in higher g_m values for shorter gate length devices. However, the improvement in $GTFP$, which is a unique and major FoMs, with L downscaling reduces below 40 nm due to short channel

effects. From Table 4.5, the A_V values are obtained around 41.921 dB and 35.458 dB for 40 nm and 30 nm respectively whereas the g_m/I_D shifts lower to 34.669 V^{-1} for 30 nm technology from 40.639 V^{-1} for 40 nm technology. The $GTFP$ is nothing but the product of three parameters i.e., TGF, gain and frequency, so the peak values are more for 40 nm technology as compare to 30 nm technology.

4.3 Impact of Metal Gate Work Function on GS-DG MOSFET

A planar symmetric GS-DG MOSFET has been considered which schematic structure is shown in Fig. 4.1 (b). For a better comparison of analog/RF FoMs, the threshold voltage (V_{th}) is maintained at a constant value of 0.2 V while varying the work function at $V_{DS} = 0.1\,V$. The channel doping (N_A) and source/drain doping (N_D) are changed to maintain the constant V_{th} which is tabulated in Table 4.7. The channel length of the device is fixed at 40nm. The gate stack configuration has been considered with hafnium dioxide (HfO_2) sandwiched over silicon dioxide (SiO_2) layer. The interfacial layer (SiO_2) thickness (t_{ox}) and above this high-k oxide layer (t_{hk}) are fixed at 0.6 nm, 0.5 nm (equivalent thickness of high-k) respectively, so to achieve equivalent oxide thickness (EOT) of 1.1 nm. Here

Table 4.7: Simulated Device Parameters

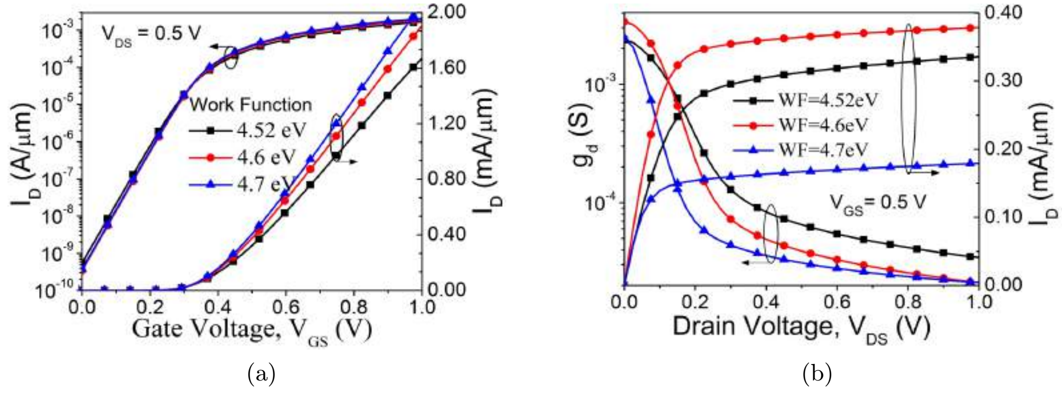
Metal gate work function (ϕ_m) in eV	Channel doping (N_A) in cm^{-3}	Channel doping (N_D) in cm^{-3}
4.52 eV (Ag: Silver)	1.5×10^{18}	1.0×10^{20}
4.6 eV (Mo: Molybdenum)	1.0×10^{16}	1.0×10^{20}
4.7 eV (Au: Gold)	1.0×10^{15}	9.0×10^{21}

the drain bias has been fixed at $V_{DD} = 1.0\,V$ [7]. To study the analog performance the simulation is carried out with drain to source voltage $V_{DS} = 0.5\,V$ (which is half of the supply voltage i.e., $V_{DD}/2$) [129] with a variable gate to source voltage $V_{GS} = 0V to 1.0V$. Threshold voltage (V_{th}) is extracted using constant current ($I_D = 10^{-6} A/\mu m$) definition from the $I_D - V_{GS}$ transfer characteristic at $V_{DS} = 0.1\,V$.

4.3.1 Performance Analysis

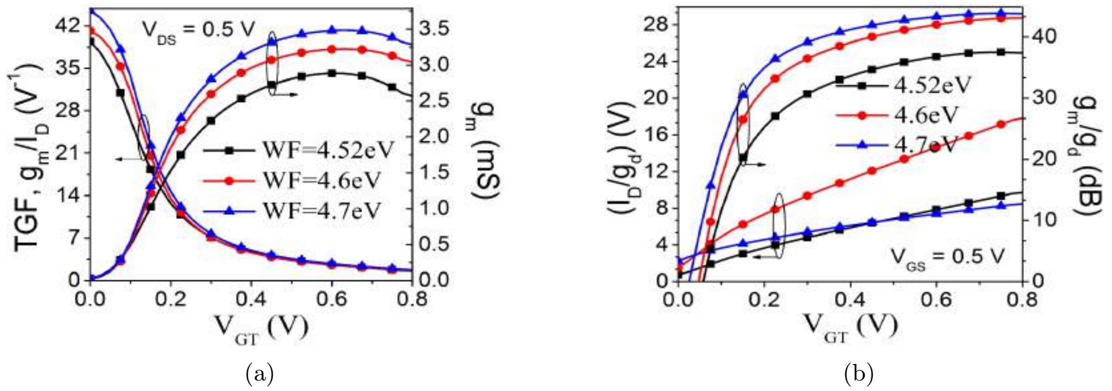
The drain current is dependent on the mobility (μ) of carriers which are controlled by the doping concentrations. Here in the low work function metal gate device the channel doping (N_A) is kept high which results in a lower drain current (I_D) then the device having higher N_A, because the mobility is directly proportional to the current. We found that the drain current increased with the rise in work function.

Both the extracted value of SS and calculated value of $DIBL$ for different work function is tabulated in Table 4.8. From the Fig. 4.9 (a), the on current increases as work function of the device increases and maximum for 4.7 eV. The off current is quite constant for all device cases as Vth is maintained constant. From the Fig. 4.9 (b) output current is maximum for 4.6 eV device case and lowest for 4.7 eV device case.



(a) (b)

Figure 4.9: (a) Drain current (I_D) in both linear and log scale as a function of gate to source voltage (V_{GS}) (b) Output conductance (g_d) and drain current (I_D) with respect to drain to source voltage (V_{DS}) for different work functions.



(a) (b)

Figure 4.10: (a) Transconductance generation factor (TGF) and transconductance (g_m) (b) Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different work functions.

From the analysis, the structure having 4.7 eV shows high drain current. The structure having work function 4.7 eV give rise to higher values of transconductance and TGF when compared with others. Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different work functions are presented in Fig. 4.10 (b). An improvement is observed in V_{EA} for work function 4.6 eV when compared to others. The simulated results for subthreshold slope (SS), maximum value of transconductance ($g_{m(max)}$) and maximum value of output conductance ($g_{d(max)}$) are outlined in Table 4.8. By comparing these values while work function varying from 4.52 eV to 4.6 eV, SS value is decreased by 0.83%, $DIBL$ value is decreased 2.3% and g_d is decreased by 62.73%. In analog/RF figures of merit transconductance (g_m) is increased by 18.75%, transconductance-to-drain-current ratio g_m/I_D is improved by 4.51%, intrinsic gain gm/gd increases by 15.23%, and early voltage V_{EA} is increased by 83.41% while coming from 4.52 eV to 4.6 eV device case. By comparing the device having 4.6 eV provides better values in case of V_{EA}, gain and TGF as compared to 4.52 eV case and nearly equal values with 4.7 eV case.

As shown in Fig. 4.11 (a), in the subthreshold regime, the intrinsic capacitance parameters have small values that increase slowly; however, in the superthreshold region,

Table 4.8: Electrostatic and Analog performances for different values of work function

Work Function (eV)	$DIBL$, (mV/V)	SS, ($mV/decade$)	g_m, (mS)	g_d, (μS)	V_{EA}, (V)	A_V, (dB)	TGF, (V^{-1})
4.52	20.43	62.58	2.56	34.5	9.71	37.42	39.39
4.6	19.96	62.06	3.04	21.2	17.81	43.12	41.17
4.7	21.48	63.23	3.28	21.1	8.46	43.81	41.18

they rise swiftly. It is because of the rise in the fringing field lines emanating from the gate edges. The device having work function 4.7 eV shows high value for C_{gs} and device having 4.52 eV gives high C_{gd} when compared to others. However, in case of 4.6 eV, both the intrinsic capacitance values are least which in turns to high cutoff frequency.

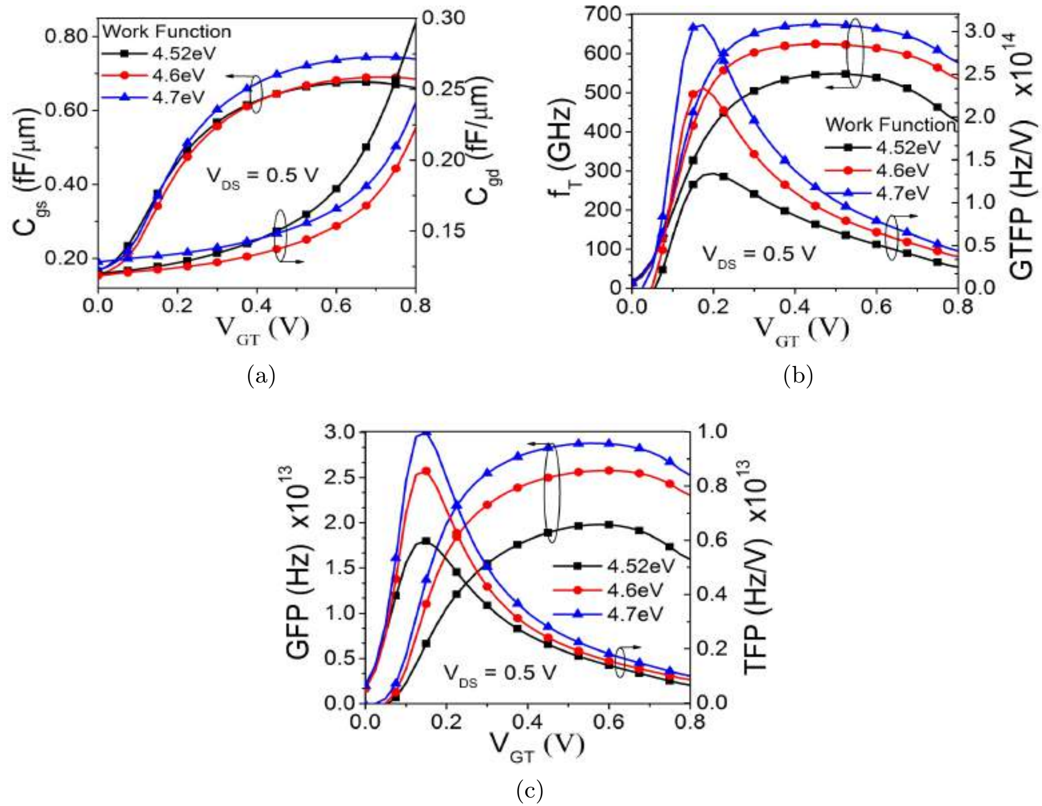


Figure 4.11: (a) Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) (b) Cut off frequency (f_T) and gain trans-conductance frequency product ($GTFP$) (c) Gain frequency product (GFP) and trans-conductance frequency product (TFP) as a function of gate over drive voltage (V_{GT}) for different work functions.

In Fig. 4.11 (b), the value of f_T obtained for the device having high work function i.e. 4.7 eV is higher as compare to its counterparts. This is because, the g_m value is high for work function 4.7 eV and is low for 4.52 eV case. It is interesting to see the Fig 4.11 (b) that as the gate work function increases, the $GTFP$ also increases and it is highest for the device having work function 4.7 eV. This is due to the reduction in peak electric field, lower output conductance of the device having work function 4.7 eV. From the Fig. 4.11 (c), the value of ($GFP = g_m/g_d \times f_T$) increases as work function increases and reaches utmost for the device having work function 4.7 eV. The product of g_m/I_D and

f_T represents a trade-off between power and bandwidth and is utilized in moderate to high-speed designs. It is clear that the device having higher work function gives higher TFP values from others. It is due to the high-frequency values for higher work function devices.

Table 4.9: RF performances for different values of work function

Work Function (eV)	C_{gs}, (fF)	C_{gd}, (fF)	f_T, (GHz)	GFP, (GHz) $\times 10^4$	TFP,(GHz/V) $\times 10^3$	$GTFP$, (GHz/V) $\times 10^5$
4.52	0.673	0.297	547.26	1.98	5.98	1.32
4.6	0.69	0.222	624.47	2.58	8.56	2.34
4.7	0.745	0.24	674.42	2.87	9.98	3.08

These simulated results may be slightly higher than those of the experimental results, since, some considered parasitic parameters may be smaller than those of the real case, such as gate-to-source/drain capacitance, source/drain contact resistance. All the extracted values for analog/RF FoMs are tabulated in Table 4.9. As work function increases from 4.52 eV to 4.6 eV, GFP of the device increases by 30.33%, cut off frequency (f_T) increases by 14.10%, TFP increases by 43.14% and $GTFP$ is increased by 77.27%.

4.4 GS-DG-MOSFET with Miscellaneous Device Design

The transistor density and the rise of performances, due to the methodical downscaling, leads to higher chip functionality and frequencies. Due to close proximity of source and drain, the gate electrode loses the control of the potential distribution and current flow in the channel region, results undesirable effects called short channel effects (SCEs) [78,130]. Various approaches to channel engineering using halo implantation, gate work function engineering, gate stack (high-k gate oxide with interfacial layer SiO_2), multi-gate devices, etc., have been proposed to alleviate the short channel effects. A comparative study is made through various performance metrics between single material (SM) GS-DG, dual material (DM) GS-DG, and dual material single halo (DM-SH) GS-DG MOSFETs. The key idea behind this investigation is to provide a physical explanation for the improved analog and RF performances exhibited by the device.

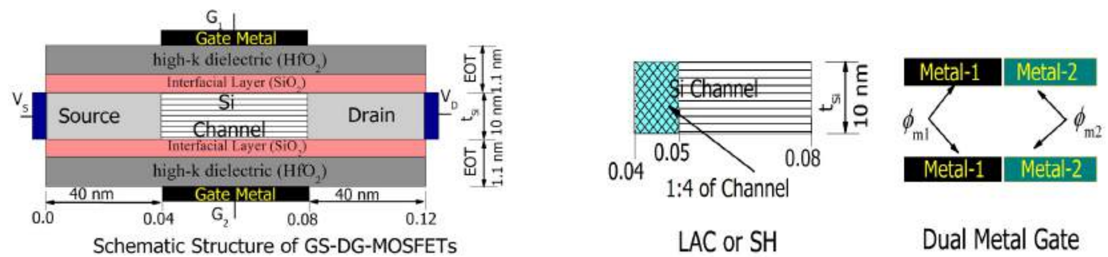


Figure 4.12: Schematic structures of DG-MOSFETs of SM-GS-DG, DM-GS-DG and DM-SH-GS-DG with different device cases named as D1, D2 and D3 respectively.

The schematic of cross-sectional view of the DG-MOSFETs (n-channel) with a channel length (L_g) considering 40 nm Source/Drain length (L_S/L_D). The silicon

thickness (t_{Si}) is about 10 nm and the source drain doping is uniform with N_D density of 10^{20} cm^{-3}. The Equivalent Oxide Thickness (EOT) is about 1.1 nm. The thicknesses of SiO_2 and equivalent HfO_2 are about 1.0 nm, 0.1 nm respectively. The work function for the gate electrode is assumed as 4.77 eV for single material structures and 4.8 eV and 4.6 eV for dual material structures. The channel engineering concept is applied in the structural model with a ratio of 1 : 4 as shown in Fig 4.12. According to channel engineering, the comparative study and the performance evaluation have been done between three different cases of the calibrated model [78] as summarized in Table 4.10. The default value for the z-direction is considered as 1 μm for the simulations.

Table 4.10: Device Structures Considered in study

Device Case	**Name**	N_A **(p-type)** (cm^{-3})	**Channel Engineering (Halo Doping) ratio**	**Gate Metal Work function** (eV)
SM-GS-DG	D1	10^{16}	1(40 nm)	$\phi_{m1} = 4.77$
DM-GS-DG	D2	10^{16}	1(40 nm)	$\phi_{m1} = 4.8$, $\phi_{m2} = 4.6$
DM-SH -GS-DG	D3	10^{18} : 10^{16}	1 : 4(10 nm : 30 nm)	$\phi_{m1} = 4.8$, $\phi_{m2} = 4.6$

4.4.1 Electrostatic Performance

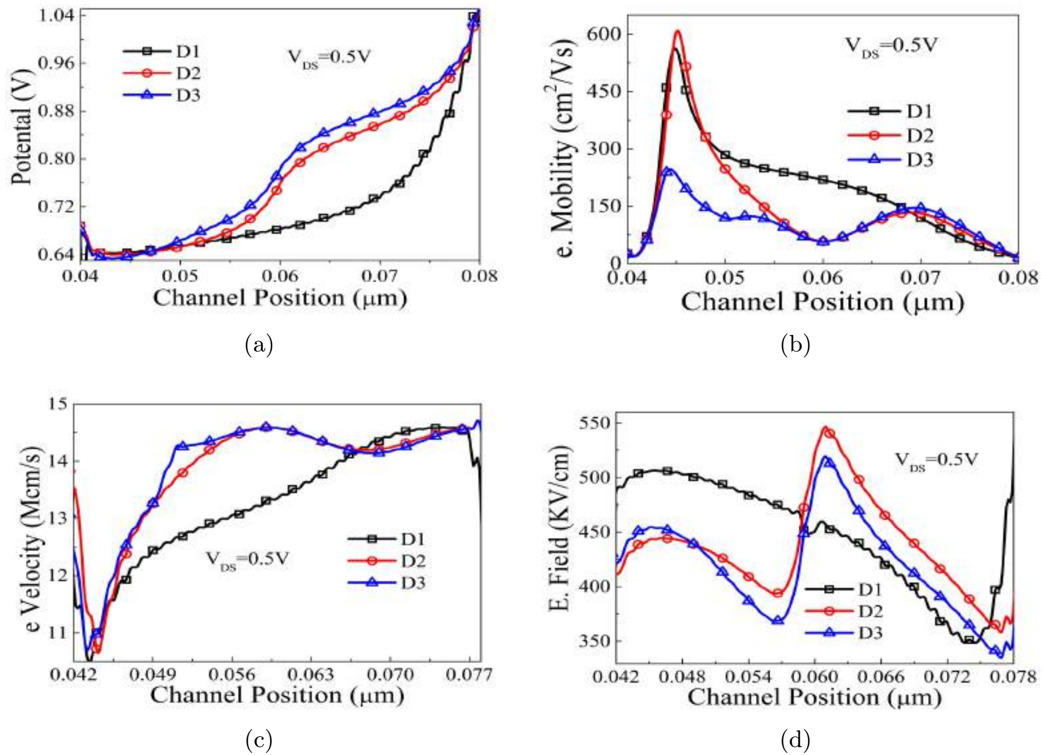


Figure 4.13: Simulated parameters for n-MOSFET along the channel position (from the Source to the Drain, from the left to the right) for the device cases at $V_{DS} = 0.1\,V$ and $0.5\,V$ (a) Surface potential, (b) e-Mobility, (c) e-Velocity, (d) E-Field.

The surface potential, e-mobility, e-velocity and E-field along the channel for D1 to D3 with $V_{DS} = 0.1V$, 0.5 V and $V_{GS} = 0V to 1V$ in step of $0.025V$ are shown in Fig. 4.13. In all figures, the position along the channel (from the Source to the Drain) is plotted in the x-axis direction where 0.06 μm indicates the center of the channel. The difference in

the value of work function of the two gate materials in the DM gate devices results in an additional peak that influences the transport phenomena. Fig 4.13 (a) shows the surface potential of the device. This parameter can be controlled by adjusting the work function of the gate metal and the doping concentration, which consequently leads to control the threshold voltage. The additional peaks of electron mobility and electron velocity near the source side for DM devices impact the carrier transport efficiency, as shown in Fig 4.13 (b) and (c) respectively. In Fig 4.13 (d), the peak value of the electric field near the drain side is somewhat reduced for the DM devices as compared to SM counterpart. Again, the halo effect, in addition to DM i.e. D3 device, shows a small increase in potential due to the abrupt change of doping profile compared with D1. The increase in surface potential, at the abrupt doping profile junction, reduces the electric field resulting in smaller DIBL and HCEs, which are the major effects in the case of the short channel devices. Moreover, the lower potential at the drain side in D3 implies the reduction of drain conductance (g_d), which in turn improves the analog circuit performance of the device. The $I_D - V_{GS}$ transfer characteristics in linear and log scales are shown in Figure

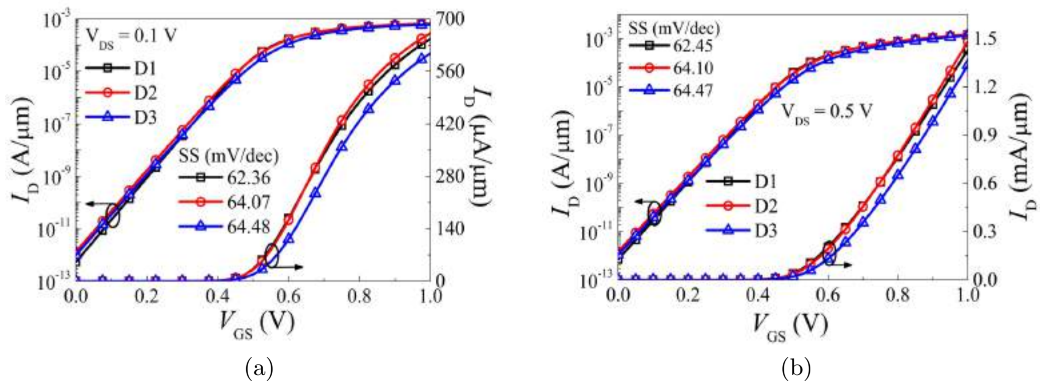


Figure 4.14: Drain current (I_D) of n-MOSFET in both linear and log scale as a function of gate to source voltage (V_{GS}) for (a) $V_{DS} = 0.1\,V$ (b) $V_{DS} = 0.5\,V$.

4.14 for D1, D2 and D3 configurations. V_{th} is maintained to a constant value for all the device cases at $V_{DS} = 0.1\ V$ as a consequence of the leakage current is quite constant. In Figure 4.14 (a), it is interested to note that the leakage current (I_{off}) is varying in between $10^{-11}\ A/\mu m$ and $10^{-13}\ A/\mu m$ for all devices. However, in Figure 4.14 (b), the device D2 gives higher drive current because of the additional peaks in electron mobility and the electron velocity. In the device cases of high-k with interfacial oxide, (SiO_2) layer, the gate leakage current is reduced. The high-k gate dielectric material increases the capacitive coupling, which decreases the leakage current. The CMOS standby power is affected by the subthreshold current. MOSFETs designed for low power consumption and high-speed nano scale digital applications work at the sub-threshold regime. The sub-threshold current affects the dynamic circuits. A steep sub-threshold slope (SS) is required for switching operation. The inset SS values of Figure 4.14 are somewhat higher in case of DM devices i.e. 64 to 65 $mV/decade$, which are acceptable as the ideal value of SS is 60 $mV/decade$. D2 and D3 devices show higher SS which provides larger amounts of drive current in saturation regime, due to an improved carrier transport efficiency.

4.4.2 Analog/RF Performance Metrics

The device described here designed as per 45 nm technology node and beyond the high-k dielectrics (mostly HfO_2) are used in gate stacks to achieve a small equivalent oxide thickness (EOT) with the aim to reduce the gate leakage current, the threshold voltage and supply voltage [7]. However, one of the key issues is the process induced defect that degrades device mobility resulting in poor performance and reliability [113]. So in this simulation, the interface trapped charge density at the semiconductor to insulator interface is set to $4 \times 10^{11}\ cm^{-2}$. The typical concentration of trapped charge density ranges between $10^{10}\ cm^{-2}$ to $10^{11}\ cm^{-2}$ in thin interface layers [108]. The electron and hole surface recombination velocity is defined around $1 \times 10^{4}\ cm/s$. Based on the TCAD simulations of the device the analog and high-frequency performances are discussed through the extracted and calculated data presented in the following graphs and tables.

The variations of the transconductance and transconductance generation factor with V_{GT} for 0.5 V are shown in Fig. 4.15 (a) for the three devices. The g_m and TGF parameters are defined and calculated by Eq. 4.1 and 4.2. It is evident from Fig. 4.15

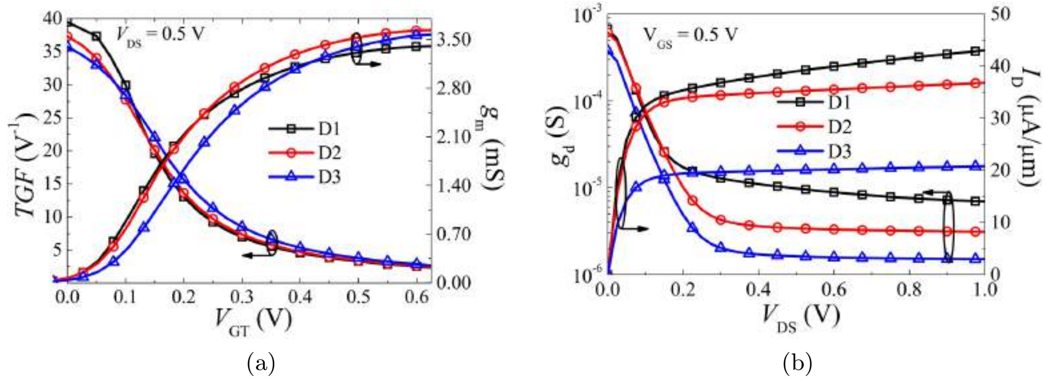


Figure 4.15: (a) Transconductance generation factor (TGF) and Transconductance (g_m) as a function of gate overdrive voltage (V_{GT}) for $V_{DS} = 0.5\ V$ (b) Drain Current (I_D) and Output Transconductance (g_d) as a function of V_{DS} at $V_{GS} = 0.5\ V$

(a) that the g_m is higher in the subthreshold regime for the DM devices than the SM device. However, the device with lateral asymmetric channel (LAC) shows a lower g_m because of the higher doping concentration reduces the surface mobility that consequently reduces the drain current. The ideal value of TGF is limited to $\approx 40V^{-1}$ at minimum SS of 60 $mV/decade$ of the device. The variation of TGF occurs at subthreshold region of operation for the three studied devices. A slight reduction $(10\% - 12\%)$ in the value of TGF can be observed for the DM devices. This reduction is due to the higher value of I_D. However, it will not affect the performances in the subthreshold regime drastically. Because TGF can be termed as the available gain per unit value of the power dissipation and the power dissipation is lower in the subthreshold regime. The drain current and output conductance as a function of V_{DS} for different cases at $V_{GS} = 0.5\,V$ are presented in Fig. 4.15 (b). The output conductance g_d is defined and calculated by Eq. 4.3. The SM structure leads to a higher value of g_d than the DM structures. In a DM device, as

V_{DS} is increased beyond pinch-off, the additional voltage is absorbed under gate metal towards drain end (ϕ_{m2}) rather than under gate metal near source end (ϕ_{m1}). Hence, the channel region under ϕ_{m1} i. e., the source end of the channel is effectively screened from variations in the drain potential. As a result, V_{DS} hardly has any influence on I_D beyond saturation thereby producing a very small value of g_d. Moreover, the width of the drain depletion region becomes less in DM devices resulting in a further reduction in output conductance in such devices as compared to the SM device.

CMOS analog circuits require transistors with low output conductance to achieve high gains. Large g_d means low output resistances which resulting in an increase in I_D with V_{DS} in the saturation regime. The components are associated with this increase, namely channel length modulation (CLM) and DIBL. Moreover, a low g_d induces a higher early voltage of the device as furnished in Eq. 4.6. Fig. 4.15 (b) shows a good control of CLM and DIBL owing to low g_d value for the D3 device.

$$V_{EA} = I_D/g_d \tag{4.6}$$

$$A_V = g_m/g_d = (g_m/I_D) \times V_{EA} \tag{4.7}$$

Fig. 4.16 (a) shows the variation of the Early Voltage (V_{EA}) and intrinsic gain (A_V) as a function of V_{GT} which is calculated and defined by Eq. 4.6 and 4.7 respectively. For better analog performances, the V_{EA} and A_V should be higher as possible. The D2 and D3 devices, i.e. DM configurations, show better values than the D1 device (SM). The improvement in V_{EA} leads to improve the output resistance because of reductions of SCEs in the DM devices. As before, a significant improvement in the device gains is evident in Fig. 4.16 (a) for the DM devices in comparison to the SM device. Such improvement in the device gain for the DM devices is mainly due to the reduced g_d and partially due to the improved g_m in such devices, as observed in Fig. 4.15 (a). The intrinsic capacitances C_{gs} and C_{gd} as a function of V_{GT} for both subthreshold and above threshold or strong inversion regions are shown in Fig. 4.16 (b). The C_{gs} values are

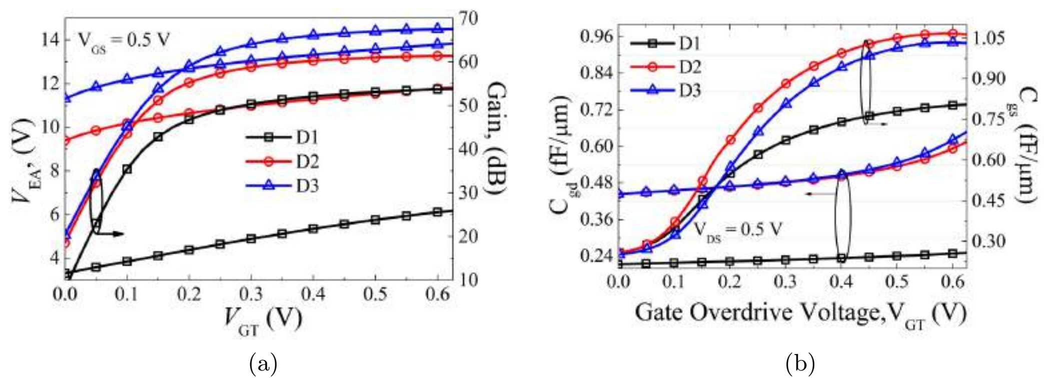
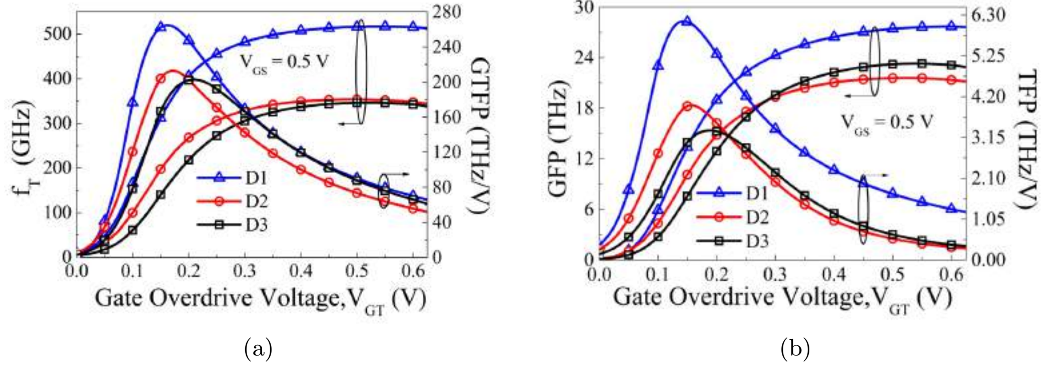


Figure 4.16: (a) Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for n-MOSFET at $V_{DS} = 0.5\,V$. (b) Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) as a function of gate over drive voltage (V_{GT}).

considerably lower for DM devices than the SM device. It is due to the lower electron concentration at the source side of the device. Because of higher electron concentration at the drain side, the DM devices (D2 and D3) show a higher value of C_{gd}. It is observed

that both capacitances C_{gs} and C_{gd} start increasing with V_{GT} increase until saturation. After saturation, both values become constant as expected because; the additional V_{DS} cannot affect the junction.

Fig. 4.17 (a) emphasizes that the DM devices provide higher f_T in the above threshold voltage region than the SM device. The difference in f_T is mainly due to the difference in g_m. It is partially due to the higher value of total capacitance $(C_{gs} + C_{gd})$ as observed in Fig. 4.16 (b). The maximum value of the peak of f_T corresponds to the point between the minimum gate-drain/source capacitance and the peak of transconductance. Higher transconductance and lower parasitic gate capacitances are found for the device D2 as compared to other devices considered in this study. Moreover, Fig. 4.17 (a) reveals that f_T is higher for D2 reflecting superior gate controllability due to dual metal gate.



(a) (b)

Figure 4.17: RF FoMs as a function of gate over drive voltage (V_{GT}) at $V_{DS} = 0.5\,V$ of n-MOSFET (a) Cut off frequency (f_T) and gain transconductance frequency product ($GTFP$) (b) Gain frequency product (GFP) and transconductance frequency product (TFP).

$$TFP = (g_m/I_D) \times f_T \tag{4.8}$$

$$TFP = (g_m/I_D) \times f_T \tag{4.9}$$

A unique FoM for analog/RF performances is the gain transconductance frequency product ($GTFP$) as given in Eq. 4.5 and plotted in Fig. 4.17 (a). The peak value of $GTFP$ is achieved at $V_{GS} = 0.525\,V$ for all the configurations, where the level of drain current is quite low, i.e. $I_D \approx 10^{-5}\,A/\mu m$. It is interesting to note that the voltage corresponds to V_{GS} just above $150\,mV$ of the threshold voltage of the device. This allows the circuit designer to determine the best region of operation by trading off among gain, transconductance and speed. Here the device D2 shows higher $GTFP$ as compared to other configurations because of higher f_T, g_m and lower g_d. The product of g_m/I_D and f_T i.e. TFP is calculated by Eq. 4.8 and represents a tradeoff between power and bandwidth. TFP is also utilized in moderate to high speed designs. Similarly, gain frequency product i.e. GFP, as given in Eq. 4.9, is also a very important parameter for operational amplifiers in high frequency application. The GFP and TFP parameters as a function of V_{GT} for $V_{DS} = 0.5\,V$ are plotted in Fig. 4.17 (b). It appears that $GFP$and TFP are started linearly increasing with the

increase of V_{GT} in sub threshold region and hold an optimum value then start decreasing in saturation region. The DM devices show better GFP and TFP values than the SM device. This is due to the high g_m and f_T values of DM devices.

Table 4.11: RF performance of different devices for $V_{DS} = 0.5\,V$

Device	C_{gs} (fF)	C_{gd} (fF)	f_T (GHz)	GFP (GHz)	TFP (GHz/V)	$GTFP$ (GHz/V)
D1	1.651	0.251	286.75	1.535×10^4	3.584×10^3	1.535×10^5
D2	1.064	0.307	425.91	2.603×10^4	5.162×10^3	2.662×10^5
D3	1.031	0.324	421.33	2.843×10^4	4.071×10^3	2.247×10^5

As stated theTGF is slightly lower in case of DM device, but that will not hamper much in the device performance. Similarly, the peak values of RF FoMs like f_T, GFP, TFP and $GTFP$ are compared for various DG configurations at $V_{DS} = 0.5\,V$ in Table 4.11. From the data given in the table, the f_T, TFP and $GTFP$ values are better in case of DM-GS-DG case, i.e. D2 device. Because of the high doping profile near the source in case of DM-SH-GS-DG, i.e. D3, the device shows somewhat lower values of previously enumerated parameters than the D2 device.

4.4.3 Linearity Analysis

The higher order derivatives of $I_D - V_{GS}$ i.e. g_{m2} and g_{m3} against gate to source voltage (V_{GS}) for different device cases at $V_{DS} = 0.1\,V$ are plotted in Fig. 4.18 (a) and (b) respectively. Generally, for better linearity and lesser distortion the amplitude of g_{m2} and g_{m3} should be less. The value of V_{GS} at which the higher order of transconductance parameters (g_{m2} and g_{m3}) are become zero is known as zero crossover point (ZCP) which decide the optimum bias point for device operation. From the Fig. 4.18 (a) and (b), the DM architectures show lower value for both g_{m2} and g_{m3} as compare to SM counterpart. The D3 device i.e. DM-SH device gives minimum amplitudes of g_{m2} and g_{m3} as it shows a lower g_m.

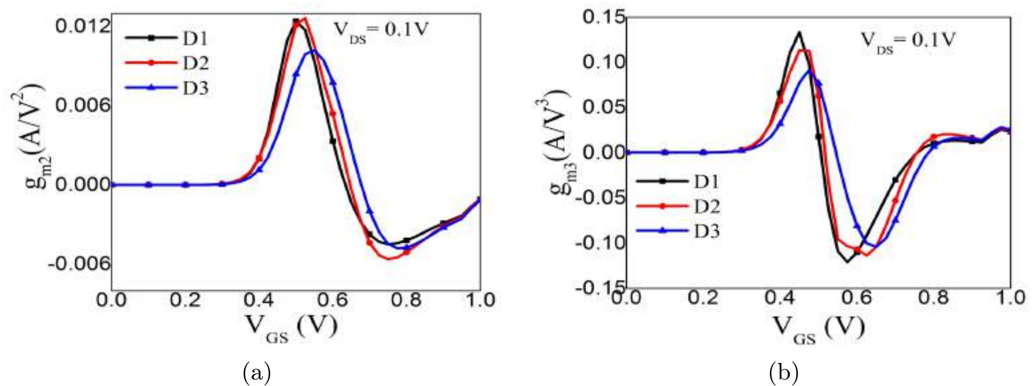


Figure 4.18: (a) g_{m2} (b) g_{m3}, as a function of gate to source voltage for $V_{DS} = 0.1\,V$.

VIP_2 and VIP_3 are the second and third order harmonics respectively and presented in Fig. 4.19 (a) and (b). These are the valuable FOMs, which can properly determine

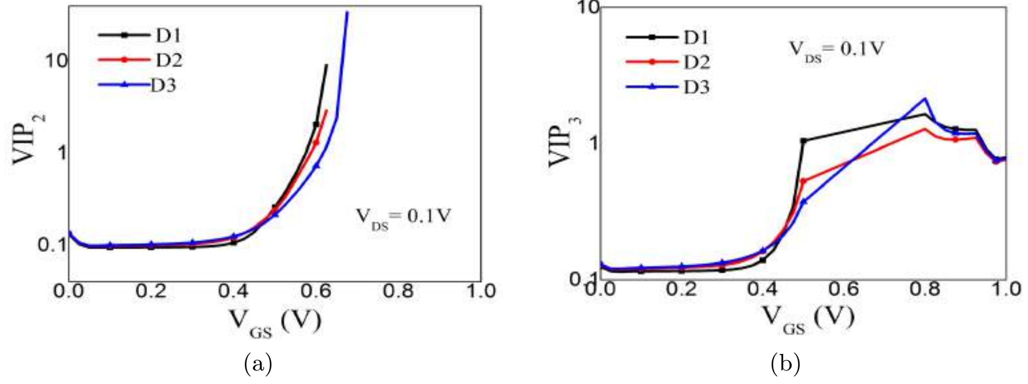


Figure 4.19: (a) VIP_2 (b) VIP_3, as a function of gate to source voltage (V_{GS}) at $V_{DS} = 0.1\ V$ for n-channel device cases.

the distortion characteristics. The amplitudes of VIP_2 and VIP_3 should be as high as possible for achieving high linearity. It can be seen from Fig. 4.19 (a) and (b) that the peak points of VIP_2 and VIP_3 are significantly increases for D3 architecture as compared to other devices. This is due to the reduced harmonic distortion i.e. amplitudes of g_{m2} and g_{m3} as discussed in Fig. 4.18 owing to improvement in carrier transport efficiency and less leakage current. Thus, DM-SH is more linear than SM and DM counterparts.

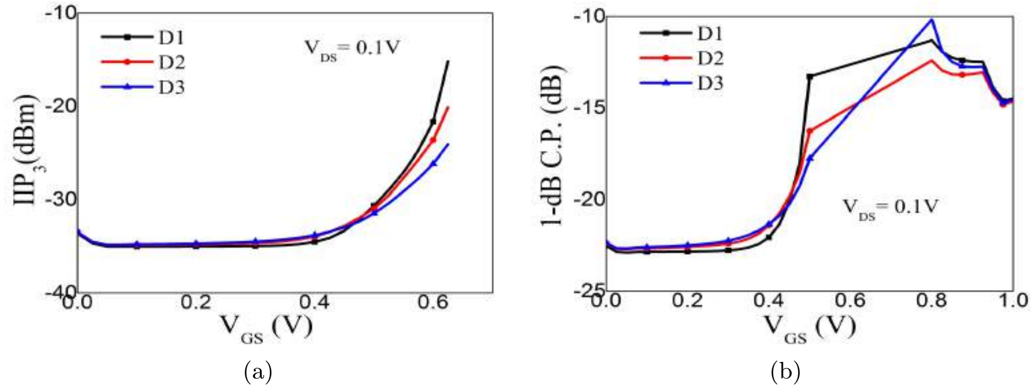


Figure 4.20: Comparison of Linearity Parameters as a function of gate to source voltage (V_{GS}) at $V_{DS} = 0.1\ V$ of n-MOSFET (a) IIP_3 (b) 1-dB Compression Point.

Again IIP_3 and 1-dB compression point are two more important FoMs for evaluating the linearity performance. Fig.4.20 (a) and (b) represents the variation of IIP_3 and 1-dB compression point with V_{GS} at $V_{DS} = 0.1\ V$ for all three configurations. 1-dB compression point is nothing but the input power value in dB at which the gain of the low noise amplifier drops by 1-dB. It is a crucial parameter for an amplifier as it gives the idea about maximum power handles by the amplifier. The D3 configuration shows peak amplitude in the case of 1-dB compression point as compared to others. It is because of the step profile in potential as discussed in Fig.4.13 (a) which enhances the carrier transport and improved gate controllability.

4.4.4 Validation with Reported Experimental Results

In accordance with ITRS for analog and mixed signal CMOS technology with $45-nm$, the target $I_{on} = 651\mu A/\mu m$.

Table 4.12: Validation with Reported Experimental Results-1

Parameters	**Widiez *et al.*** [131]		Ch.-2 (high-k)GS-DG	
	DG	SG	(Si_3N_4)	(HfO_2)
Ion $(\mu A/\mu m)$	506	346	570	568
I_{off} $(\mu A/\mu m)$	4.3×10^{-9}	8.3×10^{-7}	2.75×10^{-10}	3.01×10^{-10}
V_{th} (V)	0.45	0.3 V	0.325	0.3
$SS(mV/decade)$	64	80	61.21	62.19

Table 4.13: Validation with Reported Experimental Results-2

Parameters	Ch.-4 Miscellaneous Design of GS-DG		
	SM-GS-DG	DM-GS-DG	DM-GS-SH-DG
Ion $(\mu A/\mu m)$	646.6	**661.9**	608
I_{off} $(\mu A/\mu m)$	5.3×10^{-13}	1.3×10^{-12}	1×10^{-12}
V_{th} (V)	-	-	-
$SS(mV/decade)$	62.36	64.07	64.48

4.5 Summary

In this chapter high-k dielectrics have been investigated as an alternative to Silicon dioxide (SiO_2) based gate dielectric for nanoscale semiconductor devices. Analog/RF figures of merit (FoMs) such as transconductance, early voltage, transconductance generation factor (TGF), intrinsic gain, cutoff frequency, gain bandwidth product are explored for the device. The impact of channel length, metal gate work function, and miscellaneous device design are worked out with a solid understanding of what is happening in the device and extension towards linearity analysis.

The following technical topics and contributions are presented in this chapter:

- *Various high-k dielectrics on DG-MOSFET (Section 4.1)*

  This section presents the impact of the high-k oxide layer as single and gate stack (GS) in view of the analog and RF performance of DG-MOSFET at the nanoscale through 2-D device simulation. The key idea behind this investigation is to provide a physical explanation for the improved analog and RF performance exhibited by the device. It is observed that devices that have single oxide layer gate dielectric Si_3N_4 i.e. D2 and devices with gate stack i.e. D5, the $DIBL$ is improved by 6.77% and SS value is decreased by 1.85%. For analog performances the early voltage is raised by 5.91%, the gain of the device is improved by 2.44% and TGF values increases by

1.62%. Similarly the RF performances like f_T, $GTFP$, GFP and TFP are improved by 10.24%, 34.37%, 10.99% and 13.81% respectively for device D5 over device D2. Similarly comparing the device with HfO_2 as single layer dielectric i.e. D3 with double layer i.e. D6 it is observed that D6 have an improvement of 45.54 % in $DIBL$, 70.53% in V_{EA}, 16.19% in gain, 5.15% in f_T, 18.76% in TFP and 50.68% in $GTFP$ over D3.

It has been observed that the performance enhancement of GS configurations (k=7.5 i.e device D5 in the study) is encouraging as far as the nanoscale DG-MOSFET is concerned. Also it significantly reduces the SCEs. Parameters like DC gain of (91.257 dB, 43.436 dB), nearly ideal values (39.765 $V-1$, 39.589 $V-1$) of TGF, an early voltage of (2730 mV, 16897 mV), cutoff frequency (294 GHz, 515.5 GHz) and $GTFP$ of ($5.14 \times 10^5 GHz/V$, $1.72 \times 10^5 GHz/V$) for two different values of $V_{DS} = 0.1\,V$ and $0.5\,V$ respectively are found to be close to ideal values. Analysis shows an opportunity for realizing HP analog and RF circuits with the device proposed in this section i.e. device D5.

- *Impact of Channel Length on GS-DG MOSFET (Section 4.2)*

  A systematic study to show the impact of channel length on the analog/RF performances of GS-DG architecture. The downscaling of channel length becomes the biggest challenge to maintain a higher speed, low power and better electrostatic integrity for each generation. This investigation is done to find out the potential of the channel length in view of analog and RF performance measures of sub-100 nm.

  The improvement in $GTFP$ with L down scaling continues up till 40 nm where a peak value of $1.33 \times 10^5 GHzV^{-1}$ is attained. Beyond 40 nm, peak $GTFP$ value reduces to $1.20 \times 10^5 GHzV^{-1}$ in 30nm GS-DG MOSFET due to SCEs (peak $g_m/I_D \approxeq 34.669V^{-1}$ and $A_V \approxeq 35.458dB$, Table 4.5 and 4.6). The optimized performance values of "L" will be 40 nm for the chosen device dimension $DIBL = 37.24\,mV/V, SS = 65.95\,mV/decade, I_{on} = 1.912\,mA, A_V = 41.92\,dB, f_T = 425.80\,GHz, GTFP = 1.33 \times 10^5 GHz/V$. The other device parameters could also be properly chosen for further downscaling of the transistor.

  For shorter gate length devices ($L = 30nm$), the design results in an impressive 69.10% improvement in f_T along with 36.31% enhancement in “sweet spot” as compared to $L = 60\,nm$. The study generates an optimized channel length of $L = 40\,nm$ for the designed device dimension in connection with the analog and RF performance for circuit design.

- *Impact of Metal Gate Work Function on GS-DG MOSFET (Section 4.3)*

  A quantitative assessment on the GS-DG MOSFET performance values are numerically calculated with different gate metal work function ($\phi_m = 4.52\,eV, 4.6\,eV, 4.7\,eV$). The effect of electrostatic control on DC, analog and RF FoMs have been investigated.

  When gate metal work function was raised from 4.52 eV to 4.6 eV, the SS and $DIBL$

were decreased by 0.83% and 2.3%, respectively. Similarly, the output conductance (g_d) is decreased by 62.73%, and A_V is increased by 15.23% in 4.6 eV case. These results enhance the important FoMs of the technology, i.e. TGF by 4.51%, f_T by 14.10%, TFP by 43.13%, GFP by 30.3% and $GTFP$ by 77.27% for the 4.6 eV device case as compare to its counterpart the 4.52 eV case.

- *GS-DG-MOSFET with Miscellaneous Device Design (Section 4.4)*

  The analog performance, as well as some new RF FoMs, are proposed for the first time on GS-DG MOSFET with various gate and channel engineering. The comparison is made through various performance metrics between single material (SM) GS-DG, dual material (DM) GS-DG, and dual material single halo (DM-SH) GS-DG MOSFETs. The key idea behind this investigation is to provide a physical explanation for the improved analog and RF performances exhibited by the device.

  The DM-GS-DG device, i.e. D2, shows an interesting improvement in early voltage by 91.41%, gain of the device by 14.06%, cut off frequency f_T by 48.53%, $GTFP$ by 73.42%, GFP by 69.57% and TFP by 44.02% over its counterpart SM-GS-DG i.e. D1 device. Moreover, the DM configuration with the addition of LAC doping i.e. D3 device shows optimum values in the case of A_V and GFP. Only a decrement of 5.8% in TGF for DM devices as compared to SM device will not hamper that much to the performance. Therefore, the DM devices can be very attractive for ultra low-power high-frequency analog/RF applications.

  The analysis shows an opportunity for realizing high-performance analog and RF circuits with the device are proposed. The DM-DG configurations can be preferred over SM-DG as they show 48.53% improvement in f_T, 25.54% in A_V and more than 90% in V_{EA}.

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List of Contribution

1. P. K. Sahu, **S. K. Mohapatra**, and K. P. Pradhan, "A Study of SCEs and Analog FOMs in GS-DG-MOSFET with Lateral Asymmetric Channel Doping," *Journal of Semiconductor Technology and Science*, vol. 13,no. 6, pp. 647-654, Dec. 2013.

2. K. P. Pradhan, **S. K. Mohapatra**, P. K. Sahu, and D. K. Behera, "Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET," *Microelectronics Journal*, vol. 45, no. 2, pp. 144-151, 2014.

3. P. K. Sahu, **S. K. Mohapatra**, and K. P. Pradhan, "Impact of Downscaling on Analog/RF Performance of sub-100 nm GS-DG MOSFET," *Informacije Midem-Journal of Microelectronics Electronic Componentsand Materials*, vol. 44, no. 2, pp. 119-125, Mar. 2014.

4. **S. K. Mohapatra**, K. P. Pradhan, P. K. Sahu, and M. R. Kumar, "The performance measure of GS-DG MOSFET: an impact of metal gate work function," *Advances in Natural Sciences: Nanoscience and Nanotechnology*, vol. 5, no. 2, pp. 1-6, Mar. 2014.

5. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Improved Performance in GS-DG-MOSFET with Dual Material Gate and Lateral Asymmetric Channel," in 16th *International Conference on Automatic Control, Modelling & Simulation*, Brasov, Romania, Jun. 2014, pp. 267-271.

6. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Inuence of High-k Gate Dielectric on Nanoscale DG-MOSFET." *International Journal of Advanced Science & Technology*, vol. 65, 2014.

7. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Linearity and Analog Performance Analysis in GSDG-MOSFET with Gate and Channel Engineering," in *Proceedings of IEEE* 11th *INDICON, Emerging Trends and Innovation in Technology*, Pune, India, Dec. 2014, pp. 1-5.

8. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Estimation of Analog/RF FOMs using Device Design Engineering in GS-DG-MOSFET," *Materials Science in Semiconductor Processing*, vol. 31, pp. 455-462, 2015.

9. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Improved Performance in GS-DG-MOSFET with Dual Material Gate and Lateral Asymmetric Channel," *Int. J. of Nano and Biomaterials*, vol. 5, no. 4, 2014.

Chapter 5

Role of Fin Aspect Ratio in sub-20 nm SOI-FinFET

Nowadays, FinFETs integrated into complex circuit applications, they could fulfill the demand for smartphones and tablets with the better performance and make for chips that compute faster. This chapter presents a detailed analysis of the impact of fin height (H_{Fin}) and width (W_{Fin}) on various AC figures of merit (FoMs).

5.1 Sub-20 nm SOI FinFET

FinFETs are pragmatic DG devices, easy to fabricate, harder to optimize [60, 132]. Since the gates are on the lateral sides, the edges of the transistor need to be smooth, and the inter-gate distance should be in the 10 nm range. The underlying mechanisms in planar DG and FinFETs are more or less the same, simply transformed by a rotation from horizontalÂăto the vertical direction. Separating the two gates (MugFET) is very useful for signal mixing and threshold voltage adjustment. But, if the two gates are meant to stay interconnected, a more efficient solution is to fabricate Triple-Gate FinFETs [133].

The FinFET technology is becoming more widespread as feature sizes within integrated circuits fall, and there is a growing need to provide very much higher levels of integration with less power consumption within integrated circuits. FinFETs are not available as discrete devices. So, it is essential to simulate for studying performance variation in view of analog and RF circuit application. In continuation of our previous study on DG-MOSFET, it is a unique attempt has been made to present a deep analysis of process variability dependency on various performance metrics of 3D FinFET. The 3-D SOI-FinFET simulated in this work is shown in Fig. 5.1. Table 5.1

Table 5.1: Device Parameters as per ITRS 2013

Design	**HP**	**LOP**	**LSTP**	**This Work FinFET/Trigate**
Gate length, L_g (nm)	20	20	20	20
EOT, t_{ox} (nm)	0.84	0.9	1.2	0.9
Supply Voltage, V_{DD} (V)	0.85	0.67	0.87	0.7

typifies the design considerations of the device. An n-channel MOSFET having inter facial oxide as SiO_2 with high-k material (Si_3N_4) as spacer in the underlap regions are modeled. The Source/Drain length (L_S/L_D) as 40 nm, and doping is uniform with N_D at a density of 10^{20} cm^{-3} is considered. The Equivalent Oxide Thickness (EOT) is 0.9 nm [134, 135] and supply voltage $V_{DD} = 0.7\,V$. The work function for the gate electrode is assumed as 4.5 eV. The undoped channel is maximizes the effective mobility and hence on current density from the source [136]. Table symbolizes the typical cases that are reckoned for device simulation.

Table 5.2: Typical cases of 3D SOI-FINEET for study

Device Design	H_{Fin}/L_g	W_{Fin}/L_g
[43, 135, 137]	0.25, 0.6, 0.8, 1.0, 1.1, 1.3	0.25, 0.5, 0.6, 0.8

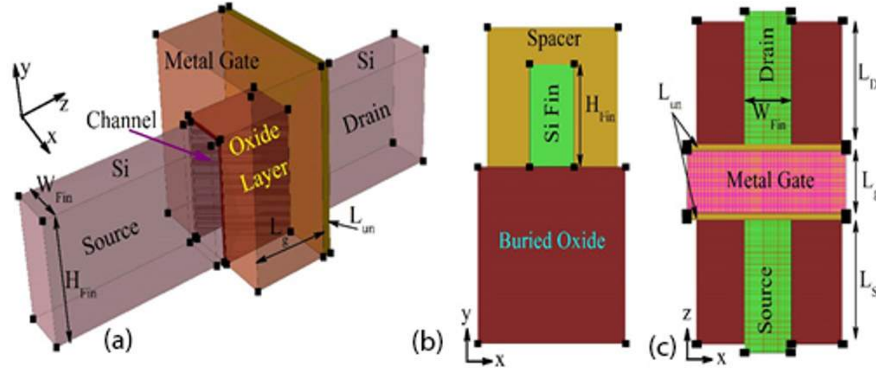


Figure 5.1: Perspective view of SOI FinFET (a) 3-D view (b) 2-D view in x-y (c) 2-D view in x-z . The metal and spacer regions are made transparent in (a).

5.1.1 Simulation Setup for this Work

- The ϕ_m adjusted to achieve the desired V_{th} value. The numerical simulation uses the drift-diffusion [138] approach and field dependent mobility, concentration dependant mobility and velocity saturation model [139].
- Suitable empirical parameter β is selected to calibrate the drift-diffusion transport model. The inversion layer mobility models Lombardi (constant voltage and temperature, CVT) [140, 141] and Auger recombination models are included.
- All the structure junctions are assumed as abrupt, the biasing conditions are reckoned at room temperature and the generation of smooth mesh [142] is done in the simulation.
- The validity of the simulator has been investigated by comparing its results with previous literature data. From Fig. 5.2, it can be noted that our simulation results are in great agreement with Andrade *et al.* [134].

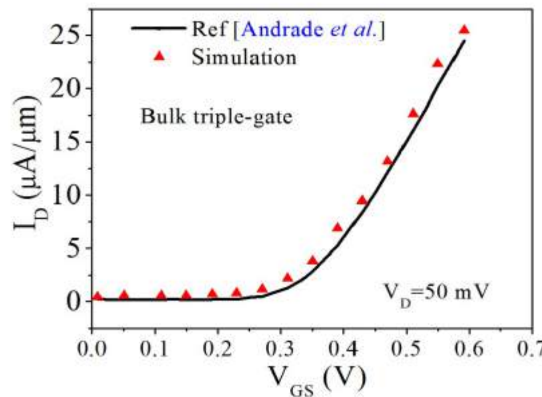


Figure 5.2: Simulation Setup are in good agreement with Experimental data

5.1.2 Static Performance of 3-D FinFET

The advantages of FinFET technology are higher drain current and switching speed, less than half the dynamic power requirement with 90% less static leakage current [143, 144].

The most important geometric parameter of FinFET technology are fin height (H_{Fin}) and fin width (W_{Fin}), which ratio known as aspect ratio ($AR = W_{Fin}/H_{Fin}$) [145]. The structural classification of the device is FinFET ($AR < 1$), Trigate ($AR = 1$) and Planar ($AR > 1$) [135]. Taller fins in the device shows higher on current (I_{on}) and narrow fins establish SCEs immunity. A trade off is required in between device performances with its aspect ratio [133].

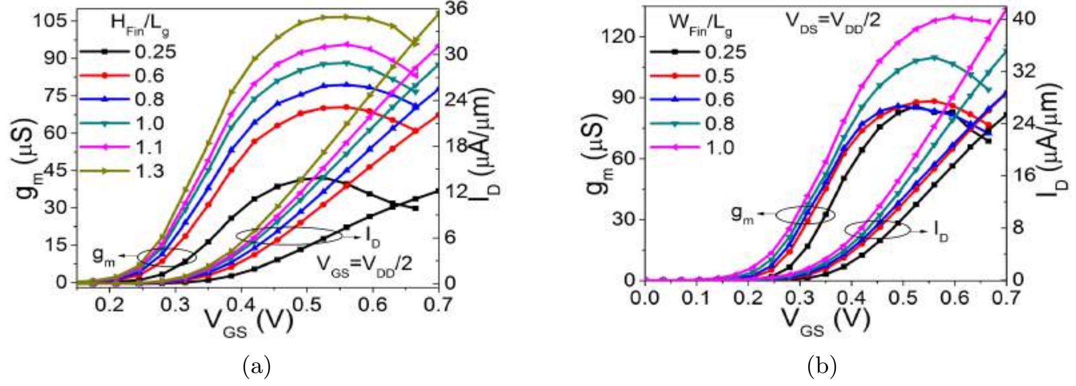


Figure 5.3: Drain current (I_D) variability of process parameter (a) H_{Fin} (b) W_{Fin} in linear scale as a function of gate to source voltage (V_{GS}).

The variation of Fin height and fin width on drain current is plotted in Fig. 5.3. As the height and width of the Fin increase the on current enhancement occurs. However, if we observe the same plot on a logarithmic scale, then there is a high leakage current for higher values of H_{Fin} and W_{Fin}. There is always a trade-off between I_{on} and I_{off} for device design. So, the device engineers can choose the optimum parameter dimensions as per their requirement. The extracted values of I_{on} and I_{off} for different H_{Fin}/L_g

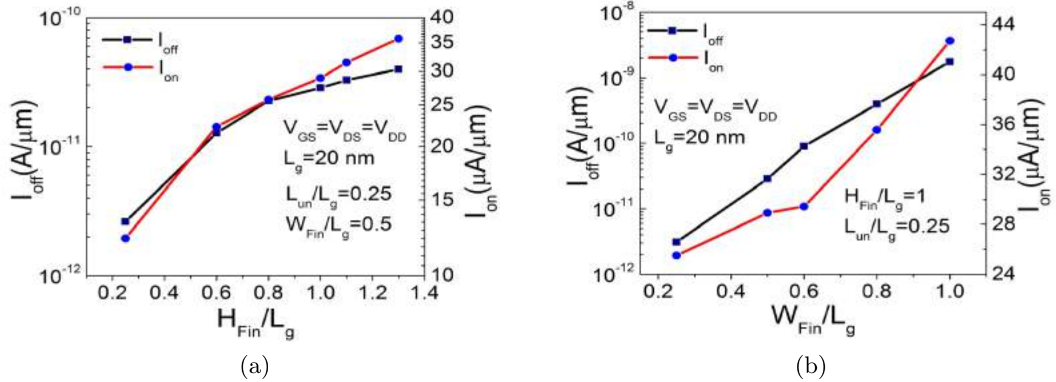


Figure 5.4: On current (I_{on}) and leakage current (I_{off}) with variation of (a) H_{Fin} (b) W_{Fin} at $V_{GS} = V_{DS} = V_{DD}$.

ratio are presented in Fig. 5.4 (a). As per our previous discussion, both the I_{on} and I_{off} increases with the increase in H_{Fin}. This is to confirm that for high drive current with matching the current drivability taller fins are required, whereas narrow fins give better SCE immunity. This is because an increasing in H_{Fin} the electric field in the silicon region decreases which minimizes the leakage current. By comparing the I_{on} and I_{off} for all H_{Fin}/L_g cases, we can say that $H_{Fin} = 0.6 \times L_g$ is the optimum one as it gives

a moderate value for both I_{on} and I_{off}. Fig. 5.4 (b) discussed the sameI_{on} and I_{off} for different W_{Fin}/L_g ratio. A wider fin width ($W_{Fin} = 1 \times L_g$) give unacceptable SCEs, whereas a narrower fin width ($W_{Fin} = 0.2 \times L_g$) is more difficult to fabricate. So, we can take the moderate one i.e. $W_{Fin} = 0.6 \times L_g$ as the optimized W_{Fin}/L_g ratio.

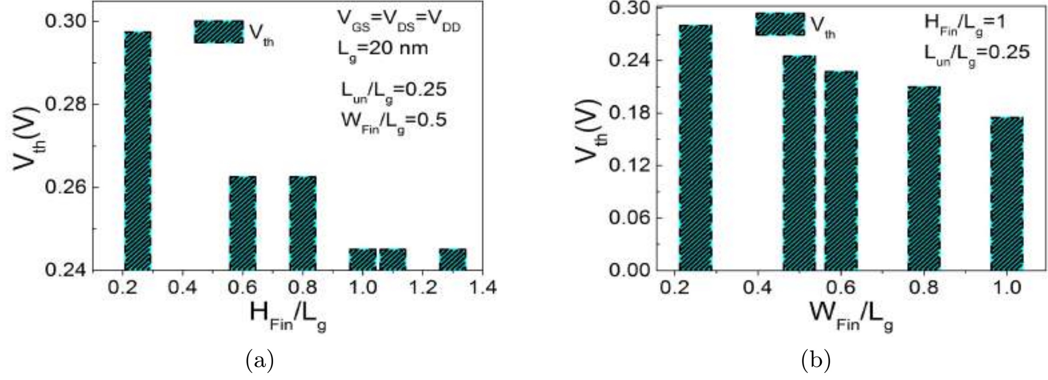


Figure 5.5: Variation of threshold voltage (V_{th}) of the device as a function of of (a) H_{Fin} (b) W_{Fin} at $V_{GS} = V_{DS} = V_{DD}$.

The V_{th} sensitivity towards H_{Fin}/L_g and WFin/Lg ratios are presented in Fig. 5.5. V_{th} is extracted at the gate voltage where drain current I_D is $100nA$. For $H_{Fin} = 1.3 \times L_g$, the V_{th} value in the TG-SOI FinFET design is the smallest among the other H_{Fin}/L_g ratios. That means the V_{th} decreases with increase in H_{Fin}/L_g ratio. For the multigate structures like FinFET, V_{th} is dependent on W_{Fin} as the side gates influence the channel potential. From the figures by comparing all the variations of H_{Fin}/L_g and W_{Fin}/L_g ratios, the W_{Fin} or $H_{Fin} = 0.6 \times L_g$ or $0.8 \times L_g$ can be considered as the optimum ones for design consideration point of view.

Various performance metrics like $g_m, TGF, g_d, V_{EA}, C_{gg}, f_T, R_o$, and Gain ($A_V$) are evaluated and the sensitivity of above said parameters with W_{Fin}, and H_{Fin} are systematically presented in the following sections. Finally, depending upon the aspect ratio (W_{Fin}/H_{Fin}) of the device, we have distinguished the 3-D device as FinFET or Trigate or planar device. The intrinsic delay and power dissipation are also discussed for all the three cases of the device.

5.1.3 Effect of H_{Fin} on Analog/RF Performance

Fig. 5.6 (a) and (b) show the plot of g_m for 20 nm FinFETs at high ($V_{DD}/2$) and low ($50mV$) drain biases for different H_{Fin}/L_g ratios. The other main device parameters are $L_g = 20\,nm, W_{Fin} = 10\,nm, t_{ox} = 0.9\,nm, t_{box} = 40\,nm, t_{sub} = 70\,nm, L_{un} = 5\,nm, T = 300\,K$. for this analysis. To analyze the immense improvement in g_m ($\partial I_D/\partial V_{GS}$) with increase in H_{Fin}/L_g ratio, we have evaluated and studied the $I_D - g_m$ curve. According to the literature, access resistance problem is more serious in FinFETs. However, some solutions are available like increasing the H_{Fin} out of the gate region [146]. The parasitic resistance problem can be avoided by using higher H_{Fin}/L_g ratio which further increases the drain current. This is also validated from Fig. 5.6 (a) and (b), both the parameters i.e. I_D, and g_m are increasing with increase in H_{Fin}/L_g ratio. Higher I_D, and g_m values

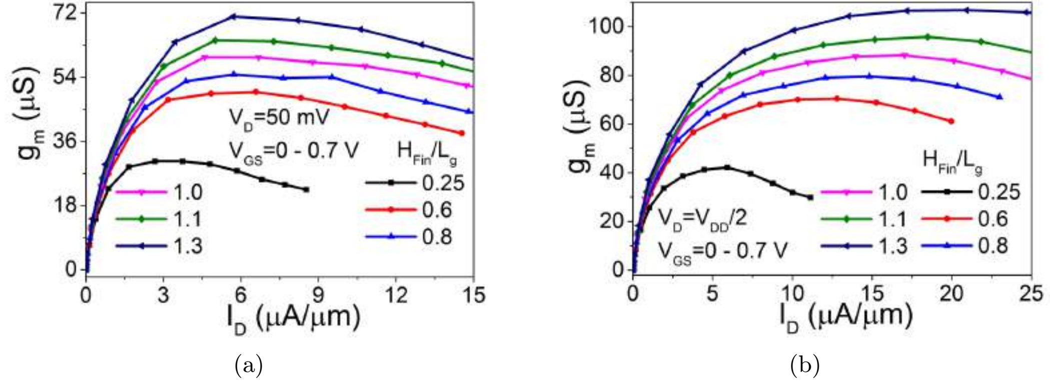


Figure 5.6: Transconductance (g_m) as a function of drain current (I_D) of the device (a) for $V_{DS} = 0.05\,V$ (b) for $V_{DS} = 0.35\,V$.

are obtained for $H_{Fin} = 1.1 \times L_g$ i.e. 22 nm and $H_{Fin} = 1.3 \times L_g$ i.e. 26 nm cases.

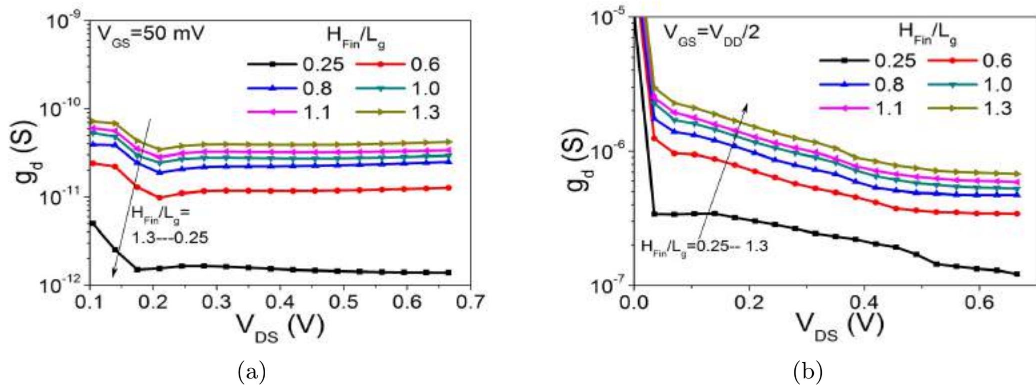
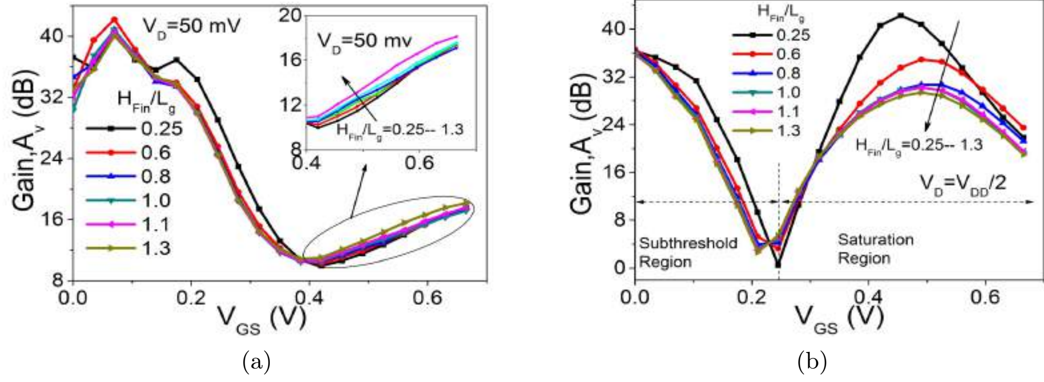


Figure 5.7: Drain conductance (g_d) of the device as a function of drain to source voltage (V_{DS}) (a) for $V_{GS} = 0.05\,V$ (b) for $V_{GS} = 0.35\,V$.

Fig. 5.7 (a) and (b) show the variation of output conductance (g_d) with V_{DS} at high ($0.35V$) and low ($50mV$) gate biases for different H_{Fin}/L_g ratio. Because of the wrapping of gate from three sides of the channel and narrow Fin width, FinFETs have more electrostatic control over the channel and it is fully depleted. For this reason drain bias dependency (depletion width at drain side) is less, so is the channel length modulation (CLM) which further minimizes the change in I_D, and hence the g_d ($\partial I_D/\partial V_{DS}$) is low. Again from the Fig. 5.7 (a) and (b), g_d increases with increase in H_{Fin}/L_g ratio which can hamper the gain (g_m/g_d) of the device.

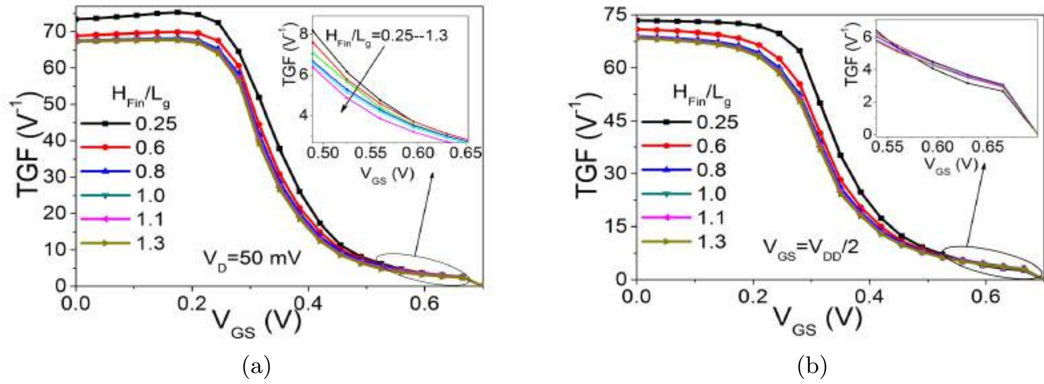
CMOS Analog circuits require transistors with low g_d in order to achieve high gain. Higher the g_d means, low output resistance which resulting an increase in I_D with V_{DS} in saturation regime. The components are associated with this increase, namely CLM and $DIBL$. Fig. 5.8 (a) and (b) demonstrate the intrinsic gain (A_V) for different region of operations of the FinFET with the variation of H_{Fin}/L_g ratio. From the figure, a decrement in H_{Fin}/L_g ratio will depict a higher A_V. This is due to the large reduction in g_d values for lower H_{Fin}/L_g ratios which is already discussed in Fig. 5.7 (a) and (b).

Transconductance generation factor ($TGF = g_m/I_D$) is plotted against V_{GS} with a variation of H_{Fin}/L_g ratio at two different V_{DS} is plotted in Fig. 5.9 (a) and (b). TGF



(a) (b)

Figure 5.8: Intrinsic gain ($A_V = g_m/g_d$) as a function of gate to source voltage (V_{GS}) (a) for $V_{DS} = 0.05\,V$ (b) for $V_{DS} = 0.35\,V$.



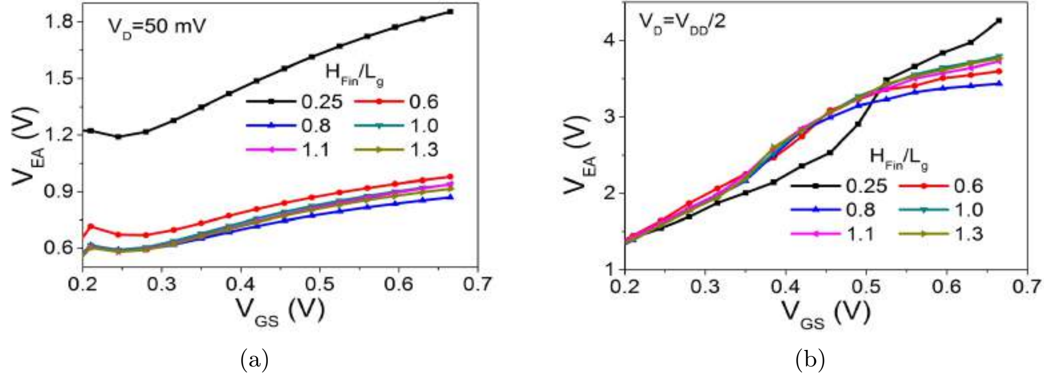
(a) (b)

Figure 5.9: Transconductance generation factor ($TGF = g_m/I_D$) as a function of gate to source voltage (V_{GS}) (a) for $V_{DS} = 0.05\,V$ (b) for $V_{DS} = 0.35\,V$.

demonstrates the effective use of the current to achieve a desired value of transconductance. The high value of TGF is advantageous to realize analog circuits which are operating at low supply voltage. From the figure, the variation of TGF occurs at subthreshold region (at low V_{GS} and low V_{DS}) of operation and almost same TGF is achieved in strong inversion. This g_m/I_D ratio is inversely proportional to the level of channel inversion i.e. to the higher I_D value. Form Fig. 5.9 (a) and (b), lower H_{Fin}/L_g ratios depict high TGF values and it gradually decreases as H_{Fin}/L_g ratio increases in the subthreshold region of operation. This is due to the higher I_D values for larger H_{Fin}/L_g ratios as given in Fig. 5.6.

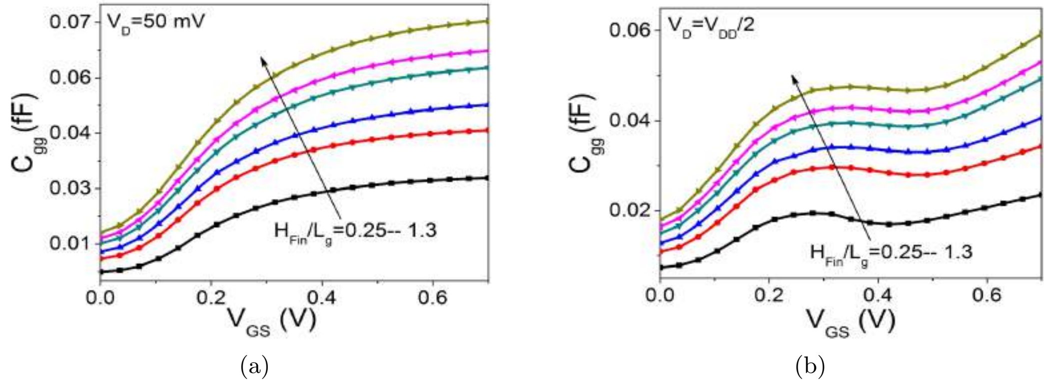
Also a low g_d propagates a higher drain current to output conductance ratio, which is nothing but the early voltage ($V_{EA} = I_D/g_d$) of the device. Fig. 5.10 (a) and (b) show the variation of V_{EA} as a function of V_{GS} for different H_{Fin}/L_g ratios at two regions of operation. From the Fig. 5.10 (a) and (b), the devices with small H_{Fin}/L_g ratios have a good control over CLM and DIBL owing to low gd value which further improves the V_{EA}. For better analog performance the V_{EA} and A_V should be as high as possible. The V_{EA} is increasing with a decrease in H_{Fin}/L_g ratio in the subthreshold region ($V_D = 50\,mV$), however there is no such variations in the super threshold region ($V_D = 0.35\,V$).

The C_{gg} value of the device increases with increase in H_{Fin}/L_g ratio. It is caused by the increased fringing field density with H_{Fin}/L_g ratio. Sun et al. [137] have reported



(a) (b)

Figure 5.10: Early Voltage ($V_{EA} = I_D/g_d$) as a function of drain to source voltage (V_{DS}) (a) for $V_{DS} = 0.05\,V$(b) for $V_{DS} = 0.35\,V$.

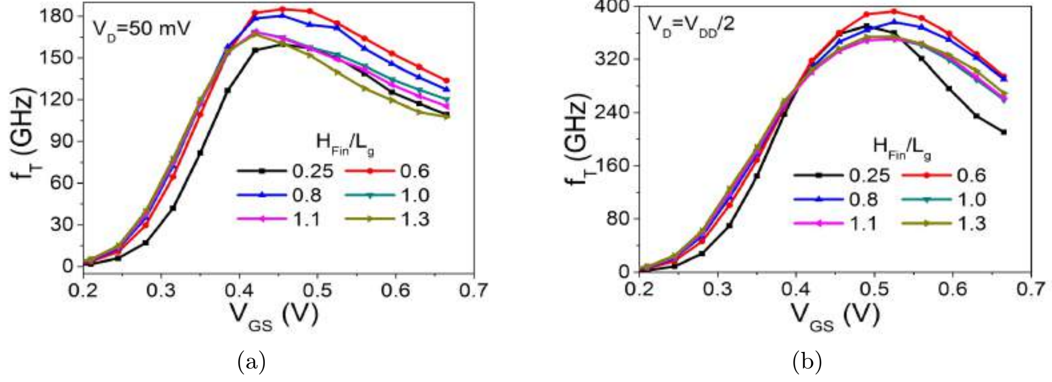


(a) (b)

Figure 5.11: Total gate capacitance (C_{gg}) as a function of gate to source voltage (V_{GS}) (a) for $V_{DS} = 0.05\,V$(b) for $V_{DS} = 0.35\,V$.

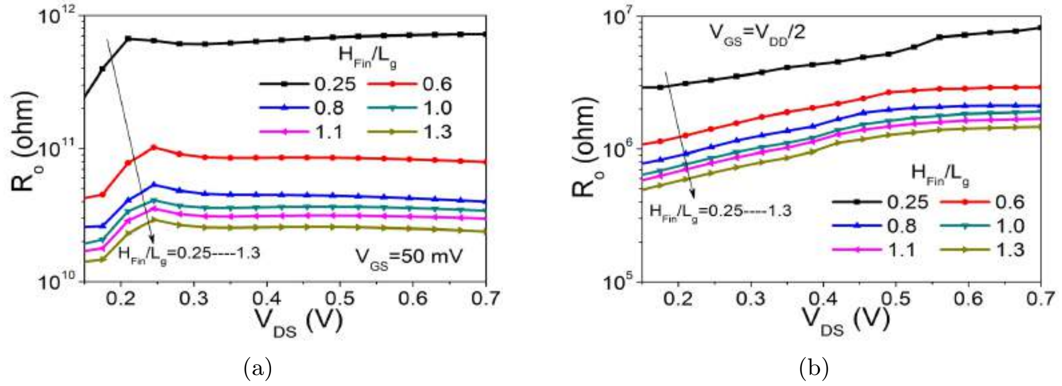
that $H_{Fin} = 0.6 \times L_g$ or $0.8 \times L_g$ are good for better SCE immunity. So, we have varied H_{Fin} from $0.25 \times Lg$ to $1.3 \times Lg$. As FinFET has a taller stripe, then the height of gate electrode along the channel side walls is larger which increases the fringing field, so as the total capacitance. Cut-off frequency f_T is one of the most important parameters for evaluating the RF performance of the device. Generally, f_T is the frequency when the current gain is unity.

From Fig. 5.12 (a) and (b), the variations of f_T can be observed with respect to V_{GS} for different H_{Fin}/L_g ratios. As we know $f_T = g_m/2\pi C_{gg}$, so both g_m and C_{gg} values will have equal and opposite influence on f_T. The reduction in capacitance in case of lower H_{Fin}/L_g ratios (refer Fig. 5.11) is further counterbalanced by reduction of g_m with lower in H_{Fin}/L_g ratio (refer Fig. 5.6). It is very much significant that the forecast improvement in f_T with traditional scaling of a FinFET can be only achievable by choosing optimal value of H_{Fin} and W_{Fin}. The difference in f_T is mainly due to the difference in g_m, and partially due to the higher value of total capacitance (C_{gg}). The peak point of f_T corresponds to the point between the minimum gate-drain/source capacitance and peak of transconductance. It is also clear from Fig. 10 that f_T is highest for the device having $H_{Fin} = 0.6 \times L_g$, reflecting superior gate controllability, and hence higher transconductance and lower parasitic gate capacitances as compared to other devices considered in our study.



(a) (b)

Figure 5.12: Cutoff frequency (f_T) as a function of gate to source voltage (V_{GS}) (a) for $V_{DS} = 0.05\,V$(b) for $V_{DS} = 0.35\,V$.



(a) (b)

Figure 5.13: Output resistance (R_0) of the device as a function of drain to source voltage (V_{DS}) (a) for $V_{DS} = 0.05\,V$(b) for $V_{DS} = 0.35\,V$.

Fig. 5.13 (a) and (b) show the output resistance (R_0) for different H_{Fin}/L_g ratios at low and high V_{DS}. R_0 also have an impact on the intrinsic gain ($g_m \times R_0$). According to the figure, the lower H_{Fin} devices predict larger R_0. This is due to the improvement in SCEs and lower values of g_d (as $R_0 = 1/g_d$) for low H_{Fin}/L_g ratios (refer Fig. 5.7).

The important FoMs for circuit design application are discussed with various Fin height and at a constant width of 10 nm. The impact of Fin width with a constant height of 20 nm are as follows.

5.1.4 Effect of W_{Fin} on Analog/RF Performance

A systematically investigation with a variation of W_{Fin}/L_g ratio are done. For the simulation in this section the main device parameters are $L_g = 20\,nm$, $H_{Fin} = 20\,nm$, $t_{ox} = 0.9\,nm$, $t_{box} = 40\,nm$, $t_{sub} = 70\,nm$, $L_{un} = 5\,nm$, V_{GS} varied from 0 V-to-0.7 V, $T = 300\,K$. By choosing a smaller W_{Fin}, we can able to minimize the longitudinal electric field at the source side because of closeness of multiple gates [147]. However, as scaling approaches the fundamental dimension such as atomic size range, the sensitivity of the device parameters have a greater impact on the device performance. Fig. 5.14 (a) and (b) show the $g_m - I_D$ plot with a variation of W_{Fin}/L_g ratio at $V_{DS} = 0.05\,V$ and $V_{DS} = 0.35\,V$ respectively. Here W_{Fin} is varied from $0.25 \times L_g$ to $1.0 \times L_g$ because for this aforesaid technology node, Sun *et al.* [137] have reported that $W_{Fin} = 0.6 \times L_g$ for

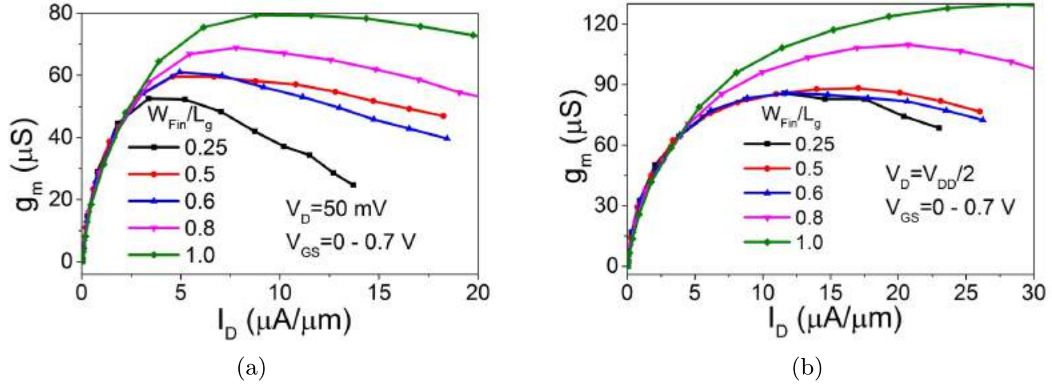


Figure 5.14: Transconductance (g_m) as a function of Drain current (I_D) of the device (a) for $V_{DS} = 0.05\,V$ (b) for $V_{DS} = 0.35\,V$.

FinFET and $W_{Fin} = 1.0 \times L_g$ for Trigate is required to minimize SCEs. Both I_D and g_m are increasing with increase in W_{Fin}/L_g ratio as predicted and obtained maximum values at $W_{Fin} = 0.25 \times L_g$. The effect of series resistance is clearly visible from Fig. 5.14 (a) (low drain bias/linear region) by not following the linear dependency nature for low W_{Fin} cases. From this analysis we can say that the R_S is much higher for low Fin width devices.

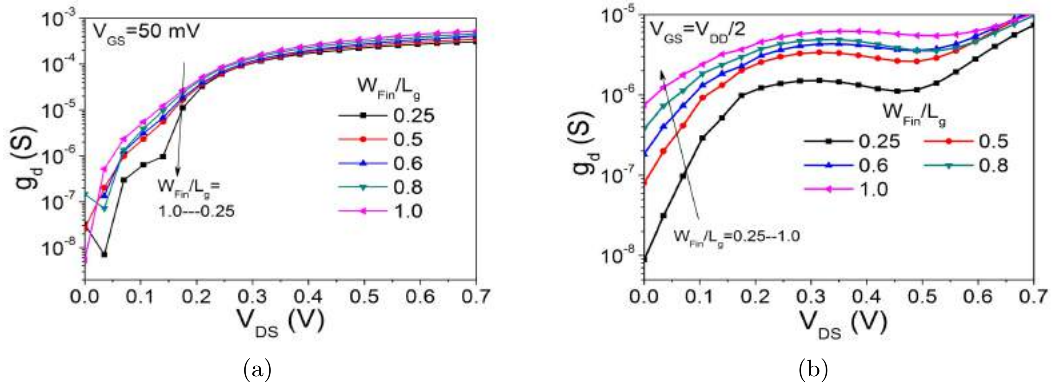
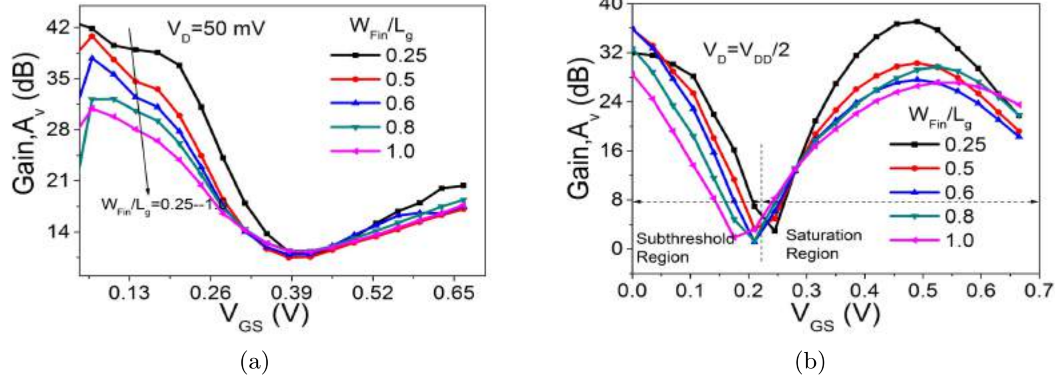


Figure 5.15: Drain conductance (g_d) of the device as a function of drain to source voltage (V_{DS}) (a) for $V_{GS} = 0.05\,V$ (b) for $V_{GS} = 0.35\,V$.

Fig. 5.15 (a) and (b) demonstrate $g_d - V_{DS}$ curve for different W_{Fin}/L_g ratios at two regions of operation. The output conductance is related to the important device dimensions as ($g_d \approx 2H_{Fin} + W_{Fin}$) [148]. So, g_d is directly proportional to W_{Fin} i.e. narrower W_{Fin} predicts lower g_d values which is our requirement. It can be observed that the g_d variation is more for higher applied voltage ($V_{GS} = V_{DD}/2$) case. This because of the device is heating at higher biasing voltage. Moreover, thinning the W_{Fin} and reducing the supply voltage are worthy enough to reduce the body heating problem, hence, the SCEs. So, the FinFETs with thinner fin width are well known for suppression of SCEs because they are free from substrate associated degradation in the g_d.

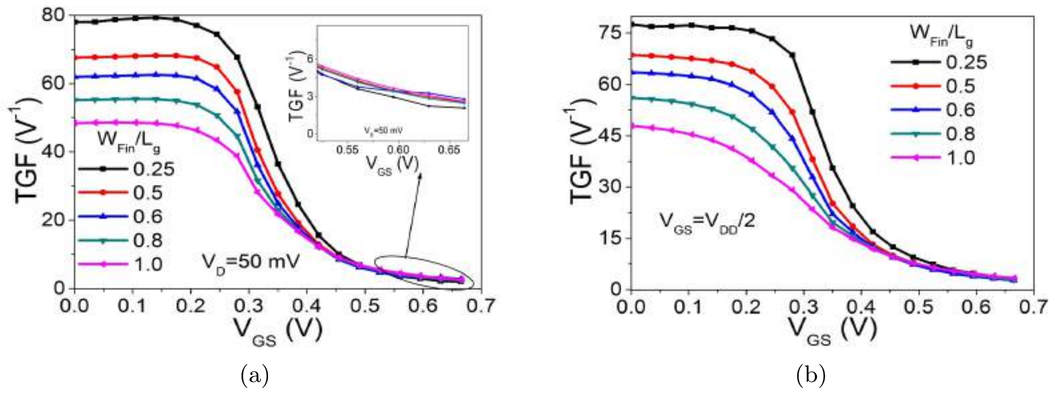
Fig. 5.16 (a) and (b) show the intrinsic gain (A_V) of the device against V_{GS} with a variation of W_{Fin}/L_g ranging from 0.25 to 1.0 at $V_{DS} = 50\,mV$ and $V_{DD}/2$. A higher gain can be observed for the FinFETs having lower fin widths is due to the much lower g_d



(a) (b)

Figure 5.16: Intrinsic gain ($A_V = g_m/g_d$) as a function of gate to source voltage (V_{GS}) (a) for $V_{DS} = 0.05\,V$ (b) for $V_{DS} = 0.35\,V$.

(refer Fig. 5.15), which is because of the fully depletion of fins. A plot of $TGF(g_m/I_D)$

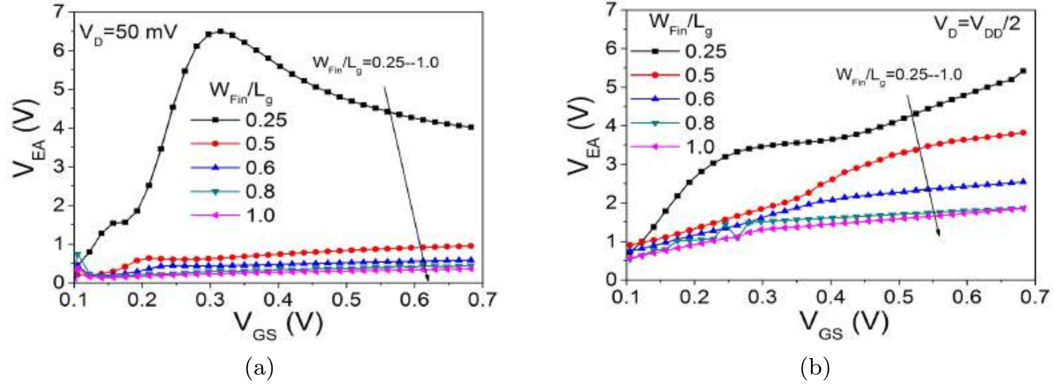


(a) (b)

Figure 5.17: Transconductance generation factor ($TGF = g_m/I_D$) as a function of gate to source voltage (V_{GS}) (a) for $V_{DS} = 0.05\,V$ (b) for $V_{DS} = 0.35\,V$.

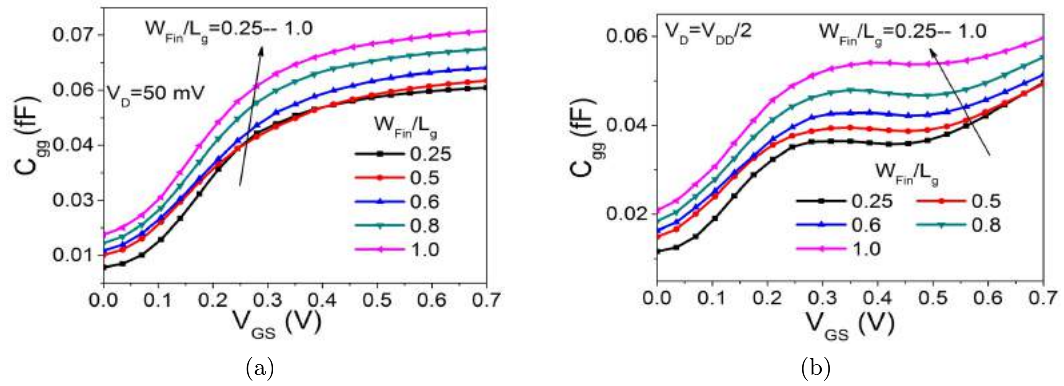
as a function of V_{GS} for both linear and saturation regions of operation is given in Fig. 5.17 (a) and (b). g_m/I_D is more sensitive to W_{Fin}/L_g ratio at linear region (low V_{GS}), however in saturation region (high V_{GS}), the variation seems to be much smaller (refer the inset figure). As per Subramanian *et. al* [149] g_m/I_D has a strong dependency on series resistance (R_S) than any other parameter. So, I_D,sat is a strong function of R_S and the ratio (g_m/I_D)sat is a weak function of R_S hence less sensitive in saturation region. The decrement in g_d for low fin widths can also be explained in terms of higher early voltage ($V_{EA} = I_D/g_d$) as observed from Fig. 5.18 (a) and (b). V_{EA} is used to explain the $I_D - V_{DS}$ curve for BJT, however in case of MOSFET, it is the hypothesized intercept of saturation output characteristics on the V_{DS} axis. However, we can say that lower W_{Fin}/L_g ratios predict better V_{EA} due to the reduction of substrate effect, body heating problem, and better immunity towards SCEs as discussed under Fig. 5.15.

The $C_{gg} - V_{GS}$ data for different fin width at $V_{DS} = 0.05\,V$ and $0.35\,V$ are presented in Fig. 5.19 (a) and (b) respectively. It can be measured that the C_{gg} values are much lower for FinFETs with low W_{Fin}/L_g ratios. There is a 25.37% of reduction in C_{gg} from $W_{Fin}/L_g = 1$ to $W_{Fin}/L_g = 0.25$. However from Fig. 5.14, we know that higher W_{Fin}/L_g ratios also predict high transconductance values. So, increase in gm contributes



(a) (b)

Figure 5.18: Early Voltage ($V_{EA} = I_D/g_d$) as a function of drain to source voltage (V_{DS}) (a) for $V_{GS} = 0.05\,V$ (b) for $V_{GS} = 0.35\,V$.



(a) (b)

Figure 5.19: Total gate capacitance (C_{gg}) as a function of gate to source voltage (V_{GS}) (a) for $V_{DS} = 0.05\,V$ (b) for $V_{DS} = 0.35\,V$.

to abolish the increment of C_{gg}, which results a little variation in cutoff frequency for all cases of W_{Fin}/L_g as shown in Fig. 5.20.

The high frequency ($f_T = g_m/2\pi C_{gg}$) of operation for different W_{Fin}/L_g ratios can be observed from Fig. 5.20 (a) and (b). f_T is extracted at which the current gain is unity. A little improvement of f_T can be observed with increase in fin width. This difference in f_T is mainly due to the difference in g_m, as observed in Fig. 5.14, and due to the higher value of total capacitance (C_{gg}), as observed in Fig. 5.19. The peak point of f_T corresponds to the point between the minimum gate capacitance and peak of transconductance.

Fig. 5.21 (a) and (b) compare the output resistance (R_0) with a variation of W_{Fin} ranging from 5 nm to 20 nm at low $V_{GS}(50\,mV)$ as well as high $V_{GS}(0.35\,V)$. There is no such variation in R_0 with respect to W_{Fin}/L_g ratio observed for lower V_{GS} case. However, there is a significant variation in case of higher V_{GS} with W_{Fin}/L_g ratio. This is because of the dependency of R_0 on electric field and possibly due to bias voltage. From Fig. 5.21 (b), a low value of R_0 is observed for thicker W_{Fin} values where current crowding or electron pile-up effects are more serious. This results an improvement in drive current and transconductance as discussed under Fig. 5.14. So, FinFETs with high W_{Fin}/L_g ratio give higher g_m, but they have a poor gate control results severe SCEs (low device gain) and FinFETs with low W_{Fin}/L_g ratio predict high series resistance

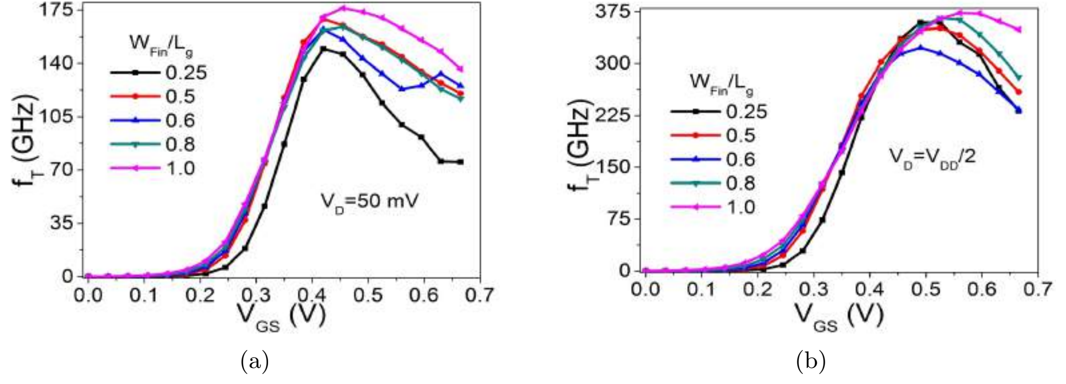


Figure 5.20: Cutoff frequency (f_T) as a function of gate to source voltage (V_{GS}) (a) for $V_{DS} = 0.05\,V$ (b) for $V_{DS} = 0.35\,V$.

which limits the achievable g_m, but a better immunity towards SCEs as it shows higher gain.

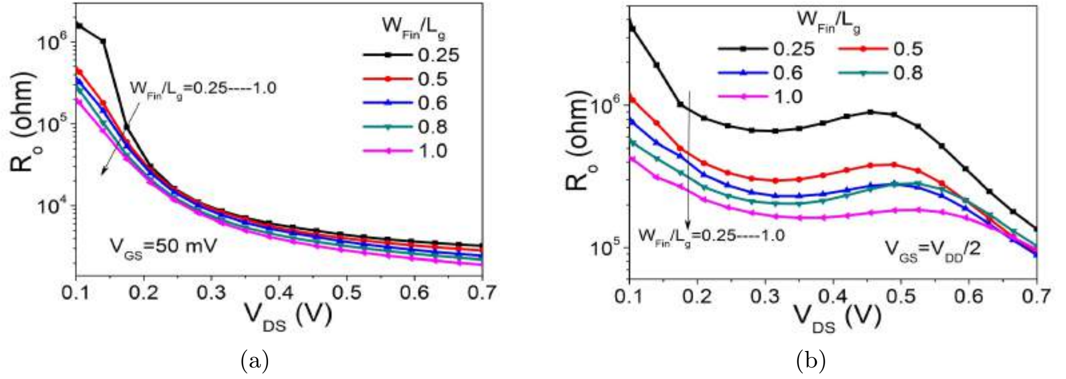


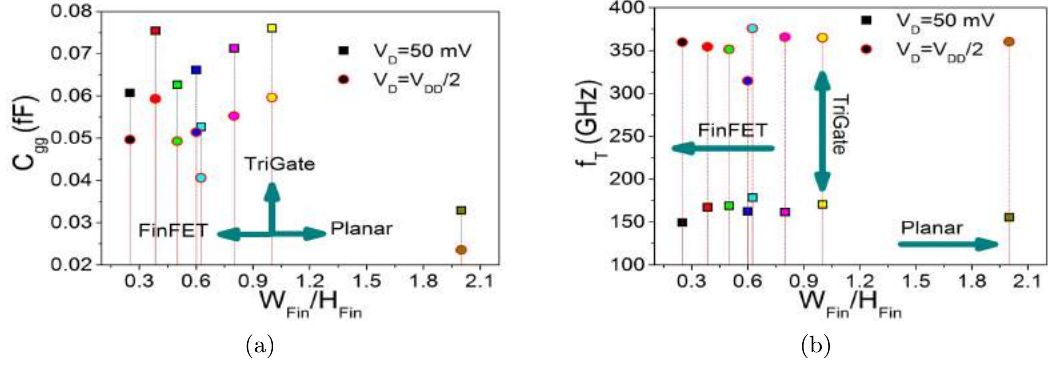
Figure 5.21: Output resistance (R_0) of the device as a function of drain to source voltage (V_{DS}) (a) for $V_{GS} = 0.05\,V$ (b) for $V_{GS} = 0.35\,V$.

Up to this, we have systematically investigated the parameter variation (W_{Fin} and H_{Fin}) effects on various device performances including DC as well as Analog/RF. From the above study, taller fins are needed for higher current drivability and also shows a little improvement in high frequency of operation whereas shorter fins are required for better SCEs. From this point of view, the aspect ratio ($AR = W_{Fin}/H_{Fin}$) of the device is a very interesting and significant parameter from FinFET design consideration point of view. However, some fabrication limitations are major concerns to achieve such taller fin heights and narrower Fin widths. The dependency of AR on intrinsic delay, power dissipation, cutoff frequency, etc. are discussed in further section.

5.1.5 Impact of Aspect Ratio

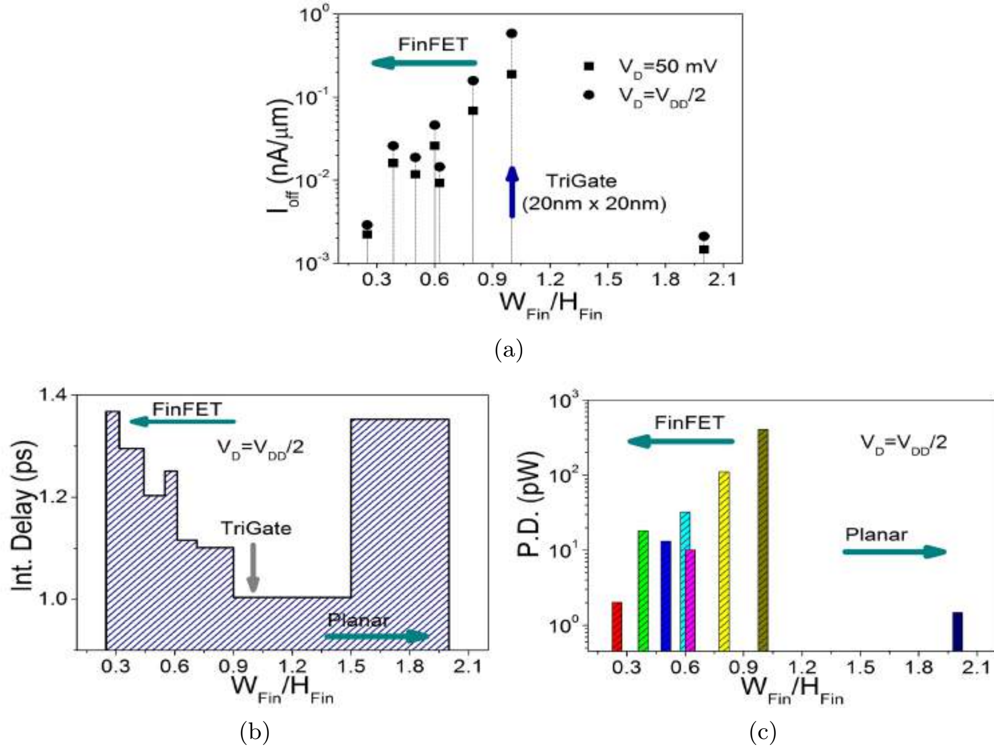
In this section, according to the AR we have distinguished the device as FinFET, Trigate, and Planar MOSFET. The device having $H_{Fin} > W_{Fin}$ (i.e. $AR < 1$) is known as FinFET, and the reverse i.e. $H_{Fin} < W_{Fin}$ ($AR > 1$) is considered as Planar, and where $H_{Fin} = W_{Fin}$ ($AR = 1$) is called Trigate [145]. The main device parameters are $L_g = 20\,nm, t_{ox} = 0.9\,nm, t_{box} = 40\,nm, t_{sub} = 70\,nm, L_{un} = 5\,nm, V_{GS} = V_{DS} = V_{DD} =$

$0.7\ V, T = 300\ K$, AR varied as (0.250, 0.385, 0.5, 0.6, 0.625, 0.8, 1.0, 2.0) [145, 147]



(a) (b)

Figure 5.22: (a) Total gate capacitance (C_{gg}) (b) Cutoff frequency (f_T) as a function of Fin aspect ratio ($AR = W_{Fin}/H_{Fin}$).



(b) (c)

Figure 5.23: (a) Drain leakage current (I_{off}) (b) Intrinsic Delay ($(C_{gg} \times V_{DD})/I_{eff}$) (c) Static power dissipation ($V_{DD} \times I_{off}$) as a function of Fin aspect ratio ($AR = W_{Fin}/H_{Fin}$).

The total gate capacitance (C_{gg}) and cutoff frequency (f_T) with a variation of AR are given in Fig. 5.22 (a) and (b) respectively. In case of Planar MOSFET i.e. for $AR > 1$, the obtained C_{gg} is reasonably low which further enhances the f_T. By comparing all different AR cases, $AR = 0.6$ gives better values for both C_{gg} and f_T.

From the circuit level design requirements, the intrinsic delay is the more important measure to be analyzed. So to minimize the intrinsic delay ($(C_{gg} \times V_{DD})/I_{eff}$), we have included the optimization of delay with respect to aspect ratio. Where Ieff is the average of drain current I_D for $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}/2$ and I_D for $V_{GS} = V_{DD}/2$ and $V_{DS} = V_{DD}$ [150]. The I_{off}, intrinsic delay, and static power dissipation ($V_{DD} \times I_{off}$)

with variation of AR ranging from 0.3 to 2 are plotted in Fig. 5.23 (a), (b) and (c) respectively. For FinFET design with $AR \approx 0.3$ and Planar design with $AR \approx 2$, the I_{off} is reduced by a larger factor as compared to other designs including the Trigate design ($AR = 1$). Similarly, intrinsic delay and power dissipation can be observed and compared with different designs (FinFET, Trigate, and Planar). The Trigate design ($AR = 1$) shows minimum delay but again maximum power dissipation as compared to its counterparts. It is due to the high I_{eff} in case of $AR = 1$. However, the FinFET design with $AR = 0.3$ and Planar with $AR = 2$ show optimum values of power dissipation.

5.2 Summary

In continuation with our previous chapters on DG-MOSFET, a unique attempt has been made to present a deep analysis of process variability dependency on various performance metrics of 3-D FinFET.In this chapter, we have addressed the Aspect Ratio ($AR = W_{Fin}/H_{Fin}$) of FinFET and its impact on the important performance measure for analog/RF circuit design. From the results, we have obtained that taller Fins are required for higher drive current and narrower Fins for immunization to SCEs.

The following technical topics and contributions are presented in this chapter:

- *Role of Fin Aspect Ratio in sub-20 nm SOI-FinFET (Chapter 5)*

  Now a days FinFETs integrated into complex circuit applications can fulfill the demand of smart phones and tablets for better performance and make chips that can compute faster. In this work a study has been made on the impact of Fin height H_{Fin} and width W_{Fin} variations on various performance matrices including static as well dynamic FoMs. The static or low frequency performances like threshold voltage (V_{th}), on current (I_{on}), off current (I_{off}), power dissipation, transconductance (g_m), output conductance (g_d), transconductance generation factor ($TGF = g_m/I_D$), early voltage (V_{EA}), gain (A_V) and dynamic or high frequency performances as gate capacitance (C_{gg}), cutoff frequency (f_T), output resistance (R_0), intrinsic delay are systematically presented with the variation of device geometry parameters.

  In case of H_{Fin} variation, $H_{Fin} = 0.6 \times L_g$ case shows the optimum device performances in terms of gain and maximum frequency of operation. By thinning the W_{Fin}, we can able to make the FinFET free from substrate related effects which further improves the A_V, V_{EA} and R_0 of the device. The Trigate ($AR = 1$) shows a tremendous improvement in delay of the device because of higher I_{eff}. However, FinFETs ($AR < 1$) and Planar MOSFETs ($AR > 1$) predict desirable improvements in power dissipation and f_T. So, the present work provides valuable results insights in the performance measures of a FinFET or Trigate or Planar MOSFET, according to the requirement for high performance (HP) or low standby power (LSTP) applications. This contribution can be of great help to device engineers in designing 3-D devices as per their requirement in circuit application.

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List of Contribution

1. D. Singh, **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Variation study of process parameters in Trigate SOI-FinFET," in *Proceedings of IEEE* 11th *INDICON ,Emerging Trends and Innovation in Technology*, Pune, India, Dec. 2014, pp. 1-4.

2. **S. K. Mohapatra**, K. P. Pradhan, D. Singh, and P. K. Sahu, "The Role of Geometry Parameters and Fin Aspect Ratio of sub-20nm SOI-FinFET: An Analysis towards Analog and RF Circuit Design," *IEEE Transactions on Nanotechnology*, vol. 14, no. 3, pp. 1-9, May. 2015.

Chapter 6

Temperature Dependence Inflection Point in SDOI (Si directly on Insulator) MOSFETs

The evaluation of ZTC/TCP is one of the key analysis for optimal device operation and reliability. The sensitivity of various DG-MOSFET and FinFET performances has been systematically analyzed towards temperature variation. From the presented outcomes of this work, it is evident that there exist different inflection points for I_D, and g_m, which should be seriously taken into consideration for nanoscale MOSFET based circuit operation.

MOSFETs are widely used in the field of military, satellite communications, medical equipment, automobile, nuclear sectors, wireless and mobile communications etc. as amplifier design, analog integrated circuits (ICs), digital CMOS design, mixed-signal ICs, power electronics and switching devices. As per the demand in a variety of applications and the use the nanoscale transistors, it is important to analyze the performances at a wide range of temperatures [151, 152]. Nowadays most of the applications made up of ICs are based on CMOS technology. The CMOS technology designed with SOI devices offer a reduction in junction capacitance, second order effects. Along with it also has the immunity to SCEs. At a high-temperature, unwanted flow of high leakage current through the well junction and presence of latch up puts a limit on the use of bulk CMOS devices. However, due to the absence of the well and latch up in SOI devices, it can be preferred for applications both at low and high-temperature [15, 153–156]. It is desirable to bias the digital, and analog circuits meant for wide temperature applications at a point where the $V-I$ characteristics show little or no variation with respect to temperature. This inflection point is typically known as temperature compensation point (TCP) or zero temperature coefficient (ZTC) [157–161]. An inflection point on the behavior of MOSFET over a wide range of temperatures (T) influences performance of both analog and digital circuits. This work is an investigation to find the point of inflection at which the temperature coefficient is zero of Ultra-Thin Si directly on Insulator (UT-SDOI) single gate (SG), double gate (DG), and gate stack double gate (GS-DG), n-MOSFET over wide range of temperatures ($100\,K - 400\,K$) through 2-D device simulation.

6.1 Back Ground Review

Previously, Shoucair [162] and Prijic *et al.* [158] have identified the ZTC point for a bulk CMOS in both linear and saturation regions for the temperature varying between 25^0C-200^0C. Groeseneken et al. [160] and Jeon, *et al.* [153] have experimentally demonstrated the existence of ZTC point for thin and thick film SOI MOSFETs respectively. Osman *et al.* [161] have presented both experimental and analytical results for the ZTC point over a wide temperature range (25^0C-300^0C) for the partially depleted (PD) SOI MOSFET. They have identified two distinct ZTC points, in the linear as well as saturation region. Tan *et al.* [163] have analyzed the fully depleted (FD) and lightly doped enhanced SOI n-MOSFET over a wide range of operating temperatures ($300\,K - 600\,K$). They have identified in both linear and saturation region. In contrary, exists only in the saturation region.

The Double Gate (DG) MOSFET fabricated on SOI wafers is one of the most promising candidate due to its attractive features of low leakage current, high drive current (I_{on}), transconductance (g_m), reduced SCEs, steeper sub-threshold slopes, and suppression of latch-up phenomenon [37, 104–106]. It also offers a excellent option for analog and RF applications [77, 80]. In chapter 4 , a detailed investigation on the role of high-k gate dielectric in DG MOSFET considering both single layer and gate stack configurations has been presented with the aim to optimize the high-k gate dielectric.

Also, the role of asymmetric channel doping like single halo (SH) and double halo (DH) on various performance metrics of DG MOSFET has been studied. So far, insufficient works have been reported in the literature for further investigation on ZTC point for the multi-gate technology.

6.1.1 Zero-Temperature-Coefficient (ZTC) point

There are two ZTC points for a transistor, one for the drain current and the other for the transconductance, and in general they have different values in linear and saturation regions. These ZTC points are defined as the points at which the drain current or the transconductance remains constant and independent of temperature. The ZTC points, are values of V_{GS} at which the reduction of the threshold voltage is counter-balanced by the reduction of the mobility, and as a result, the value of the drain current or the value of the transconductance remains constant as the temperature varies. For gate voltages lower than ZTC, the decrease of threshold voltage is dominant, as a matter of fact drain current increases with temperature, while for gate voltages higher than ZTC, the mobility degradation predominates and drain current decreases with temperature. The ZTC is asignificantÂăbias point for analog designers as it corresponds to a gate voltage at which the device DC performance remains constant with temperature

ZTC biasing is one of the important techniques in high-temperature design especially for an operational transconductance amplifier (OTA). The principal advantages of ZTC technique are [164]:

- It maintains a constant operating point over a wide range of temperatures so that no transistors operate out of saturation.
- It ensures the stability of the circuit over a wide range of temperatures.
- Design simplicity and ensures reliable circuit operation when several stages are used.

It provides a bias point that is temperature independent. The main disadvantages of ZTC are high overdrive voltage associated with ZTC bias results in reduced intrinsic gain due to the small g_m as well as reduced signal swing. The reduced g_m with temperature can affect the small signal performances of the amplifier like gain, bandwidth, etc., especially when the amplifier is required to operate over a wide range of temperatures.

In general, the behavior of drain current (I_D) is exactly opposite before and after an individual bias voltage with variation in temperature. The dependence of I_D on temperature is due to the mobility and high field effect by virtue of applied bias voltage [87, 163]. There always exists the need to have a thorough investigation of the performance for analog/RF applications at a wide range of temperature [152, 165]. To the best of our knowledge, this is probably the recent approach for investigating a detailed analysis of ZTC point to examine its reliability issues over a wide temperature range ($100\ K - 400\ K$) as far as both analog and RF applications of a DG MOSFET

with high-k metal gate (HKMG) technology is concerned. Performance comparison is made between SG, DG, and GS-DG in UT-SDOI n-MOSFETs.

6.2 Device Description and Simulation Setup for GS-DG MOSFET

The schematic diagram of three different structures UT-SDOI SG, DG, and GS-DG n-MOSFETs are shown in Fig. 6.1. The physical dimensions of the structures are adopted

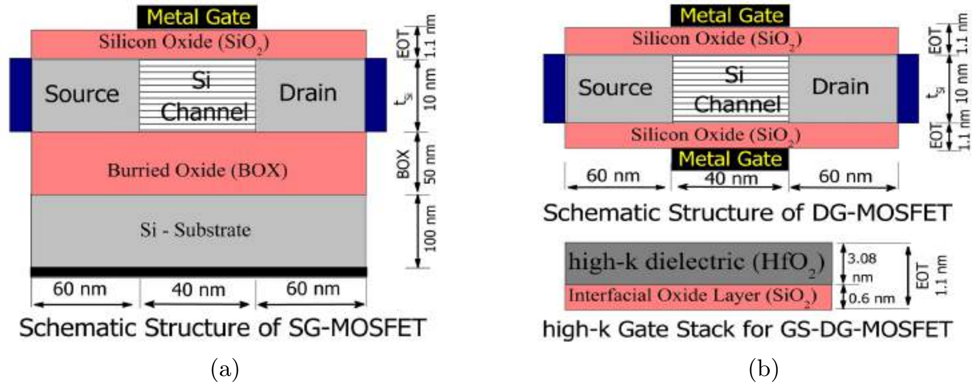


Figure 6.1: Schematic diagram of the simulated devices (a) Single Gate (SG), (b) Double Gate (DG) and Gate Stack Double Gate (GS-DG), UT-SDOI n-MOSFET

with the following specifications. The effective oxide thickness (EOT) is 1.1 nm, the silicon body thickness (t_{Si}) is $10\,nm$, the channel length (L_g) is $40\,nm$ with a fixed width of $1\,\mu m$, the source and drain extensions are of $60\,nm$ each with contacts vertically placed (S and D, respectively). Metal gate technology is preferred in high-k dielectrics because it solve the Fermi level pinning, screening of surface phonon based vibrations eliminate the poly-Si gate depletion effect and the associated degradation in transistor performance as reported Wilk *et al.* [166] and Chau *et al.* [115,167]. Hence, a metal gate work function is tuned between $4.6\,eV$ to $4.8\,eV$ for maintaining a constant threshold voltage of $0.375\,V$ at room temperature [37,106]. Molybdenum (Mo) is a candidate for gate material in FD-SOI CMOS technology, because it is compatible with a standard CMOS process flow and its work function can be adjusted within the desired range $(4.5-5.0\ eV)$ via nitrogen implantation as reported Ha *et al.* [168]. The undoped channel [169] (p-type $\approxeq 1\times 10^{16}\,cm^3$) for avoiding threshold voltage variation and highly doped source, drain (n-type $\approxeq 1\times10^{20}cm^3$) are set to reduce the effect of mobility degradation by coulombs scattering. The structures are calibrated to meet the requirement of international technology road map for semiconductors (ITRS) [7] for 45 nm technology node. According to ITRS, the drain bias has been fixed at $V_{DD} = 1.0\,V$. To study the analog performance, simulation is carried out with drain to source voltage $V_{DS} = 0.5\ V$ (which is half of the supply voltage i.e., $V_{DD}/2$) [129] with a variable gate to source voltage $V_{GS} = 0\ V$ to $1.0\,V$. Threshold voltage (V_{th}) is extracted using constant current ($I_D = 10^{-6}\,A/\mu m$) definition from the $I_D - V_{GS}$ transfer characteristic.

6.2.1 Consideration of Trapped Charges

During the pre and post-fabrication process, availability of the trapped charges are quite common and cannot be neglected in nanoscale devices. Subsequently the effect has been considered in the simulation. The trapped charges are closely connected to insulating layer in MOSFET. The property of insulator directly controls them. The presence of trapped charges creates an additional non-linear potential and a varying electric field across the gate dielectric. The high-k gate stack reduces the electric field across the layer of gate stack due to high permittivity. So a lower electric field will be required to induce the inversion layer charge as Eq. 6.1 [87]

$$Q_{ch} = \varepsilon_{di}\mathrm{E}_i \tag{6.1}$$

Where Q_{ch} is inversion charge, ε_{di} is the permittivity of dielectric and Ei is electric field. Even if, trapped charge densities are enormous, it requires moderate potential across the high-k gate stack layer. Consequently, the reduction of the threshold voltage and supply voltages are maintained. This low electric field promote gate stack reliability with huge unwanted charges inside. In 45 nm technology node and beyond the high-k dielectrics (mostly HfO_2) are used in gate stacks to achieve the low equivalent oxide thickness (EOT) to reduce gate leakage current, threshold voltage and supply voltages [7]. However, one of the key issues is the process induced defect that degrades device mobility resulting in poor performance and reliability [108, 113]. So in this simulation, interface trapped charge density is considered at a semiconductor-insulator interface for SG to be $1 \times 10^{10} cm^{-2}$ and for GS-DG is $4 \times 10^{11} cm^{-2}$. The typical concentration of trapped charge density ranges between $10^{10} cm^{-2}$ to $10^{11} cm^{-2}$ in thin interface layer as reported Castan *et al.* [170]. The electron and hole surface recombination velocity considered as $1 \times 10^4\ cm/sec$. In this simulation, all the junctions of the structures are assumed as abrupt, and the doping profiles are uniform.

The variation of relevant performance metrics for the devices as a function of temperature are addressed in following subsections. The on-state drive current (I_{on}), off-state leakage current (I_{off}), I_{on}/I_{off} ratio, subthreshold slope (SS) are the few important characterization parameters related to device scalability. As far as analog circuits are concerned, the parameters like the transconductance (g_m), output conductance (g_d), intrinsic gain (A_V), Q-factor play a prior role. Similarly cutoff frequency (f_T), delay, EDP and sweet spot [171] are the most important parameters for evaluating the RF performance of the device.

6.2.2 Static Performance Measure

As temperature increases, the mobility of carrier's decreases due to scattering effects which further reduces the I_{on} as shown in Fig. 6.2 (a). However, it can be observed that DG configurations predict a significant improvement in I_{on}. Because of the high current drivability, DG MOSFETs are highly demanded in the semiconductor industry. Again the degradation in I_{off} at high temperatures can be visible from Fig. 6.2 (b). It is due to the lattice vibration, and phonon scattering phenomena play a significant role

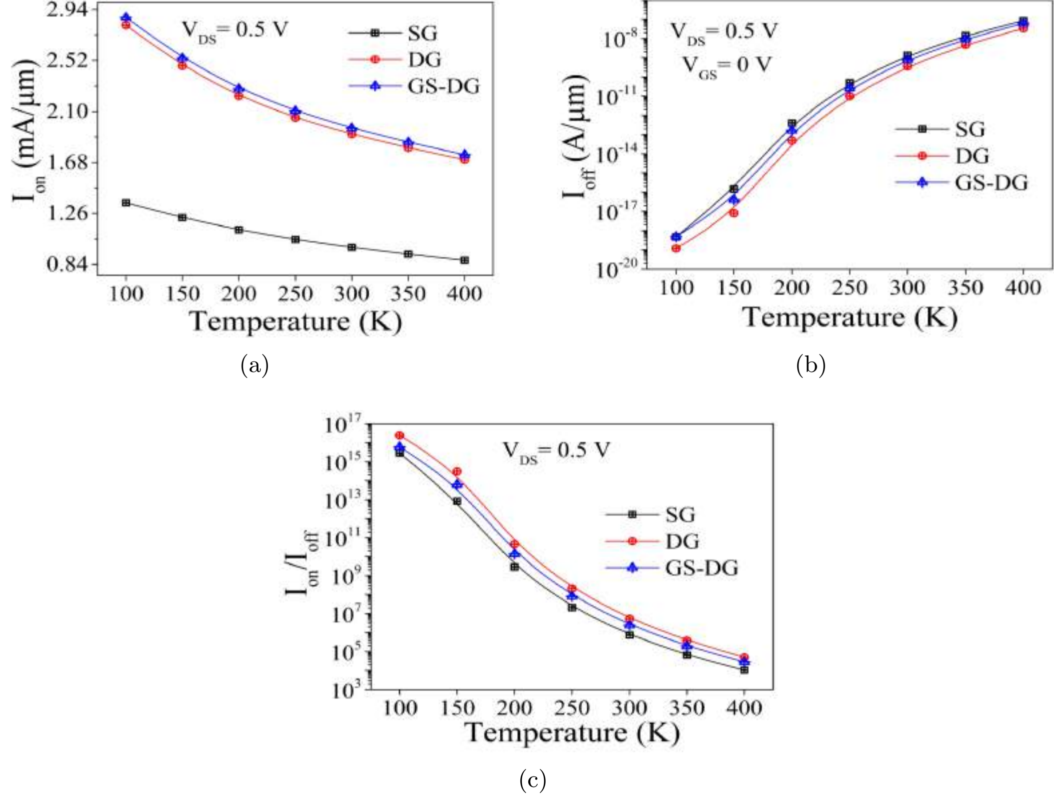


Figure 6.2: (a) On state current (I_{on}), (b) Off state current (I_{off}), (c) on-off current ratio (I_{on}/I_{off}) as a function of temperature for SG, DG, and GS-DG, UT-SDOI-MOSFETs.

as T increases. The I_{on}/I_{off} ratio is an important parameter for switching applications. It should be marginally high for a good switch. The off-current is significantly reduced by DG device structures as compared to its counterpart SG as shown in Fig. 6.2 (b). Similarly, because of improved carrier transport efficiency and low leakage current, the DG configurations provides higher on-current as inclined in Fig. 6.2 (a). From Fig. 6.2 (c), it is clear that the on-off current ratio is much higher in DG configuration cases as compared to SG case. It can also be observed that I_{on}/I_{off} decreases with increase in temperature. The I_{off} shows a very low value for $T < 200\,K$ and starts increasing as temperature increases beyond $200\,K$. This is due to low SS (refer Fig. 6.4) and high V_{th} values at low temperatures. The temperature dependency of the I_D is influenced by V_{th} as [163].

$$I_D(T) \approx \mu\,(T)\,[V_{GS} - V_{th}\,(T)] \tag{6.2}$$

The mobility term (which is hampered due to scattering effects at high T) of Eq. 6.2 forces I_D to decrease, whereas the $[V_{GS} - V_{th}]$ term (improves at higher T as V_{th} decreases) increases I_D with increase in temperature. But the behavior of I_D with T shows just adverse response at a fixed gate bias voltage. The effects of two controlling terms of Eq. 6.2 are nullified at a fixed value of bias voltage, that inflection point is called as temperature compensation point (TCP).

Fig. 6.3 (a) & (b) shows the variations of I_D and g_m with V_{GS} at different bias temperatures. As per Eq. 6.2 at high gate bias,$\mu(T)$ dominates because of the heavy

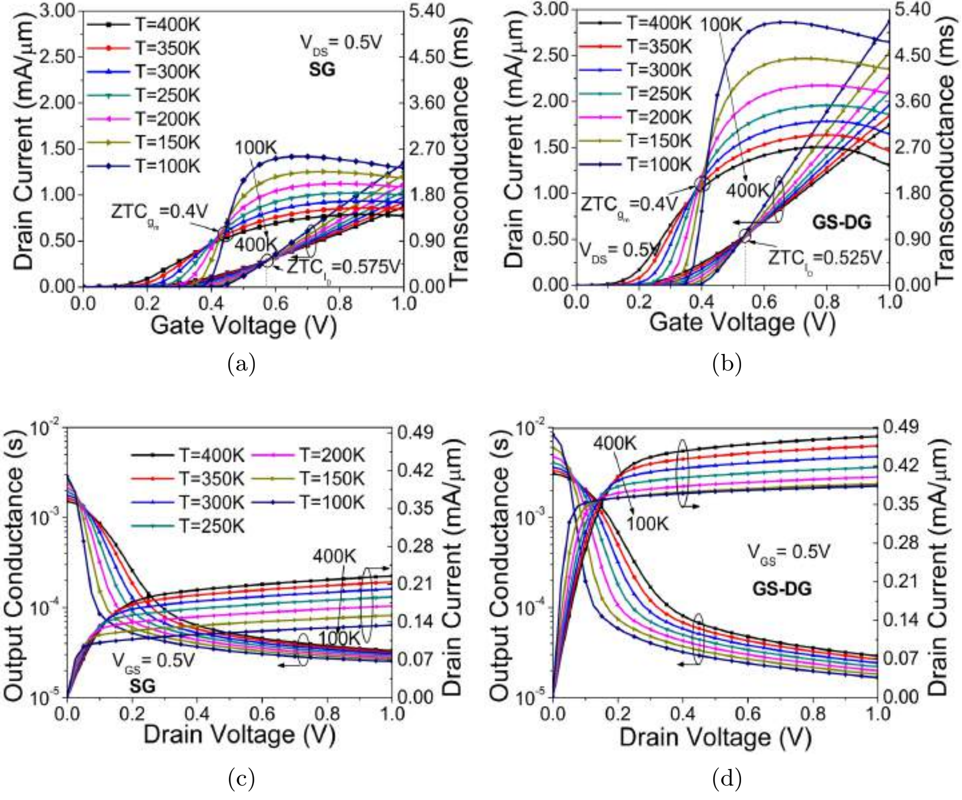


Figure 6.3: Drain current (I_D) and Transconductance (g_m) as a function of V_{GS}, Output current (I_D) and Output conductance (g_d) as a function of V_{DS}, with variation of temperature for (a) & (c) SG, (b) & (d) GS-DG, UT-SDOI-MOSFETs.

lattice scattering at higher T. It leads to a reduction in the channel mobility which further reduces I_D. At low gate bias, term influences I_D to raise because of the shrinking nature of V_{th} with an increase in T. These two opposite effects cancel out each other at a value of V_{GS} where I_D shows minimal fluctuation with T. This inflection point as shown in Fig. 6.3 (a) & (b) is imminent in between $V_{GS} = 0.5\,V$ to $0.6\,V$ for all device cases. The DG configurations exhibit higher drive current as compared to SG. ItÂăcreates an opportunity to use multigate MOSFETs for integrated circuit applications.

At $V_{GS} < V_{th}$, the channel is weakly inverted and I_D is due to diffusion. The diffusion current increases with T because of increase in intrinsic carrier concentration as per the Einstein's relation: $D = \mu k_B T$, where D is the diffusion constant, μ stands for mobility, kB is Boltzmann's constant and T represents the temperature. At $V_{GS} > V_{th}$, the value of g_m decreases with T due to the mobility degradation. The reduction in V_{th} with temperature enhances g_m, however the degradation of mobility reduces g_m. These two phenomena take care of each other to give rise a temperature compensation point for g_m. From the figure, we can conclude that the value of transconductance ZTC point $(0.4\,V)$ is lower than the drain current ZTC bias point $(0.552\,V)$. The inflection point for I_D and g_m are two important FoM in analog circuit design for both high and low-temperature applications. In OPAMP (operational amplifier) based circuit design and transistors used in biasing string can be biased at the inflection point for drain current

to maintain a constant DC level. The input devices may be biased at the inflection point for transconductance to achieve stable circuit parameters. The above said points are obtained for constant bias conditions in case of floating body or body tied configuration MOSFETs. Hence, there is only one possibility to bias the transistor i.e. either at the inflection point for I_D or gm. Moreover, this point is usually affected by process variations. Hence, depending upon the nature of applications, the bias conditions are picked accordingly. The simulated output current (I_D) and output conductance (g_d) versus drain bias (V_{DS}) at a $V_{GS} = 0.5\,V$ for different T are plotted in Fig. 6.3 (c) & (d). Because of the aforementioned effects of $\mu(T)$ and V_{th} with respect to T, the inflection point can be observed in the figure.

The subthreshold Slope (SS) is the important parameter for calculating the off state current. Furthermore, SS is calculated as Eq. 6.3 [28, 87]:

$$SS\,(mV/dec) = \frac{\partial V_{GS}}{\partial\,(\log I_D)} \tag{6.3}$$

$$I_D \alpha \exp\left(qV_{GS}/\eta kT\right) \tag{6.4}$$

I_D is the drain current, V_{GS} is the gate voltage, q is the charge of electron, k is the Boltzmann's constant, η is the body factor and T is the temperature. At room temperature (300 K) and ideal condition ($\eta = 1$), the function changes by 10 for every 60 mV change in V_{GS}. The ideal value for the SS is 60 $mV/decade$. Also the SS can be related to temperature as Eq. 6.5 [28]

$$SS\,(mV/dec) \approx 60mV\frac{T}{300K} \tag{6.5}$$

According to above relation, SS will vary according to T. From the extracted values of

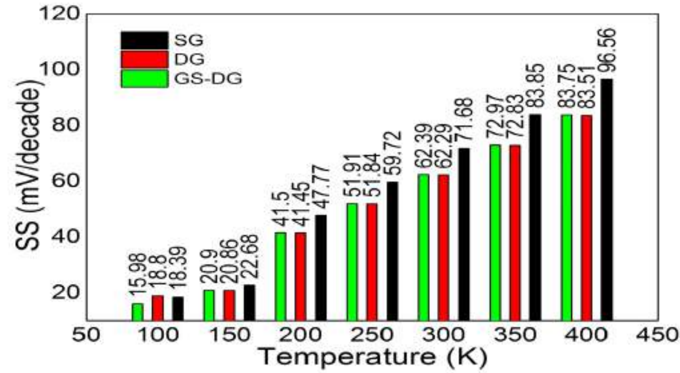


Figure 6.4: Variation of Subthreshold slope (SS) as a function of temperature.

SS which is shown in Fig. 6.4, one can validate Eq. 6.5. As the temperature increases from 300 K, the SS values are rapidly increasing which degrades the device performance. By comparing the SS values between SG and DG configurations, at 300 K, the SG device shows 71.68 $mV/decade$ whereas the DG devices show 62 $mV/decade$ that is near to the ideal value.

6.2.3 Analog/RF FoMs

The intrinsic capacitances (C_{gs} and C_{gd}) during the inversion region is due to the depletion charge encompassing near the drain and source respectively. These charges

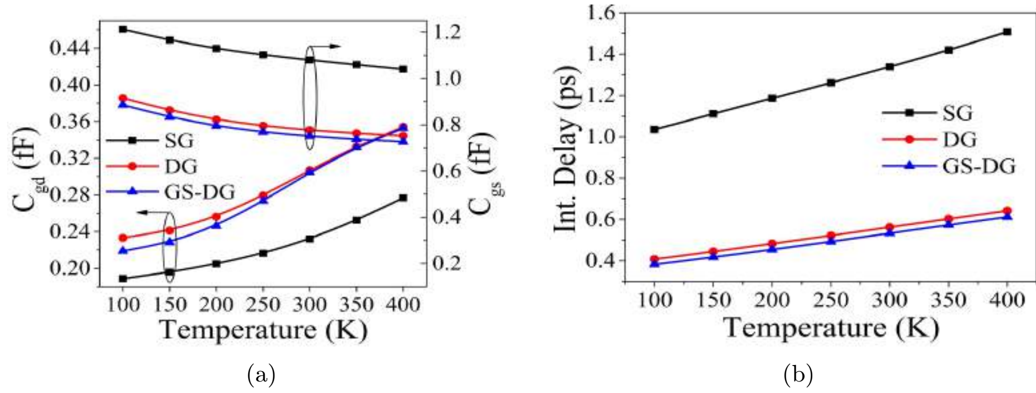


Figure 6.5: Variation of (a) C_{gs} and C_{gd}, (b) Intrinsic delay as a function of temperature.

are depending on the junction width, temperature and applied bias. It can be observed from the Fig. 6.5 (a), C_{gs} decreases with rise in T, however C_{gd} shows a reverse phenomenon. In case of C_{gd}, the parameter starts to increase gradually with a raise in T and obtain its supreme amount at $T = 400\ K$. The sensitivity of intrinsic delay ($\tau = CV/I$) on T conceivably noticed from Fig. 6.5 (b). Significant degradation in τ is observed for higher T is because of the larger values of intrinsic capacitances. Furthermore, SG device more delays as compared to DG configurations, which affect the speed of the device. ItÂăis due to the lower drive current (I_D) and higher C_{gs} in case of SG case.

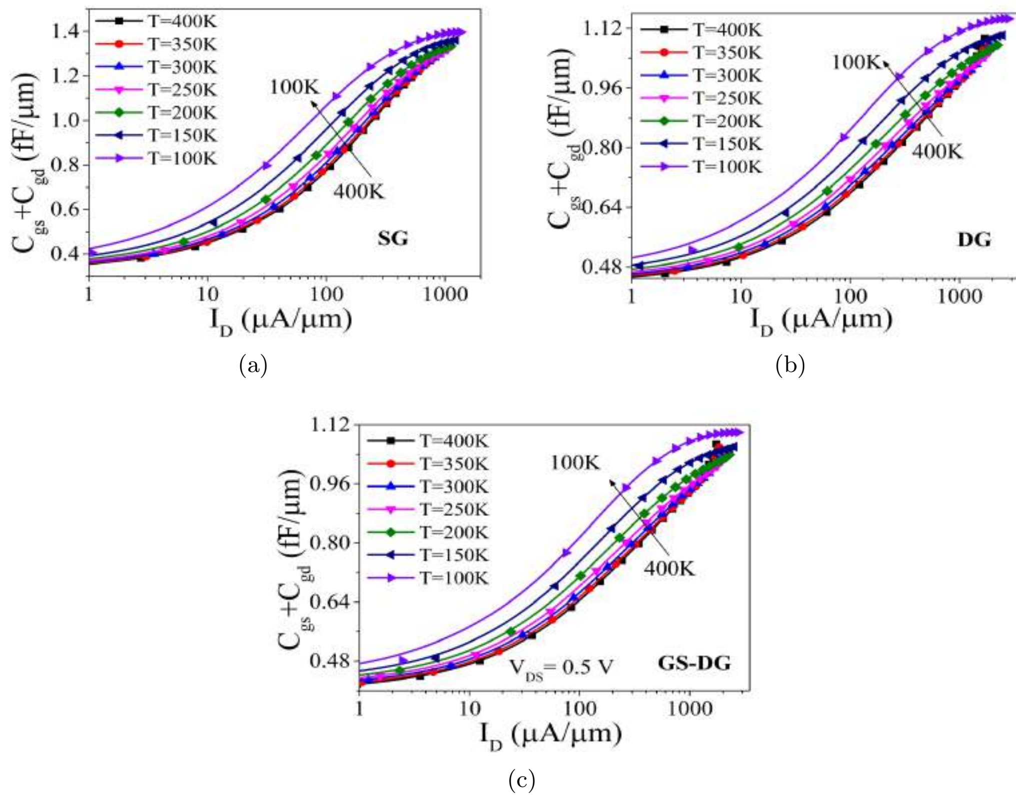


Figure 6.6: Total Capacitance ($C_{gs} + C_{gd}$) as a function of I_D with different values operating temperatures for (a) SG, (b) DG, and (c) GS-DG, UT-SDOI-MOSFETs.

Fig. 6.6 discussed the total capacitance $(C_{gs}+C_{gd})$ as a function of I_D with variation in T. This parameter is required to evaluate the cut-off frequency (f_T) of the devices. The hike in $(C_{gs}+C_{gd})$ occurs with reduction in T.

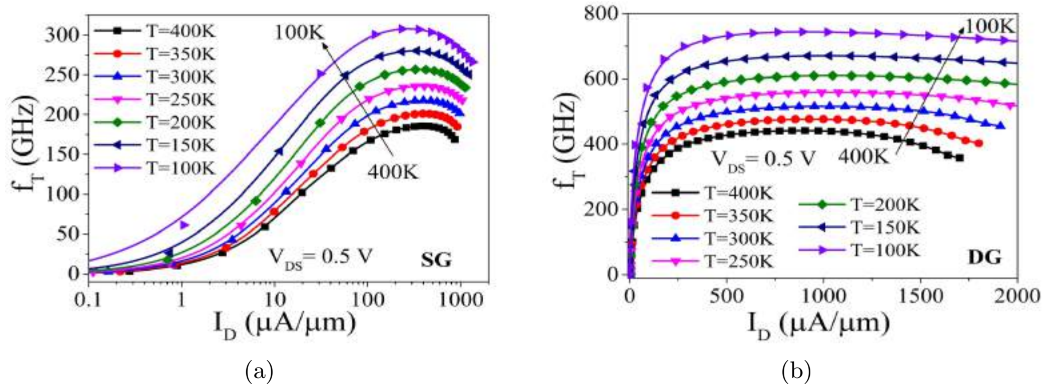


Figure 6.7: Cut off Frequency (f_T) as a function of I_D with different values operating temperatures for (a) single gate and (b) double gate device.

The enhancement in f_T occurs at higher drive current and lower T values in Fig. 6.7. This improvement in f_T is partially due to the increment in gm and merely because of the low values of intrinsic capacitances. From the Fig. 6.7, we can also claim that DG configuration is deserving candidates for RF applications compared to SG device as these devices give higher f_T. Fig. 6.8 describes the dependency of intrinsic gain (A_V)

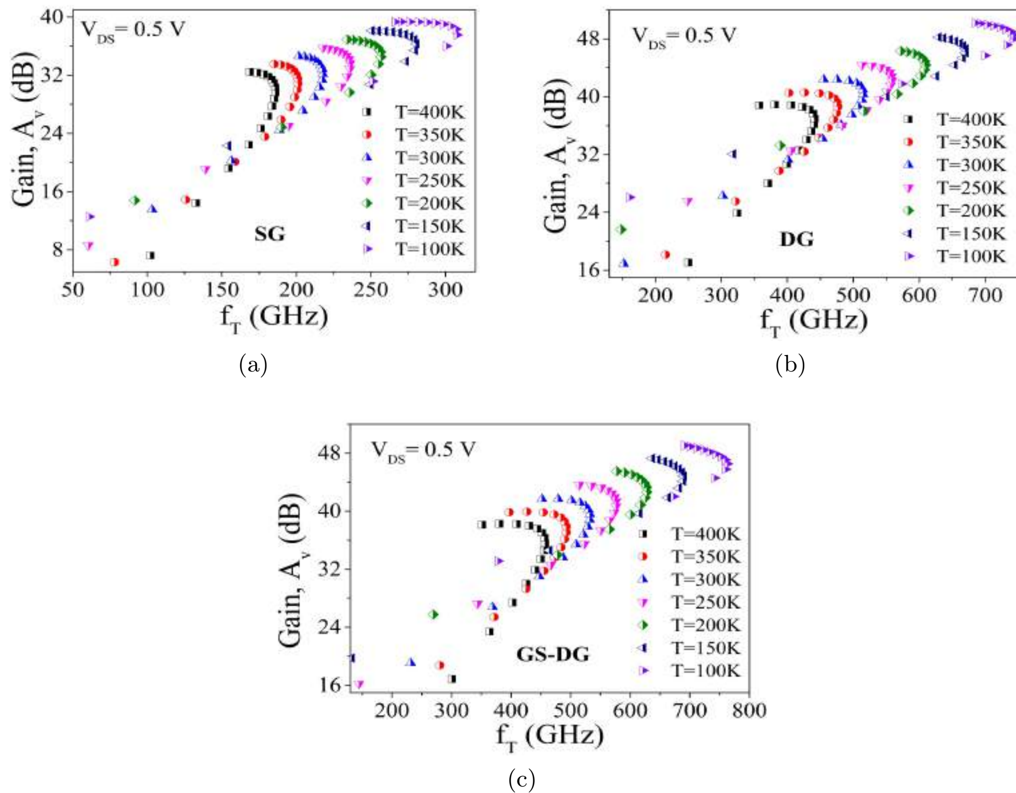


Figure 6.8: Intrinsic Gain (A_V) as a function of Cutoff Frequency (f_T) for all the devices under study with different values operating temperatures.

on cut-off frequency (f_T) with variation in T for SG and DG devices. It can be observed that A_V increases with the increase in T. High gain can be obtained for high temperature as observed in Fig. 6.8. From the Fig. 6.8 (a), it has been observed that performance wise DG devices are superior compared SG device under similar conditions. From the same plot, it is shown that the gain of DG devices are about 50 dB compared to 40 dB in case of SG device at the temperature 400 K.

The crucial parameters for RF performances i.e the maximum achievable f_T and $(g_m/I_D)\times f_T$ which is nothing but the 'sweet spot' of the device are analyzed in the Table 6.1. From the observations, authors claim that the proposed devices show impressive results in the desired temperature ranges. The f_T and sweet spot of the device increases as temperature decreases and attains their maximum values for $T = 100\ K$.

Table 6.1: Key high frequency circuit parameters for various temperatures

Temperature	**Peak cutoff frequency** (GHz)			**Sweet spot** (GHz)		
in K	**SG**	**DG**	**GS-DG**	**SG**	**DG**	**GS-DG**
400	185.80	441.27	456.79	301.99	707.64	709.00
350	201.15	476.62	492.92	336.51	787.06	786.19
300	217.78	515.18	532.34	373.93	874.14	870.62
250	236.06	558.66	576.54	415.09	971.96	965.11
200	256.67	609.40	627.82	461.98	1084.64	1074.46
150	280.35	670.48	689.53	516.96	1218.45	1206.54
100	307.88	743.23	762.86	583.91	1378.91	1367.80

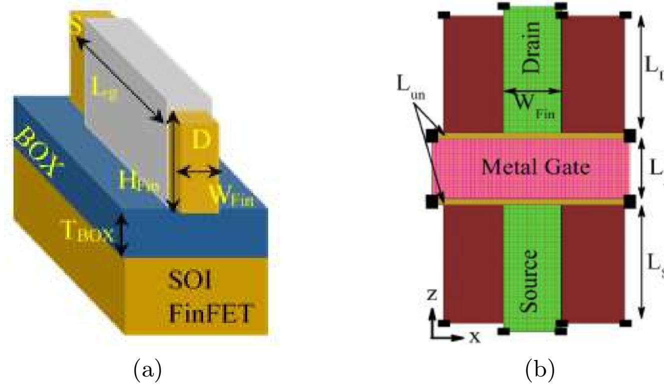
6.3 Modeling and Simulation Setup for SOI-FinFET

The geometrical process parameters of FinFETs are:

- Gate length (L_g): the physical gate length of FinFETs.
- Fin height (H_{Fin}): the height of silicon fin.
- Fin width (W_{Fin}): the width of silicon fin.
- Gate oxide thickness (T_{ox}): the thickness of the gate oxide.
- Underlap channel length (L_{un}): the region under Si_3N_4 spacer.

Among all the parameters the H_{Fin} and WFin are the two which play a major role to be investigated. A tradeoff is required between the wider fin which results in unacceptable SCEs and narrower increases parasitic resistance and is hard to manufacture. Similarly from the manufacturing point of view, a taller fin achieves a better layout efficiency and higher current. So we have adopted various design parameters like W_{Fin}/L_g = 0.25, 0.5, 0.6, 0.8, 1 and H_{Fin}/L_g = 0.25, 0.6, 0.8, 1, 1.1, 1.3 in our simulation [135, 137, 172]. An n-channel MOSFET, having interfacial oxide as SiO_2 with high-k material (Si_3N_4) as spacer in the underlap regions (L_{un}) is modeled. The L_{un} is considered as 5 nm from both sides of the channel towards source and drain side. Fig. 6.9(a) and (b) show a 3-D, as well as 2-D cross sectional view of the FinFET with Source/Drain length (L_S/L_D)

as 40 nm. The source drain doping is Gaussian in nature with peak N_D at a density of $10^{20} cm^{-3}$. The Equivalent Oxide Thickness (EOT) is 0.9 nm [134, 138] and supply voltage $V_{DD} = 0.7\,V$. The work function for the gate electrode is assumed to be 4.5 eV. The channel is undoped which augments the effective mobility, and hence the current density from the source [136].



(a) (b)

Figure 6.9: (a) Perspective 3-D (b) 2-D cross-sectional view of SOI FinFET

6.3.1 Effect of H_{Fin} and W_{Fin} on Scalability

From Fig. 6.10(a), as H_{Fin}/L_g ratio increases, there is a lofty leakage current observed but with this SS also increases. However, with the same (high H_{Fin}/L_g ratio), parasitic resistance problem can be avoided, which further increases the drain current. Similarly, Fig. 6.10 (b) demonstrates that the leakage current can be significantly reduced for lower W_{Fin}/L_g ratio cases. It is because by picking a smaller W_{Fin}, we can minimize the longitudinal electric field at the source side because of the precincts of multiple gates. From both figures, it can be noticed that SS augments with the increment in both ratios, i.e. H_{Fin}/L_g and W_{Fin}/L_g, although its value is very close to the ideal one, i.e. 60 $mV/decade$.

The I_{on} and I_{off} are very much dependent on vital device geometry parameters, i.e. H_{Fin} and W_{Fin}. So, there is always an accord between I_{on} and I_{off} for the device design and device engineers can choose the optimum parameter dimensions as their requirement for specific applications.

This is to confirm that for high drive current with matching the current drivability, taller fins are required, whereas narrow fins give better SCE immunity. This is because an increase in H_{Fin} results in decrease of the electric field in the silicon region which enhances carrier mobility and further the on state current. By comparing I_{on} and I_{off} for all H_{Fin}/L_g cases, we can say that $H_{Fin} = 0.6 \times L_g$ is the optimum one as it endues a moderate value for both I_{on} and I_{off}. Fig. 6.10 (c) discussed the same I_{on} versus I_{off} benchmark for different W_{Fin}/L_g ratios. From the figure, a wider fin width ($W_{Fin} = 1 \times L_g$) gives unacceptable SCEs, whereas a narrower fin width ($W_{Fin} = 0.2 \times L_g$) is more difficult to fabricate. So, we can take the moderate one, i.e. $W_{Fin} = 0.6 \times L_g$ as the optimized W_{Fin}/L_g ratio.

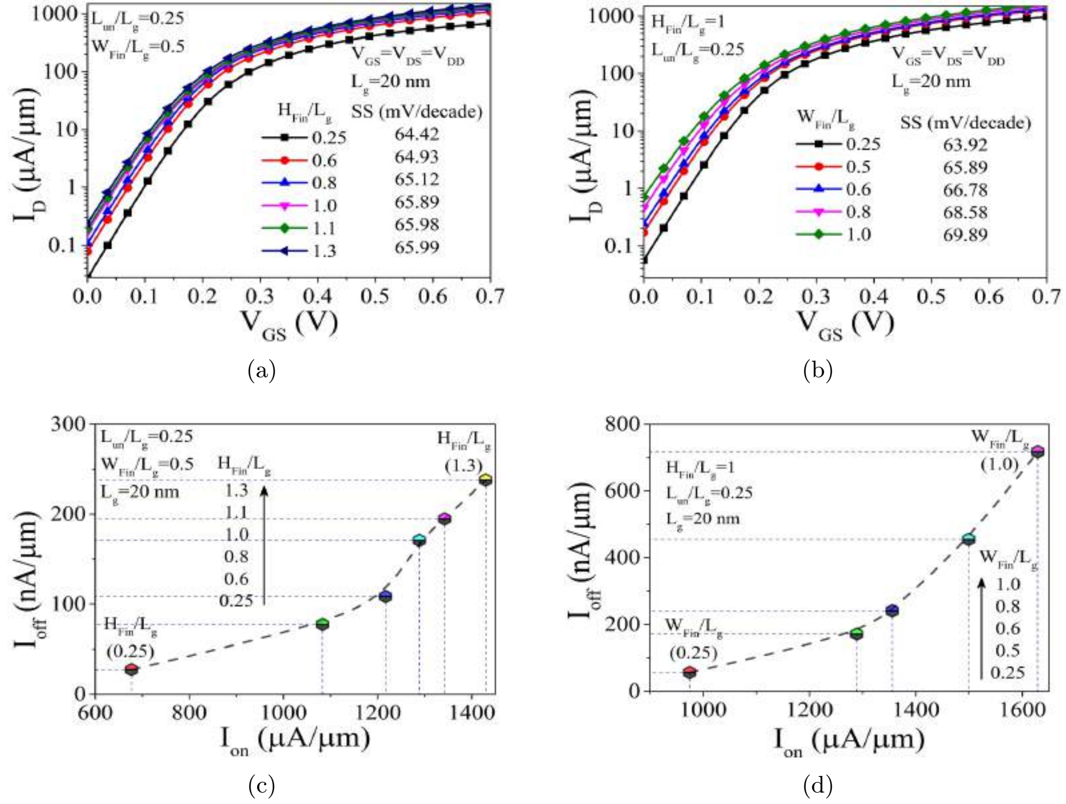


Figure 6.10: Drain current (I_D) of the device in log scale as a function of V_{GS} with variability of process parameter (a) H_{Fin} (b) W_{Fin}. On current (I_{on}) and leakage current (I_{off}) with variation of (c) H_{Fin} (d) W_{Fin} at $V_{GS} = V_{DS} = V_{DD}$.

6.3.2 Analog/RF performance with variation of Temperature

Fig. 6.11 (a) is imminent in between $V_{GS} = 0.34\ V$. It creates an opportunity to use multigate MOSFETs for integrated circuit applications. Fig. 6.11 (b) presents a plot for the important parameters which includes the variation of Ion, I_{off} for different temperatures. From the figure, it can be observed that the behaviour of I_{on} and I_{off} is opposite to each other with temperature variation. For high T values, the device shows a fairly large I_{off} and low I_{on}, which is just reverse in the case of low T. It is because, as temperature increases, the mobility of carrier's decreases due to scattering effects that further reduce I_{on}. Again the degradation in I_{off} at high temperatures is due to the lattice vibration, and the phonon scattering phenomena play a significant role as T increases.

From Fig. 6.12 (a), we can conclude that the value of transconductance ZTC point (0.14 V) is lower than the drain current ZTC bias point (0.34 V). The inflection point for I_D and g_m are two important FoM in analog circuit design for both high and low-temperature applications. In OPAMP (operational amplifier) based circuit design and transistors used in biasing string can be biased at an inflection point for drain current to maintain a constant DC level. The input devices may be biased at an inflection point for transconductance to achieve stable circuit parameters. The above said points are obtained for constant bias conditions in the case of floating body or

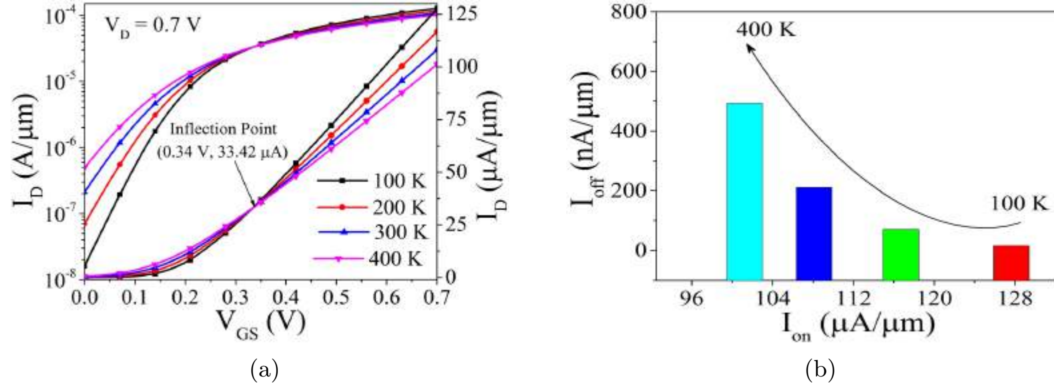


Figure 6.11: (a) Drain current (I_D) as function of Gate Voltage (V_{GS}) both in linear and log scale (b) leakage current (I_{off}) versus on current (I_{on}) with variation of temperature.

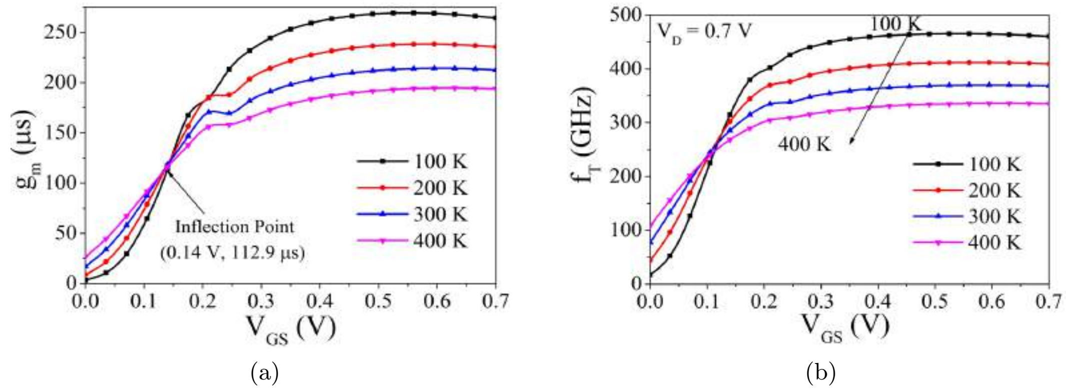


Figure 6.12: (a) Transconductance (g_m) and (b) Cut off frequency (f_T) as a function of Gate Voltage (V_{GS}) with variation of temperature.

body tied configuration MOSFETs. Hence, there is only one possibility to bias the transistor, i.e. either at an inflection point for I_D or g_m. Moreover, this point is usually affected by process variations. Hence, depending upon the nature of applications, the bias conditions are picked accordingly. The enhancement in f_T occurs at higher drive current and lower T values. This improvement in f_T is partially due to the increment in gm and merely because of the low values of intrinsic capacitance. At low temperature, the growth of cut-off frequency f_T is due to a steep increase in mobility and in turn g_m shown in Fig. 6.12 (b).

From the Fig. 6.13 (a), a high gain can be obtained for high temperatures in the subthreshold region and the reverse effect in the superthreshold region. Fig. 6.13 (b) presents one crucial parameter for analog/RF application, i.e. the 'sweet spot' (settlement among power, speed of operation and linearity), which is signified by the peak of transconductance to the current ratio (g_m/I_D) and cut-off frequency (f_T) product. The variation of the 'sweet spot' with I_D for a broad range of T (100 K to 400 K) is well examined from Fig. 6.13 (b). The device predicts pretty higher $g_m \times f_T/I_D$ values at low T and gradually starts decaying with the increase in T.

The extracted static parameters like I_{on}, I_{off}, I_{on}/I_{off}, and power dissipation ($PD = I_{off} \times V_{DD}$) for a wide range of T variation are arranged in Table 6.2. All the parameters

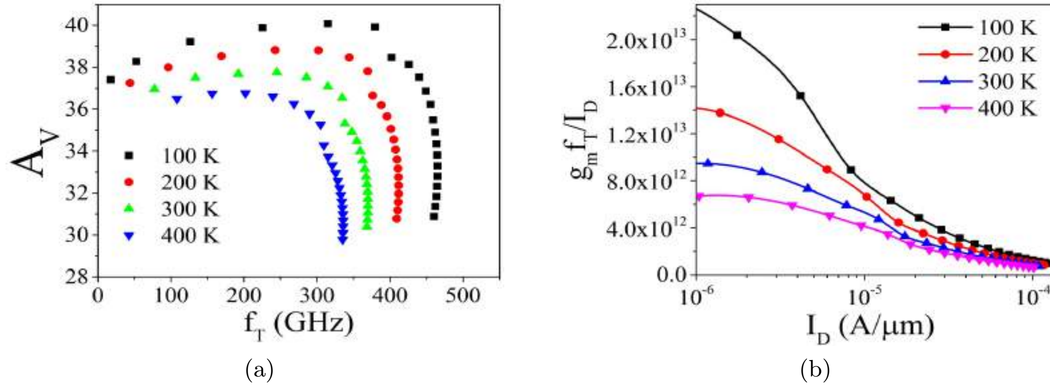


Figure 6.13: (a) Intrinsic Gain (A_V) versus Cut off frequency (f_T) (b) Sweet Spot as a function of Drain Current (I_D) with variation of temperature.

Table 6.2: Static performance of FinFET with T variation

Temp. (K)	I_{on} (μA)	I_{off} (nA)	I_{on}/I_{off}	$PD(I_{off} \times V_{DD})(W) \times 10^{-8}$
100	128	16.03	7961.96	1.122
200	117	69.83	1670.96	4.888
300	108	211.01	512.33	14.77
400	101	492.53	205.52	34.47

predict significant improvements in the lower range of T values. The performances start deteriorating as T increases. With reference to temperature 300 K the deteriorated parameters are I_{off} by 77.04%, on-off ratio by 79.01%, and 77.04% in P_D, while T steps up. Table 6.3 reveals the dynamic analysis of FinFET towards temperature sensitivity. The performances like f_T, "sweet spot", energy, and EDP are exported and compared for different temperatures. Alike the above discussed static performances, the dynamic parameters are also depict numerous enhancements at detrimental temperatures.

Table 6.3: AC/Dynamic performance of FinFET for different values of T

Temp. (K)	$C_{gg}(F)$ $\times 10^{-18}$	Peak f_T (GHz)	Sweet Spot (THz/V)	Delay (CV/I_{eff})(ps)	Energy $(CV^2)(J)$ $\times 10^{-18}$	EDP (Js) $\times 10^{-29}$
100	92.236	465	23.5	0.506	45.195	2.29
200	92.178	412	13.8	0.553	45.167	2.5
300	92.217	370	9.47	0.597	45.186	2.7
400	92.325	336	6.7	0.638	45.239	2.89

6.4 Summary

The evaluation of ZTC/TCP is one of the key analysis for optimal device operation and reliability. We have systematically analyzed the sensitivity of various device performances towards temperature variation. From the presented outcomes of this work, it is evident that there exist different inflection points for I_D, and g_m, which should be seriously taken into consideration for nanoscale DG-MOSFET or 3-D FinFET based circuit operation.

The following technical topics and contributions are presented in this chapter:

- *Device Description and Simulation Setup for GS-DG MOSFET (Section 6.2)*

  The inflection point due to the temperature of the SG, DG, and GS-DG, UT-SDOI MOSFETs have been investigated using 2-D numerical simulation. The simulation results presented gave a detailed idea about the TCP or ZTC bias point for I_D and g_m. Also, a comparison is made between various parameters like $SS, I_{on}/I_{off}, g_m, g_d, A_V, EDP$, delay, Q-factor, f_T and sweet point among the proposed devices over wide range of temperatures. It can be observed that at a particular temperature ($300K$), the DG device shows nearly 10 times more in I_{on}/I_{off}, 64.49% improvement in EDP, and more than 100% rise of f_T and sweet point as compared to SG device. Furthermore, DG configurations revealed significant improvements in circuit delay and Q-factor over SG device. The outcomes provided in this work can be used as an acceptable design tool for circuits meant for the wide range of temperature variation applications. From the investigations on TCP or ZTC, it is evident that DG configurations lead to a significant improvement in static and dynamic performances as far as nanoscale MOSFET is concerned.

- *Modeling and Simulation Setup for SOI-FinFET (Section 6.3)*

  The present understanding of this work is about to evaluate and resolve the temperature compensation point (TCP) or zero temperature coefficient (ZTC) point for a sub-20 nm FinFET. The sensitivity of geometry parameters on assorted performances of Fin based device and its reliability over ample range of temperatures i.e. 100 K to 400 K is reviewed to extend the benchmark of device scalability. The impact of Fin height (H_{Fin}), Fin width (W_{Fin}), and temperature (T) on immense performance metrics including on-off ratio (I_{on}/I_{off}), transconductance (g_m), gain (A_V), cut-off frequency (f_T), static power dissipation (P_D), energy (E), energy delay product (EDP), and sweet spot ($g_m f_T/I_D$) of the FinFET are studied.

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List of Contribution

1. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Resolving the bias point for wide range of temperature applications in high-k/metal gate nanoscale DG-MOSFET," *Facta Universitatis, Series: Electronics and Energetics*, vol. 27, no. 4, pp. 613-619, Dec. 2014.

2. P. K. Sahu, **S. K. Mohapatra**, and K. P. Pradhan, "Zero temperature coefficient bias point over wide range of temperatures for single-and double-gate UTB-SOI n-MOSFETs with trapped charges," *Materials Science in Semiconductor Processing*, vol. 31, pp. 175-183, 2015.

3. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "Temperature dependence inflection point in Ultra-Thin Si directly on Insulator (SDOI) MOSFETs: An influence to key performance metrics," *Superlattices and Microstructures*, vol. 78, pp. 134-143, 2015.

4. **S. K. Mohapatra**, K. P. Pradhan, and P. K. Sahu, "ZTC bias point of Advanced Fin based Device: The Importance and Exploration," *Facta Universitatis, Series: Electronics and Energetics*, invited paper (Accepted).

Chapter 7

Conclusion and Future Work

In this dissertation, design, modeling and simulation of non-classical MOSFETs are furnished, with a focus on static and analog/RF performance metrics, which is necessary for circuit applications.

TCAD simulation have proven to be an effective tool for Nanoelectronics development, where explorative device studies and with technology fine tuning and optimization techniques are available. It is essential to optimize the device features, make a prediction for complex device structure and quickly get insights for screen technology options with an industrial strategy. The work presented here can be useful to other researchers for developing efficient high-frequency circuit applications and other areas of interest.

Some of the simulated results have been validated with the experimental data in the literature. As the simulation is calibrated with experimental results, an assurance can be accorded for the designed devices as there is no scope for fabrication facilities in the University.

In this thesis, extensive studies has been carried out on a theoretical insight into the issues pertaining to planar MOSFET, the 2-D double gate MOSFET to 3-D FinFET technologies etc.. The 2-D analytical models for single and double gate MOSFET devices have also been explored to validate the dependencies of the characteristics with their geometrical parameters.

In this era of Nanotechnology, the non-classical MOSFETs behavior are investigated on single and double gate devices. Although DG-MOSFET was proposed long back, many a effects have not yet been explored and the author of this thesis has tried to investigate on some characteristics like effect of strain on the channel, +ve and -ve interface trapped charges, high-k gate stack, metal gate work function Engineering, etc. of the device.

The undesirable side effects such as V_{th} roll off due to increase in equivalent Ge content have been analyzed to avoid the possible degradation of device performances.

The DI configuration has demonstrated momentous improvements in terms of I_{off}, surface potential, and the electric field. The UD-DG exhibits highest on current, transconductance, but it experiences subthreshold leakage issue. On the other hand, GC and GS architectures predict reasonable performances in all respects. GS-DG-TM-SH exhibits a higher value of drain current, the peak transconductance and a lower value of $DIBL$. The $DIBL$ and HCE can be controlled effectively by increasing the gate length ratio ($L1/L2$) as per our observation.

An opportunity for realizing high-performance analog and RF circuits with the proposed devices are addressed in the work. The DM-DG configurations are found superior over SM-DG as they show 48.53% improvement in f_T , 25.54% in A_V and more than 90% in V_{EA}.

In case of FinFET, $H_{Fin} = 0.6 \times L_g$ case shows the optimum device performances in terms of gain and maximum frequency of operation. By thinning the W_{Fin}, the FinFET can be free from substrate related effects which further improves the A_V, V_{EA}, and R_0 of the device as shown in our simulated results.

The Trigate ($AR = 1$) shows improvement in delay of the device because of higher I_{eff}. FinFETs ($AR < 1$) and Planar MOSFETs ($AR > 1$) predict desirable improvements in power dissipation and f_T.

The evaluation of ZTC/TCP is one of the fundamental analysis for optimal device operation and reliability. It is evident that there exist different inflection points for I_D, and g_m, which need further investigation for DG-MOSFET and FinFET as far as circuit operations are concerned.

The impact of temperature (T) on immense performance metrics including on-off ratio (I_{on}/I_{off}), transconductance (g_m), gain (A_V), cut-off frequency (f_T), static power dissipation (P_D), energy (E), energy delay product (EDP), and sweet spot ($g_m \times f_T/I_D$) of the FinFET has been analyzed and found the importance of ZTC/TCP of nanoscale MOSFET devices.

7.1 Future Work

The problem of radiation effects on Semiconductor device operations is an important area of study and can be investigated. Both single event effects, which include single event upset (SEU) and single event transient (SET), and total ionization dose (TID) effects can be tested.

Exploration of the effect of thermal noise, random dopant fluctuation (RDF) to different models of multi-gate MOSFETs are very much essential from an application point of view.

New devices with the introduction to organic materials known as an organic device is a novel approach in the field of nanoscale application.

References

[1] L. J. Edgar, "Method and apparatus for controlling electric currents," Jan. 28 1930, US Patent 1,745,175.

[2] W. Shockley, "SHOCKLEY," Sep. 25 1951, US Patent 2,569,347.

[3] R. N. Noyce, "Semiconductor device-and-lead structure," Apr. 25 1961, US Patent 2,981,877.

[4] J. S. Kilby, "Miniaturized electronic circuits," Jun. 23 1964, US Patent 3,138,743.

[5] K. Dawon, "Electric field controlled semiconductor device," Aug. 27 1963, US Patent 3,102,230.

[6] G. E. Moore *et al.*, "Cramming more components onto integrated circuits," 1965.

[7] "The International Technology Roadmap for Semiconductors," Tech. Rep., 2011. [Online]. Available: Http://public.itrs.net

[8] M. Horowitz, T. Indermaur, and R. Gonzalez, "Low-power digital design," in *Low Power Electronics, 1994. Digest of Technical Papers., IEEE Symposium*. IEEE, 1994, pp. 8–11.

[9] W. A. Goddard III, D. Brenner, S. E. Lyshevski, and G. J. Iafrate, *Handbook of nanoscience, engineering, and technology*. CRC press, 2007.

[10] R. P. Feynman, "There's plenty of room at the bottom," *Engineering and science*, vol. 23, no. 5, pp. 22–36, 1960.

[11] C. P. Poole Jr and F. J. Owens, *Introduction to nanotechnology*. John Wiley & Sons, 2003.

[12] B. Vigna, "More than Moore: micro-machined products enable new applications and open new markets," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*. IEEE, 2005, pp. 8–pp.

[13] A. B. Kahng, "Scaling: More than Moore's law," *IEEE Design & Test of Computers*, vol. 27, no. 3, pp. 86–87, 2010.

[14] Y. Taur *et al.*, "CMOS scaling into the nanometer regime," *Proceedings of the IEEE*, vol. 85, no. 4, pp. 486–504, 1997.

[15] H.-S. P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann, and J. J. Welser, "Nanoscale CMOS," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 537–570, 1999.

[16] J. Gautier, X. Jehl, and M. Sanquer, "Single electron devices and applications," *Electronic device architecture for the nano-CMOS era*, pp. 279–297, 2009.

[17] S. Deleonibus, *Electronic Devices Architectures for the NANO-CMOS Era*. Pan Stanford Publishing, 2009.

[18] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design," *IEICE Transactions on Electronics*, vol. 75, no. 4, pp. 371–382, 1992.

[19] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305–327, 2003.

[20] H. Falk, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits," *Proceedings of the IEEE*, vol. 91, no. 2, 2003.

[21] K. Roy and S. C. Prasad, *Low-power CMOS VLSI circuit design*. John Wiley & Sons, 2009.

[22] S. P. Mohanty, N. Ranganathan, E. Kougianos, and P. Patra, *Low-power high-level synthesis for nanoscale CMOS circuits*. Springer Science & Business Media, 2008.

[23] N. Sirisantana and K. Roy, "Low-power design using multiple channel lengths and oxide thicknesses," *IEEE Design & Test of Computers*, vol. 21, no. 1, pp. 56–63, 2004.

[24] C. Wann, F. Assaderaghi, R. Dennard, C. Hu, G. Shahidi, and Y. Taur, "Channel profile optimization and device design for low-power high-performance dynamic-threshold MOSFET," in *Electron Devices Meeting, 1996. IEDM'96., International*. IEEE, 1996, pp. 113–116.

[25] K. Bernstein, D. J. Frank, A. E. Gattiker, W. Haensch, B. L. Ji, S. R. Nassif, E. J. Nowak, D. J. Pearson, and N. J. Rohrer, "High-performance CMOS variability in the 65-nm regime and beyond," *IBM journal of research and development*, vol. 50, no. 4.5, pp. 433–449, 2006.

[26] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi, and M. Bohr, "Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors," in *VLSI Technology, 2000. Digest of Technical Papers. 2000 Symposium on*. IEEE, 2000, pp. 174–175.

[27] V. De and S. Borkar, "Technology and design challenges for low power and high performance," in *Proceedings of the 1999 international symposium on Low power electronics and design*. ACM, 1999, pp. 163–168.

[28] C. Hu, *Modern semiconductor devices for integrated circuits*. Prentice Hall Upper Saddle River, NJ, 2010.

[29] K. Young, "Short-channel effect in fully depleted SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 36, no. 2, pp. 399–402, 1989.

[30] L. Chang, Y. kyu Choi, D. Ha, P. Ranade, S. Xiong, J. Bokor, C. Hu, and T.-J. King, "Extremely scaled silicon nano-CMOS devices," *Proceedings of the IEEE*, vol. 91, no. 11, pp. 1860–1873, Nov 2003.

[31] R. W. Keyes, "High-mobility FET in strained silicon," *IEEE Transactions on Electron Devices*, vol. 33, no. 6, pp. 863–863, 1986.

[32] A. Chaudhry and M. J. Kumar, "Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review," *IEEE Transactions on Device and Materials Reliability*, vol. 4, no. 1, pp. 99–109, 2004.

[33] M. J. Kumar, V. Venkataraman, and S. Nawal, "Impact of strain or Ge content on the threshold voltage of nanoscale strained-Si/SiGe bulk MOSFETs," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 1, pp. 181–187, 2007.

[34] M. V. Dunga, C.-H. Lin, X. Xi, D. D. Lu, A. M. Niknejad, and C. Hu, "Modeling advanced FET technology in a compact model," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 1971–1978, 2006.

[35] L. Jin, L. Hongxia, L. Bin, C. Lei, and Y. Bo, "Two-dimensional threshold voltage analytical model of DMG strained-silicon-on-insulator MOSFETs," *Journal of Semiconductors*, vol. 31, no. 8, p. 084008, 2010.

[36] L. Jin, L. Hongxia, Y. Bo, C. Lei, and L. Bin, "A two-dimensional analytical model of fully depleted asymmetrical dual material gate double-gate strained-Si MOSFETs," *Journal of Semiconductors*, vol. 32, no. 4, p. 044005, 2011.

[37] J. P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electronics*, vol. 48, no. 6, pp. 897–905, 2004.

[38] B. Yu, PhD Thesis, University of California, San Diego, 2009.

[39] G. Celler and S. Cristoloveanu, "Frontiers of silicon-on-insulator," *Journal of Applied Physics*, vol. 93, no. 9, pp. 4955–4978, 2003.

[40] S. Cristoloveanu, "From SOI Basics to Nano-Size," *Nanotechnology for Electronic Materials and Devices*, p. 67, 2010.

[41] C. Hu, "SOI and nanoscale MOSFETs," in *Device Research Conference, 2001*. IEEE, June 2001, pp. 3–4.

[42] T. C. Hsiao and J. C. Woo, "Subthreshold characteristics of fully depleted submicrometer SOI MOSFET's," *IEEE Transactions on Electron Devices*, vol. 42, no. 6, pp. 1120–1125, 1995.

[43] J.-P. Colinge *et al.*, *FinFETs and other multi-gate transistors*. Springer, 2008.

[44] V. Aggarwal, M. K. Khanna, R. Sood, S. Haldar, and R. S. Gupta, "Analytical two-dimensional modeling for potential distribution and threshold voltage of the short-channel fully depleted SOI (silicon-on-insulator) MOSFET," *Solid-State Electronics*, vol. 37, no. 8, pp. 1537–1542, 1994.

[45] V. Aggarwal and R. S. Gupta, “A new two-dimensional short channel model for the drain current-voltage characteristics of a fully depleted SOI (silicon-on-insulator) MOSFET,” *International journal of electronics*, vol. 79, no. 3, pp. 293–301, 1995.

[46] J.-T. Park and J. Colinge, “Multiple-gate SOI MOSFETs: device design guidelines,” *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2222–2229, Dec 2002.

[47] H. H. Hall, J. Bardeen, and G. Pearson, “The Effects of Pressure and Temperature on the Resistance of p-n Junctions in Germanium,” *Physical Review*, vol. 84, no. 1, p. 129, 1951.

[48] C. S. Smith, “Piezoresistance effect in germanium and silicon,” *Physical review*, vol. 94, no. 1, p. 42, 1954.

[49] D. Tweet and S. Hsu, “Enhanced mobility NMOS and PMOS transistors using strained Si/SiGe layers on silicon-on-insulator substrates,” May 14 2001, uS Patent App. 09/855,392.

[50] T. Ghani *et al.*, “A 90nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors,” in *Electron Devices Meeting, 2003. IEDM’03 Technical Digest. IEEE International.* IEEE, 2003, pp. 11–6.

[51] J. Welser, J. Hoyt, and J. Gibbons, “Electron mobility enhancement in strained-Si n-type metal-oxide-semiconductor field-effect transistors,” *IEEE Electron Device Letters*, vol. 15, no. 3, pp. 100–102, 1994.

[52] J. Welser, J. Hoyt, and J. Gibbons, “NMOS and PMOS transistors fabricated in strained silicon/relaxed silicon-germanium structures,” in *Electron Devices Meeting, 1992. IEDM’92. Technical Digest., International.* IEEE, 1992, pp. 1000–1002.

[53] A. Khakifirooz *et al.*, “Strain engineered extremely thin SOI (ETSOI) for high-performance CMOS,” in *VLSI Technology (VLSIT), 2012 Symposium on.* IEEE, 2012, pp. 117–118.

[54] K. Cheng *et al.*, “High performance extremely thin SOI (ETSOI) hybrid CMOS with Si channel NFET and strained SiGe channel PFET,” in *Electron Devices Meeting (IEDM), 2012 IEEE International.* IEEE, 2012, pp. 18–1.

[55] D. M. Paskiewicz, B. Tanto, D. E. Savage, and M. G. Lagally, “Defect-free single-crystal SiGe: a new material from nanomembrane strain engineering,” *ACS nano*, vol. 5, no. 7, pp. 5814–5822, 2011.

[56] D. Hisamoto, T. Kaga, and E. Takeda, “Impact of the vertical SOI DELTA structure on planar device technology,” *IEEE Transactions on Electron Devices*, vol. 38, no. 6, pp. 1419–1424, 1991.

[57] J. P. Denton and G. W. Neudeck, “Fully depleted dual-gated thin-film SOI P-MOSFETs fabricated in SOI islands with an isolated buried polysilicon backgate,” *IEEE Electron Device Letters*, vol. 17, no. 11, pp. 509–511, 1996.

[58] K. Suzuki and T. Sugii, “Analytical models for n+-p+ double-gate SOI MOSFET’s,” *IEEE Transactions on Electron Devices*, vol. 42, no. 11, pp. 1940–1948, 1995.

[59] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and T. Sugii, “High-Speed and Low-Power n+-p+ Double-Gate SOI CMOS,” *IEICE transactions on electronics*, vol. 78, no. 4, pp. 360–367, 1995.

[60] D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu, “A folded-channel MOSFET for deep-sub-tenth micron era,” in *Electron Devices Meeting, 1998. IEDM ’98. Technical Digest., International*, Dec 1998, pp. 1032–1034.

[61] H.-S. Wong, D. Frank, and P. Solomon, “Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET’s at the 25 nm channel length generation,” in *Electron Devices Meeting, 1998. IEDM ’98. Technical Digest., International*, Dec 1998, pp. 407–410.

[62] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, “Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance,” *IEEE Electron Device Letters*, vol. 8, no. 9, pp. 410–412, 1987.

[63] D. Frank, S. Laux, and M. Fischetti, “Monte Carlo simulation of a 30 nm dual-gate MOSFET: how short can Si go?” in *Electron Devices Meeting, 1992. IEDM ’92. Technical Digest., International*, Dec 1992, pp. 553–556.

[64] S. Cristoloveanu and S. Li, *Electrical characterization of silicon-on-insulator materials and devices.* Springer Science & Business Media, 1995, vol. 305.

[65] D. D. Lu, M. V. Dunga, C.-H. Lin, A. M. Niknejad, and C. Hu, "A computationally efficient compact model for fully-depleted SOI MOSFETs with independently-controlled front-and back-gates," *Solid-State Electronics*, vol. 62, no. 1, pp. 31–39, 2011.

[66] S. Khandelwal *et al.*, "BSIM-IMG: A compact model for ultrathin-body SOI MOSFETs with back-gate control," *IEEE Transactions on Electron Devices*, vol. 59, no. 8, pp. 2019–2026, 2012.

[67] S. Wind, D. Frank, and H.-S. Wong, "Scaling silicon MOS devices to their limits," *Microelectronic Engineering*, vol. 32, no. 1, pp. 271–282, 1996.

[68] P. Razavi and A. A. Orouji, "Nanoscale triple material double gate (TM-DG) MOSFET for improving short channel effects," in *Advances in Electronics and Micro-electronics, 2008. ENICS'08. International Conference on.* IEEE, 2008, pp. 11–14.

[69] P. K. Tiwari, S. Dubey, M. Singh, and S. Jit, "A two-dimensional analytical model for threshold voltage of short-channel triple-material double-gate metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. 108, no. 7, p. 074508, 2010.

[70] K. Goel, M. Saxena, M. Gupta, and R. Gupta, "Modeling and simulation of a nanoscale three-region tri-material gate stack (TRIMGAS) MOSFET for improved carrier transport efficiency and reduced hot-electron effects," *IEEE Transactions on Electron Devices*, vol. 53, no. 7, pp. 1623–1633, 2006.

[71] M.-L. Chen, W.-K. Lin, and S.-F. Chen, "A new two-dimensional analytical model for nanoscale symmetrical tri-material gate stack double gate metal–oxide–semiconductor field effect transistors," *Japanese Journal of Applied Physics*, vol. 48, no. 10R, p. 104503, 2009.

[72] R. K. Sharma, M. Gupta, and R. Gupta, "TCAD assessment of device design technologies for enhanced performance of nanoscale DG MOSFET," *IEEE Transactions on Electron Devices*, vol. 58, no. 9, pp. 2936–2943, 2011.

[73] B. H. Lee, S. C. Song, R. Choi, and P. Kirsch, "Metal electrode/high-k dielectric gate-stack technology for power management," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 8–20, 2008.

[74] D. Nirmal, P. Vijayakumar, P. P. C. Samuel, B. K. Jebalin, and N. Mohankumar, "Subthreshold analysis of nanoscale FinFETs for ultra low power application using high-k materials," *International Journal of Electronics*, vol. 100, no. 6, pp. 803–817, 2013.

[75] J. Colinge, "Fully-depleted SOI CMOS for analog applications," *IEEE Transactions on Electron Devices*, vol. 45, no. 5, pp. 1010–1016, 1998.

[76] B. Razavi, "CMOS technology characterization for analog and RF design," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 3, pp. 268–276, 1999.

[77] V. Kilchytska *et al.*, "Influence of device engineering on the analog and RF performances of SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 577–588, 2003.

[78] N. Mohankumar, B. Syamal, and C. Sarkar, "Influence of Channel and Gate Engineering on the Analog and RF Performance of DG MOSFETs," *IEEE Transactions on Electron Devices*, vol. 57, no. 4, pp. 820–826, April 2010.

[79] A. Sarkar, A. K. Das, S. De, and C. K. Sarkar, "Effect of gate engineering in double-gate MOSFETs for analog/RF applications," *Microelectronics Journal*, vol. 43, no. 11, pp. 873–882, 2012.

[80] R. K. Sharma and M. Bucher, "Device design engineering for optimum analog/RF performance of nanoscale DG MOSFETs," *IEEE Transactions on Nanotechnology*, vol. 11, no. 5, pp. 992–998, 2012.

[81] B. Yu, C. H. Wann, E. D. Nowak, K. Noda, and C. Hu, "Short-channel effect improved by lateral channel-engineering in deep-submicronmeter MOSFET's," *IEEE Transactions on Electron Devices*, vol. 44, no. 4, pp. 627–634, 1997.

[82] A. Kranti, T. M. Chung, D. Flandre, and J.-P. Raskin, "Laterally asymmetric channel engineering in fully depleted double gate SOI MOSFETs for high performance analog applications," *Solid-State Electronics*, vol. 48, no. 6, pp. 947–959, 2004.

[83] G. V. Reddy and M. J. Kumar, "Investigation of the novel attributes of a single-halo double gate SOI MOSFET: 2D simulation study," *Microelectronics journal*, vol. 35, no. 9, pp. 761–765, 2004.

[84] Z. Li, Y. Jiang, and L. Zhang, "A single-halo dual-material gate SOI MOSFET," in *Electron Devices and Semiconductor Technology, 2007. EDST 2007. Proceeding of 2007 International Workshop on.* IEEE, 2007, pp. 66–69.

[85] S. Chakraborty, A. Mallik, C. K. Sarkar, and V. R. Rao, “Impact of halo doping on the subthreshold performance of deep-submicrometer CMOS devices and circuits for ultralow power analog/mixed-signal applications,” *IEEE Transactions on Electron Devices*, vol. 54, no. 2, pp. 241–248, 2007.

[86] J. Colinge, “Multi-gate SOI MOSFETs,” *Microelectronic Engineering*, vol. 84, no. 9, pp. 2071–2076, 2007.

[87] S. M. Sze, *Physics of Semiconductor Devices*, third edit ed. John Wiley and Sons Inc., 2009.

[88] D. Flandre, L. Ferreira, P. Jespers, and J.-P. Colinge, “Modelling and application of fully depleted SOI MOSFETs for low voltage, low power analogue CMOS circuits,” *Solid-State Electronics*, vol. 39, no. 4, pp. 455–460, 1996.

[89] A. Lazaro and B. Iniguez, “RF and noise performance of double gate and single gate SOI,” *Solid-State Electronics*, vol. 50, no. 5, pp. 826–842, 2006.

[90] J.-P. Raskin, T. M. Chung, V. Kilchytska, D. Lederer, and D. Flandre, “Analog/RF performance of multiple gate SOI devices: wideband simulations and characterization,” *IEEE Transactions on Electron Devices*, vol. 53, no. 5, pp. 1088–1095, 2006.

[91] A. Matsuzawa, “High quality analog CMOS and mixed signal LSI design,” in *Quality Electronic Design, 2001 International Symposium on.* IEEE, 2001, pp. 97–104.

[92] F. Silveira, D. Flandre, and P. Jespers, “A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA,” *Solid-State Circuits, IEEE Journal of*, vol. 31, no. 9, pp. 1314–1319, 1996.

[93] J. Colinge, M. Cao, and W. Greene, “Analog parameters of short-channel SOI MOSFETs,” in *SOI Conference, 1997. Proceedings., 1997 IEEE International.* IEEE, 1997, pp. 88–89.

[94] H. Fukui, “Optimal noise figure of microwave GaAs MESFET’s,” *IEEE Transactions on Electron Devices*, vol. 26, no. 7, pp. 1032–1037, 1979.

[95] C. Chen *et al.*, “High-performance fully-depleted SOI RF CMOS,” *IEEE Electron Device Letters*, vol. 23, no. 1, pp. 52–54, 2002.

[96] H. M. Boots, G. Doornbos, and A. Heringa, “Scaling of characteristic frequencies in RF CMOS,” *IEEE Transactions on Electron Devices*, vol. 51, no. 12, pp. 2102–2108, 2004.

[97] G. Dambrine, C. Raynaud, D. Lederer, M. Dehan, O. Rozeaux, M. Vanmackelberg, F. Danneville, S. Lepilliet, and J.-P. Raskin, “What are the limiting parameters of deep-submicron MOSFETs for high frequency applications?” *IEEE Electron Device Letters*, vol. 24, no. 3, pp. 189–191, 2003.

[98] Y. Pratap, S. Haldar, R. Gupta, and M. Gupta, “Performance Evaluation and Reliability Issues of Junctionless CSG MOSFET for RFIC Design,” *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 1, pp. 418–425, 2014.

[99] S. Kang, B. Choi, and B. Kim, “Linearity analysis of CMOS for RF application,” *IEEE Transaction on Microwave Theory and Techniques*, vol. 51, pp. 972–977, 2003.

[100] R. Gautam, M. Saxena, R. Gupta, and M. Gupta, “Effect of localised charges on nanoscale cylindrical surrounding gate MOSFET: Analog performance and linearity analysis,” *Microelectronics Reliability*, vol. 52, no. 1, pp. 989–994, 2012.

[101] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, “Device scaling limits of Si MOSFETs and their application dependencies,” *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259–288, 2001.

[102] T. Skotnicki, J. A. Hutchby, T.-J. King, H.-S. Wong, and F. Boeuf, “The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance,” *IEEE Circuits and Devices Magazine*, vol. 21, no. 1, pp. 16–26, 2005.

[103] I. Ferain, C. A. Colinge, and J.-P. Colinge, “Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors,” *Nature*, vol. 479, no. 7373, pp. 310–316, 2011.

[104] Suzuki, K. and Tanaka, T. and Tosaka, Y. and Horie, H. and Arimoto, Y., “Scaling theory for double-gate SOI MOSFET’s,” *IEEE Transactions on Electron Devices*, vol. 40, no. 12, pp. 2326–2329, 1993.

[105] C. H. Wann, K. Noda, T. Tanaka, M. Yoshida, and C. Hu, “A comparative study of advanced MOSFET concepts,” *IEEE Transactions on Electron Devices*, vol. 43, no. 10, pp. 1742–1753, 1996.

[106] H.-S. Wong, "Beyond the conventional transistor," *IBM Journal of Research and Development*, vol. 46, no. 2.3, pp. 133–168, 2002.

[107] B. Cheng, M. Cao, R. Rao, A. Inani, P. Vande Voorde, W. M. Greene, J. M. Stork, Z. Yu, P. M. Zeitzoff, and J. C. Woo, "The impact of high-κ gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs," *IEEE Transactions on Electron Devices*, vol. 46, no. 7, pp. 1537–1544, 1999.

[108] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, "Review on high-k dielectrics reliability issues," *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 1, pp. 5–19, March 2005.

[109] B. H. Lee, J. Oh, H. H. Tseng, R. Jammy, and H. Huff, "Gate stack technology for nanoscale devices," *Materials Today*, vol. 9, no. 6, pp. 32–40, 2006.

[110] V. Misra, G. Lucovsky, and G. Parsons, "Issues in High-κ Gate Stack Interfaces," *MRS bulletin*, vol. 27, no. 03, pp. 212–216, 2002.

[111] J.-P. Locquet, C. Marchiori, M. Sousa, J. Fompeyrine, and J. W. Seo, "High-K dielectrics for the gate stack," *Journal of Applied Physics*, vol. 100, no. 5, p. 051610, 2006.

[112] D. Lin *et al.*, "Enabling the high-performance InGaAs/Ge CMOS: A common gate stack solution," in *Electron Devices Meeting (IEDM), 2009 IEEE International*. IEEE, 2009, pp. 1–4.

[113] Y. C. Yeo, P. Ranade, T. J. King, and C. Hu, "Effects of high-k gate dielectric materials on metal and silicon gate workfunctions," *IEEE Electron Device Letters*, vol. 23, no. 6, pp. 342–344, 2002.

[114] C. Hu, "Gate oxide scaling limits and projection," in *Electron Devices Meeting, 1996. IEDM '96., International*, Dec 1996, pp. 319–322.

[115] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-κ/metal-gate stack and its MOSFET characteristics," *IEEE Electron Device Letters*, vol. 25, no. 6, pp. 408–410, 2004.

[116] A. Inani, R. V. Rao, B. Cheng, and J. Woo, "Gate stack architecture analysis and channel engineering in deep sub-micron MOSFETs," *Japanese journal of applied physics*, vol. 38, no. 4S, p. 2266, 1999.

[117] E. D. LITTA, "Integration of thulium silicate for enhanced scalability of high-k/metal gate CMOS technology," Ph.D. dissertation, PhD Thesis, KTH Royal Institute of Technology, 2014.

[118] B. Greene *et al.*, "High performance 32nm SOI CMOS with high-k/metal gate and 0.149μm 2 SRAM and ultra low-k back end with eleven levels of copper," in *VLSI Technology, 2009 Symposium on*, 6 2009, pp. 140–141.

[119] P. Packan *et al.*, "High performance 32nm logic technology featuring 2nd generation high-k + metal gate transistors," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 12 2009, pp. 1–4.

[120] T. George James, S. Joseph, and V. Mathew, "The Influence of Metal Gate Work Function on Short Channel Effects in Atomic-layer Doped DG MOSFETs," *Journal of Electron Devices*, vol. 8, pp. 310–319, 2010.

[121] "The Spice Page. UC Berkeley," Tech. Rep. [Online]. Available: http://bwrc.eecs.berkeley.edu/classes/icbook/spice/

[122] "Stanford TCAD. Stanford University." Tech. Rep. [Online]. Available: http://www-tcad.stanford.edu/

[123] "Device, TCAD Sentaurus. "version 2012.06.G" Synopsis, Mountain View, CA." Tech. Rep. [Online]. Available: http://www.synopsys.com/Tools/

[124] L. Behlau and H.-J. Bullinger, *Technology guide: Principles-applications-trends*. Springer Science & Business Media, 2009.

[125] E. G. Ioannidis, A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, and J. Jomaah, "Effect of localized interface charge on the threshold voltage of short-channel undoped symmetrical double-gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 58, no. 2, pp. 433–440, 2011.

[126] A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, G. Pananakakis, and G. Ghibaudo, "Threshold voltage model for short-channel undoped symmetrical double-gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 55, no. 9, pp. 2512–2516, 2008.

[127] H. M. Nayfeh, J. L. Hoyt, and D. A. Antoniadis, "A physically based analytical model for the threshold voltage of strained-Si n-MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 51, no. 12, pp. 2069–2072, 2004.

[128] F. Djeffal, Z. Ghoggali, Z. Dibi, and N. Lakhdar, "Analytical analysis of nanoscale multiple gate MOSFETs including effects of hot-carrier induced interface charges," *Microelectronics Reliability*, vol. 49, no. 4, pp. 377–381, 2009.

[129] S. Chakraborty, A. Mallik, and C. K. Sarkar, "Subthreshold Performance of Dual-Material Gate CMOS Devices and Circuits for Ultralow Power Analog/Mixed-Signal Applications," *IEEE Transactions on Electron Devices*, vol. 55, no. 3, pp. 827–832, 2008.

[130] R.-H. Yan, A. Ourmazd, and K. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *IEEE Transactions on Electron Devices*, vol. 39, no. 7, pp. 1704–1710, Jul 1992.

[131] J. Widiez, J. Lolivier, M. Vinet, T. Poiroux, B. Previtali, F. Daugé, M. Mouis, and S. Deleonibus, "Experimental evaluation of gate architecture influence on DG SOI MOSFETs performance," *IEEE Transactions on Electron Devices*, vol. 52, no. 8, pp. 1772–1779, 2005.

[132] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Transactions on Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec 2000.

[133] S. Cristoloveanu, "How Many Gates do we Need in a Transistor?" in *Semiconductor Conference, 2007. CAS 2007. International*, vol. 1. IEEE, 2007, pp. 3–10.

[134] M. G. C. de Andrade, J. A. Martino, M. Aoulaiche, N. Collaert, E. Simoen, and C. Claeys, "Behavior of triple-gate Bulk FinFETs with and without {DTMOS} operation ," *Solid-State Electronics*, vol. 71, no. 0, pp. 63 – 68, 2012.

[135] B. Ho, X. Sun, C. Shin, and T.-J. K. Liu, "Design Optimization of Multigate Bulk MOSFETs," *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 28–33, January 2013.

[136] V. A. Sverdlov, T. J. Walls, and K. K. Likharev, "Nanoscale silicon MOSFETs: A theoretical study," *IEEE Transactions on Electron Devices*, vol. 50, no. 9, pp. 1926–1933, 2003.

[137] X. Sun, V. Moroz, N. Damrongplasit, C. Shin, and T.-J. K. Liu, "Variation Study of the Planar Ground-Plane Bulk MOSFET, SOI FinFET, and Trigate Bulk MOSFET Designs," *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3294–3299, Oct 2011.

[138] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*, 1984.

[139] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *IEEE Transactions on Electron Devices*, vol. 22, no. 11, pp. 1045–1047, 1975.

[140] W. Shockley and W. Read Jr, "Statistics of the recombinations of holes and electrons," *Physical review*, vol. 87, no. 5, p. 835, 1952.

[141] R. N. Hall, "Electron-hole recombination in germanium," *Physical Review*, vol. 87, no. 2, p. 387, 1952.

[142] S. Saha, "MOSFET test structures for two-dimensional device simulation," *Solid-State Electronics*, vol. 38, no. 1, pp. 69–73, 1995.

[143] A. Kranti and G. A. Armstrong, "Device design considerations for nanoscale double and triple gate FinFETs," in *SOI Conference, 2005. Proceedings. 2005 IEEE International*. IEEE, 2005, pp. 96–98.

[144] C. Manoj, M. Nagpal, D. Varghese, and V. Ramgopal Rao, "Device design and optimization considerations for bulk FinFETs," *IEEE Transactions on Electron Devices*, vol. 55, no. 2, pp. 609–615, 2008.

[145] R. Coquand *et al.*, "Comparative simulation of TriGate and FinFET on SOI: Evaluating a multiple threshold voltage strategy on triple gate devices," in *SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2013 IEEE*, Oct 2013, pp. 1–2.

[146] A. Kranti and G. A. Armstrong, "Design and optimization of FinFETs for ultra-low-voltage analog applications," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3308–3316, 2007.

[147] A. Nandi, A. K. Saxena, and S. Dasgupta, "Design and analysis of analog performance of Dual-k spacer underlap N/P-FinFET at 12 nm gate length," *IEEE Transactions on Electron Devices*, vol. 60, no. 5, pp. 1529–1535, 2013.

[148] V. Kilchytska, G. Paillonçy, D. Lederer, J.-P. Raskin, N. Collaert, M. Jurczak, and D. Flandre, "Frequency variation of the small-signal output conductance of decananometer MOSFETs due to substrate crosstalk," *IEEE Electron Device Letters*, vol. 28, no. 5, pp. 419–421, 2007.

[149] V. Subramanian *et al.*, "Impact of fin width on digital and analog performances of n-FinFETs," *Solid-State Electronics*, vol. 51, no. 4, pp. 551–559, 2007.

[150] M.-H. Na, E. Nowak, W. Haensch, and J. Cai, "The effective drive current in CMOS inverters," in *Electron Devices Meeting, 2002. IEDM'02. International.* IEEE, 2002, pp. 121–124.

[151] R. L. Patterson, J. E. Dickman, A. Hammoud, and S. Gerber, "Electronic components and circuits for extreme temperature environments," in *IEEE Aerospace Conference Proceedings*, vol. 6, 2003, pp. 2543–2548.

[152] B. Yu, H. Wang, H.-S. Kim, Q. Xiang, M.-R. Lin, L. Chang, and C. Hu, "Nanoscale CMOS at low temperature: design, reliability, and scaling trend," in *International Symposium on VLSI Technology, Systems, and Applications*, 2001, pp. 23–25.

[153] D.-S. Jeon and D. Burk, "A temperature-dependent SOI MOSFET model for high-temperature application (27 ÂřC-300 ÂřC)," *IEEE Transactions on Electron Devices*, vol. 38, no. 9, pp. 2101 – 2111, 1991.

[154] M. Bruel, "Silicon on insulator material technology," *Electronics Letters*, vol. 31, no. 14, pp. 1201–1202, 1995.

[155] J. P. Colinge, "The SOI MOSFET: From single gate to multigate," in *FinFETs and Other Multi-Gate Transistors.* Springer US, 2008, pp. 1–48.

[156] G. Reichert, C. Raynaud, O. Faynot, F. Balestra, and S. Cristoloveanu, "Submicron SOI-MOSFETs for high temperature operation (300-600K)," *Microelectronic Engineering*, vol. 36, no. 1-4, pp. 359–362, Jun. 1997.

[157] Z. D. Prijić, S. S. Dimitrijev, and N. D. Stojadinović, "Analysis of temperature dependence of CMOS transistors' threshold voltage," *Microelectronics Reliability*, vol. 31, no. 1, pp. 33–37, 1991.

[158] Z. Prijić, S. Dimitrijev, and N. Stojadinović, "The determination of zero temperature coefficient point in CMOS transistors," *Microelectronics Reliability*, vol. 32, no. 6, pp. 769–773, Jun. 1992.

[159] Z. Prijić, Z. Pavlović, S. Ristić, and N. Stojadinović, "Zero-temperature-coefficient (ZTC) biasing of power VDMOS transistors," *Electronics Letters*, vol. 29, no. 5, pp. 435–437, 1993.

[160] G. Groeseneken, J.-P. Colinge, H. Maes, J. Alderman, and S. Holt, "Temperature dependence of threshold voltage in thin-film SOI MOSFETs," *IEEE Electron Device Letters*, vol. 11, no. 8, pp. 329–331, 1990.

[161] A. Osman, M. Osman, N. Dogan, and M. Imam, "Zero-temperature-coefficient biasing point of partially depleted SOI MOSFET's," *IEEE Transactions on Electron Devices*, vol. 42, no. 9, pp. 1709–1711, 1995.

[162] F. Shoucair, "Analytical and experimental methods for zero-temperature-coefficient biasing of MOS transistors," *Electronics Letters*, vol. 25, no. 17, pp. 1196 – 1198, 1989.

[163] T. H. Tan and A. K. Goel, "Zero-Temperature-Coefficient Biasing Point of a Fully depleted SOI MOSFET," *Microwave and Optical Technology Letters*, vol. 37, no. 5, pp. 366–370, 2003.

[164] D. Flandre, L. Demeûs, V. Dessard, A. Viviani, B. Gentinne, J.-P. Eggermont *et al.*, "Design and application of SOI CMOS OTAs for high-temperature applications," in *24th European Solid-State Circuits Conference 1998 (ESSCIRC 1998)*, 1998.

[165] F. Gámiz, "Temperature behaviour of electron mobility in double-gate silicon on insulator transistors," *Semiconductor Science and Technology*, vol. 19, no. 1, pp. 113–119, 2004.

[166] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics*, vol. 89, no. 10, pp. 5243–5275, 2001.

[167] R. Chau *et al.*, "Application of high-k gate dielectrics and metal gate electrodes to enable silicon and non-silicon logic nanotechnology," *Microelectronic Engineering*, vol. 80, pp. 1–6, 2005.

[168] D. Ha, H. Takeuchi, Y.-K. Choi, T. J. King, W. P. Bai, D. L. Kwong, A. Agarwal, and M. Ameen, "Molybdenum gate HfO 2 CMOS FinFET technology," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International.* IEEE, 2004, pp. 643–646.

[169] H. A. El Hamid, J. Roig Guitart, and B. Iñíguez, "Two-dimensional analytical threshold voltage and subthreshold swing models of undoped symmetric double-gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1402–1408, 2007.

[170] H. Castán, S. Dueñas, H. García, A. Gómez, L. Bailón, M. Toledano-Luque, A. Del Prado, I. Mártil, and G. González-Díaz, "Effect of interlayer trapping and detrapping on the determination of interface state densities on high-k dielectric stacks," *Journal of Applied Physics*, vol. 107, pp. 1–5, 2010.

[171] A. Kranti, R. Rashmi, S. Burignat, J. P. Raskin, and G. A. Armstrong, "Analog/RF performance of sub-100 nm SOI MOSFETs with non-classical gate-source/drain underlap channel design," in *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), Topical Meeting on*, 2010.

[172] H. Shang *et al.*, "Investigation of FinFET devices for 32nm technologies and beyond," in *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on.* IEEE, 2006, pp. 54–55.

[173] V. Venkataraman, S. Nawal, and M. Kumar, "Compact Analytical Threshold-Voltage Model of Nanoscale Fully Depleted Strained-Si on Silicon Germanium-on-Insulator (SGOI) MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 3, pp. 554–562, March 2007.

[174] M. J. Kumar, V. Venkataraman, and S. Nawal, "A simple analytical threshold voltage model of nanoscale single-layer fully depleted strained-silicon-on-insulator MOSFETs," *IEEE Transactions on Electron Devices*, vol. 53, no. 10, pp. 2500–2506, 2006.

[175] H. Yin, K. Hobart, R. L. Peterson, F. Kub, S. Shieh, T. Duffy, and J. Sturm, "Fully-depleted strained-Si on insulator NMOSFETs without relaxed SiGe buffers," in *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International.* IEEE, 2003, pp. 3–2.

[176] M. J. Kumar and A. A. Orouji, "Two-dimensional analytical threshold voltage model of nanoscale fully depleted SOI MOSFET with electrically induced S/D extensions," *IEEE Transactions on Electron Devices*, vol. 52, no. 7, pp. 1568–1575, 2005.

[177] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 7, no. 11, pp. 1164–1171, 1988.

Curriculum Vitae

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CAREER OBJECTIVE

I aim to find interesting research opportunities on Nano-electronics devices with application towards IoT in which my contributions will make a difference to the quality of life of real people.

EDUCATION

Degree	Percentage(%)	Year	Subject Taken	University/Board
Ph.D.	Continuing.	2011-Till	Nanoelectronics Device	N.I.T. Rourkela.
M.E.	69.68	1999-2001	Communication Control & Networking	R. G. P. V., Bhopal, M.P.
B.E.	69.5	1990-1994	Electronics & Telecommunication	Utkal University, Bhubaneswar.
+2Sc.	60	1988-1990	Phy, Chem., Math., Bio.	C.H.S.E., Odisha.
10th	68.2	1988	Maths,Sciences, etc.	B.S.E., Odisha

WORK EXPERIENCE

Institution	Designation	Duration	Nature of Job
INTECH Systems, Bhubaneswar	Customer Support Engineer	Feb 1995 to Feb 1996	Field
MODI XEROX, Bhubaneswar	Trainee Engineer	Apr 1996 to Apr 1997	Field
ET&T LTD, Bhubaneswar	System Engineer	Aug 1997 to Aug 1999	Field
A.B.I.T., Cuttack.	Lecturer	Mar 2001 to June 2006	Teaching
A.B.I.T., Cuttack.	Sr. Lecturer	July 2006 to June 2007	Teaching
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PERSONAL DETAILS

- *Date of Birth* – - 25/07/1974
- *Father's Name* – Dr. Saroj Kumar Mohapatra
- *Nationality* – Indian
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- *Languages Known* – English, Hindi, Odia

MEMBERSHIP OF PROFESSIONAL BODIES

- ♢ *Life Member* – - ISTE (Indian Society of Technical Education), LM-52026
- ♢ *Life Member* – IETE (Indian Institute of Electronics & Telecom. Engineers), M-192348
- ♢ *Life Member* – OITS (Orissa Information Technology Society)
- ♢ *Student Member* – IEEE Electron Devices Society, 92400894.

DETAILS OF RESEARCH PUBLICATIONS

- ♢ International Journals : 13
- ♢ National Journals : 2
- ♢ International Conferences: 10
- ♢ National Conferences : 3

REVIEWER OF JOURNALS

- ♢ Transactions on Electron Devices, IEEE.
- ♢ Material Science in Semiconductor Processing, Elsevier.
- ♢ Transaction on Nanotechnology, IEEE.
- ♢ British Journal of Applied Science & Technology, SCIENCE DOMAIN International.
- ♢ Journal of Electrical & Electronics Engineering Research, Academic Journals.
- ♢ International Journal of Electronics, Taylor & Francis.

PARTICIPATION IN CONFERENCES AND WORKSHOPS

- ♢ Best presentation of RSW-2015 among all 20 departments of the institute on occasion of *Research Scholar Week-2015*, NIT, Rourkela, $11^{th} - 13^{th}$ May 2015.
- ♢ 11th IEEE India Conference, INDICON, Pune, $11^{th} - 13^{th}$ December 2014.
- ♢ *IEEE EDS Kolkata Chapter Mini-Colloquium, Bhubaneswar*, $3^{th} - 4^{th}$ December 2014.
- ♢ *INUP Familiarization Workshop on Nanofabrication Technologies, IIT Mumbai*, $28^{th} - 30^{th}$ November 2014.
- ♢ *TEQIP sponsored Training Programme on Aesthetics of Scientific Documentation, NIT, Rourkela*, $16^{th} - 17^{th}$ July 2014.
- ♢ *First National Conference on Recent Developments in Electronics, New Delhi*, $18^{th} - 20^{th}$ January 2013.
- ♢ *International Conference on Emerging Electronics, IIT, Bombay*, $15^{th} - 17^{th}$ December 2012.
- ♢ *IEEE EDS Mini-Colloquium on CMOS Technology, Bhubaneswar*, 7*th* April 2012.
- ♢ 6*th National Seminar on Recent Advances in Science & Technology, Cuttack*, $12^{th} - 13^{th}$ February, 2010.
- ♢ *QIP Short Term Course on RF and Microwave Measurement Fundamentals for Morden Electronic Systems* , $9^{th} - 22^{nd}$ June 2008.
- ♢ *QIP Short Term Course on RF and Microwave Measurement Fundamentals for Morden Electronic Systems* , $9^{th} - 22^{nd}$ June 2008.
- ♢ *AICTE Sponsored ISTE Short Term Training Programme on Morden Trends in Communication Techniques, New Delhi*, $26^{th} - 30^{th}$ March 2008.
- ♢ *Workshop on Soft Computing and Machine Learning for Signal Processing, control, Power and Telecommunications, Bhubaneswar*, $8^{th} - 11^{th}$ April 2005.
- ♢ *National Institute of Technical Teacher's Training and Research Programme on Induction Training, Cuttack*, 29th November - 3rd December 2004.
- ♢ *Technical Teacher's Training on Multimedia Development, Kolkota*, 31st May - 4th June 2004.

Dissemination of Work

Journal

[1] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Improved Performance in GS-DG-MOSFET with Dual Material Gate and Lateral Asymmetric Channel ," *Int. J. of Nano and Biomaterials*, p. Accepted.

[2] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "ZTC bias point of Advanced Fin based Device: The Importance and Exploration," *Facta Universitatis, Series: Electronics and Energetics*,p. Accepted.

[3] S. K. Mohapatra, K. P. Pradhan, D. Singh, and P. K. Sahu, "The Role of Geometry Parameters and Fin Aspect Ratio of sub-20nm SOI-FinFET: An Analysis towards Analog and RF Circuit Design," *Nanotechnology, IEEE Transactions on*, vol. 14, no. 03, pp. 1–9, May 2015.

[4] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Temperature dependence inflection point in Ultra-Thin Si directly on Insulator (SDOI) MOSFETs: An influence to key performance metrics," *Superlattices and Microstructures*, vol. 78, pp. 134–143, 2015.

[5] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Estimation of Analog/RF FOMs using Device Design Engineering in GS-DG-MOSFET," *Materials Science in Semiconductor Processing*, vol. 31, pp. 455–462, 2015.

[6] P. K. Sahu, S. K. Mohapatra, and K. P. Pradhan, "Zero temperature-coefficient bias point over wide range of temperatures for single-and double-gate UTB-SOI n-MOSFETs with trapped charges," *Materials Science in Semiconductor Processing*, vol. 31, pp. 175–183, 2015.

[7] S. K. Mohapatra, K. P. Pradhan, P. K. Sahu, G. S. Pati, and M. R. Kumar, "The effect of interface trapped charges in DMG-S-SOI MOSFET: a perspective study," *Advances in Natural Sciences: Nanoscience and Nanotechnology*, vol. 5, no. 4, pp. 1–7, Nov. 2014.

[8] K. P. Pradhan, S. K. Mohapatra, P. K. Sahu, and D. K. Behera, "Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET," *Microelectronics Journal*, vol. 45, no. 2, pp. 144–151, 2014.

[9] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Resolving the bias point for wide range of temperature applications in high-k/metal gate nanoscale DG-MOSFET," *Facta Universitatis, Series: Electronics and Energetics*, vol. 27, no. 4, pp. 613–619, Dec. 2014.

[10] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Influence of High-k Gate Dielectric on Nanoscale DG-MOSFET." *International Journal of Advanced Science & Technology*, vol. 65, 2014.

[11] M. R. Kumar, P. K. Agarwal, G. S. Pati, K. P. Pradhan, S. K. Mohapatra, and P. K. Sahu, "Modeling of Nanoscale Double-Gate MOSFET and Its Physical Analysis," *International Journal of Scientific & Engineering Research*, vol. 5, no. 5, pp. 11–16, May. 2014.

[12] S. K. Mohapatra, K. P. Pradhan, P. K. Sahu, and M. R. Kumar, "The performance measure of GS-DG MOSFET: an impact of metal gate work function," *Advances in Natural Sciences: Nanoscience and Nanotechnology*, vol. 5, no. 2, pp. 1–6, Mar. 2014.

[13] M. R. Kumar, S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "A Simple Analytical Center Potential Model for Cylindrical Gate All Around (CGAA) MOSFET," *Journal of Electron Devices*, vol. 19, pp. 1648–1653, Mar. 2014.

[14] P. K. Sahu, S. K. Mohapatra, and K. P. Pradhan, "Impact of Downscaling on Analog/RF Performance of sub-100nm GS-DG MOSFET," *Informacije Midem-Journal of Microelectronics Electronic Components and Materials*, vol. 44, no. 2, pp. 119–125, Mar. 2014.

[15] P. K. Sahu, K. P. Pradhan, and S. K. Mohapatra, "A Study on SCEs of FD-S-SOI MOSFET in Nanoscale," *Universal Journal of Electrical and Electronic Engineering*, vol. 2, no. 1, pp. 37–43, 2014.

[16] P. K. Sahu, S. K. Mohapatra, and K. P. Pradhan, "A Study of SCEs and Analog FOMs in GS-DG-MOSFET with Lateral Asymmetric Channel Doping," *Journal of Semiconductor Technology and Science*, vol. 13, no. 6, pp. 647–654, Dec. 2013.

[17] K. P. Pradhan, P. K. Agarwal, P. K. Sahu, and S. K. Mohapatra, "Role of High-k Materials in Nanoscale TM-DG MOSFET: A Simulation Study," *Invertis Journal of Science and Technology*, vol. 6, no. 4, pp. 1–5, 2013.

[18] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Some Device Design Considerations to Enhance the Performance of DG-MOSFETs," *Transactions on Electrical And Electronic Materials*, vol. 14, no. 6, pp. 291–294, Dec. 2013.

[19] K. P. Pradhan, S. K. Mohapatra, P. K. Agarwal, P. K. Sahu, D. K. Behera, and J. Mishra, "Symmetric DG-MOSFET with gate and channel engineering: A 2-D simulation study," *Microelectronics and Solid State Electronics*, vol. 2, no. 1, pp. 1–9, Feb. 2013.

[20] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Investigation of Prefabrication Models of Double Gate MOSFETs in Nanoscale for High Performance Circuit Application," *Nano Trends: A Journal of Nanotechnology and Its Applications*, vol. 13, pp. 40–44, Oct. 2012.

[21] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Nanoscale SOI N-MOSFETS with different gate engineering having biaxial strained channel-a superlative study," *Journal of Electron Devices*, vol. 15, pp. 1261–1268, Sep. 2012.

Conference

[1] S. Panda, P. K. Sahu, D. Singh, K. P. Pradhan, and S. K. Mohapatra, "Performance comparison between ultrathin body (UTB) single and double gate MOSFETs," in *International Conference on Microelectronics, Communication and Computation, San Diego, USA. (Best Paper Award)*, Feb 2015, pp. 1–4.

[2] S. K. Mohapatra, K. P. Pradhan, P. K. Sahu, D. Singh, and S. Panda, "Ultra-Thin Si Directly on Insulator (SDOI) MOSFETs at 20 nm gate length," in *Proceedings of IEEE International Conference on High Performance Computing and Applications (ICHPCA), Bhubaneswar, Odisha, India*, Dec 2014, pp. 1–4.

[3] D. Singh, S. Panda, S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Static performance analysis on UTB-SG and DG MOSFETs with Si and III-V channel materials," in *Proceedings of IEEE International Conference on High Performance Computing and Applications (ICHPCA), Bhubaneswar, Odisha, India*, Dec 2014, pp. 1–6.

[4] D. Singh, S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Variation study of process parameters in Trigate SOI-FinFET," in *India Conference (INDICON), 2014 Annual IEEE*, Dec 2014, pp. 1–4.

[5] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Linearity and Analog Performance Analysis in GSDG-MOSFET with Gate and Channel Engineering," in *India Conference (INDICON), 2014 Annual IEEE*, Dec 2014, pp. 1–5.

[6] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Improved Performance in GS-DG-MOSFET with Dual Material Gate and Lateral Asymmetric Channel," in 16th *International Conference on Automatic Control, Modelling & Simulation , Brasov, Romania*, Jun. 2014, pp. 267–271.

[7] K. P. Pradhan, P. K. Agarwal, P. K. Sahu, and S. K. Mohapatra, "Role of high-k materials in Nanoscale TM-DG MOSFET: A simulation study," in 1st *National Conference on Recent Developments in Electronics, University of Delhi, South Campus, New Delhi, India*, Jan. 2013, pp. 1–3.

[8] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "A New Nanoscale DG MOSFET Design with Enhanced Performance-A Comparative Study," in 2nd *International Conference on Advances in Signal & Image Processing, Dubai, UAE*, Sep. 2012, pp. 77–82.

[9] P. K. Agarwal, K. P. Pradhan, S. K. Mohapatra, and P. K. Sahu, “Insulating layer parameters are still in reduction of kink,” in *Proceedings of IEEE Nirma University International Conference on Engineering*, Dec. 2012, pp. 1–4.

[10] K. P. Pradhan, P. K. Agarwal, S. K. Mohapatra, and P. K. Sahu, “The impact of high-k gate dielectric materials over short channel parameters on sub-100 nm MOSFET,” in 17th *National Seminar on Ferroelectrics & Dielectrics, Bhubaneswar, India.* SOA University, Dec. 2012, pp. 1–8.

[11] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, “Effect of channel & gate engineering on Double Gate (DG) MOSFET-A comparative study,” in *Proceedings of IEEE International Conference on Emerging Electronics, IIT, Bombay, India*, Dec. 2012, pp. 1–3.

[12] K. P. Pradhan, S. K. Mohapatra, and P. K. Sahu, “An analytical surface potential and threshold voltage model of fully depleted strained-SOI MOSFETs in nanoscale with high-k gate oxide,” in *Proceedings of IEEE* 1st *International Conference on Emerging Technology Trends in Electronics, Communication and Networking, Surat, Gujarat, India*, Dec., 2012, pp. 1–4.

[13] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, “Investigation of dimension effects of FD-S-SOI MOSFET in nanoscale,” in *Proceedings of IEEE* 1st *International Conference on Emerging Technology Trends in Electronics, Communication and Networking, Surat, Gujarat, India*, Dec., 2012, pp. 1–4.

Appendix

Appendix A

A. Effect of Strain on Band gap

In the presence of strain, the silicon thin film experiences biaxial tension that changes its band structure. The strain causes the electron affinity of silicon to increase and the band gap, the effective mass of carriers to decrease. The above strain-related effects on the silicon band structure are modeled as follows [127, 173–176].

$(E_C)_{s-Si} = 0.57X$ and $(E_g)_{s-Si} = 0.4X$

$$V_T Ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) = V_T Ln\left(\frac{m^*{}_{h,Si}}{m^*{}_{h,s-Si}}\right)^{\frac{3}{2}} \approx 0.075X \tag{1}$$

Effect of Strain on Flat band Voltage.

The effect of strain on the front-channel flat band voltage of FD-SOI MOSFET can be modeled as follows [174]:

$$(V_{FB,f})_{s-Si} = (V_{FB,f})_{Si} + V_{FB,f} \tag{2}$$

Where $(V_{FB,f})_{Si} = \varphi_M - \varphi_{Si}$

$V_{FB,f} = \frac{-(E_C)_{s-Si}}{q} + \frac{(E_g)_{s-Si}}{q} - V_T Ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$

$\varphi_{Si} = \frac{\chi_{Si}}{q} + \frac{E_{g,Si}}{2q} + \varphi_{F,Si}$, $\varphi_{F,Si} = V_T Ln\left(\frac{N_A}{n_{i,Si}}\right)$

In a similar way, the effect of strain on the back-channel flat band voltage of FD-SOI MOSFET is modeled as follows:

$$(V_{FB})_{s-Si} = (V_{FB})_{Si} + V_{FB,b} \tag{3}$$

Where $(V_{FB})_{Si} = \varphi_{sub} - \varphi_{Si}$ and

$V_{FB,b} = \frac{-(E_C)_{s-Si}}{q} + \frac{(E_g)_{s-Si}}{q} - V_T Ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$

It is also important to consider the effect of strain on the built-in voltage across the source-body and drain-body junctions in the strained-Si thin film, i.e.

$$V_{bi,s-Si} = V_{bi,si} + (V_{bi})_{s-Si} \tag{4}$$

Where $V_{bi,si} = \frac{E_{g,Si}}{2q} + \varphi_{F,Si}$, $(V_{bi})_{s-Si} = \frac{-(E_g)_{s-Si}}{q} + V_T Ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$

B. Surface Potential and Electric Field Model

Before the onset of strong inversion, the 2-D Poisson equation in the strained-silicon thin film of an FD-s-SOI MOSFET, shown in Fig. 3.1, can be written as follows [173, 174]:

$$\frac{d^2\varphi(x,y)}{dx^2} + \frac{d^2\varphi(x,y)}{dy^2} = \frac{qN_A}{\varepsilon_{Si}} \qquad \text{for} \quad 0 \le x \le L, 0 \le y \le t_{S-Si} \tag{5}$$

The potential profile in the vertical direction in the strained-Si film (y-direction in Fig. 3.1) can be approximated by a parabolic function, as done in [173, 174], i.e.

$$\varphi(x,y) = \varphi_s(x) + C_1(x)\,y + C_2(x)\,y^2 \qquad \text{for} \quad 0 \le x \le L, 0 \le y \le t_{S-Si} \tag{6}$$

Where the coefficients $c1(x)$ and $c2(x)$ are functions of x only. Equation (5) can be solved using the following boundary conditions:

Boundary conditions

1. Electric flux (displacement) at the gate oxide or strained-Si film interface is continuous, i.e.

$$\left[\frac{d\varphi(x,y)}{dy}\right]_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\left(\frac{\varphi_{s(x)} - V'_{GS}}{t_f}\right) \tag{7}$$

2. Electric flux at the interface of buried oxide and the back channel is continuous, i.e.

$$\left[\frac{d\varphi\left(x,y\right)}{dy}\right]_{y=t_{s-Si}}=\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\left(\frac{V'_{sub}-\varphi\left(x,t_{s-Si}\right)}{t_b}\right) \tag{8}$$

3. The substrate potential at the source end is

$$\varphi\left(0,0\right)=\varphi_s\left(0\right)=V_{bi,s-Si} \tag{9}$$

4. The surface potential at the drain end is

$$\varphi\left(L,0\right)=\varphi_s\left(L\right)=V_{bi,s-Si}+V_{DS} \tag{10}$$

Using the boundary conditions, one can obtain the coefficients$C_1(x)$ and $C_2(x)$ leading to an expression for $\varphi(x,y)$ and setting $y=0$, we obtain

$$\frac{d^2\varphi_s\left(x\right)}{dx^2}-\alpha\varphi_s\left(x\right)=\beta \tag{11}$$

Where $\propto=\frac{C_b}{t_{s-Si}\varepsilon_{Si}}\left(\frac{2C_{Si}+C_f}{2C_{Si}+C_b}\right)+\frac{C_f}{t_{s-Si}\varepsilon_{Si}}$

$\beta=\frac{qN_A}{\varepsilon_{Si}}-\left(\frac{C_b}{t_{s-Si}\varepsilon_{Si}}+\frac{C^2{}_b}{(2C_{Si}+C_b)t_{s-Si}\varepsilon_{Si}}\right)V'_{sub}-\left[\frac{C_b}{t_{s-Si}\varepsilon_{Si}}\left(\frac{C_f}{2C_{Si}+C_b}\right)+\frac{C_f}{t_{s-Si}\varepsilon_{Si}}\right]V'_{GS}$

Where $C_f=\frac{\varepsilon_{ox}}{t_f}$, $C_{Si}=\frac{\varepsilon_{Si}}{t_{s-Si}}$ and $C_b=\frac{\varepsilon_{ox}}{t_b}$

The above equation (11) with constant coefficients, can be written as

$$\varphi_s\left(x\right)=Aexp\left(\lambda x\right)+Bexp\left(-\lambda x\right)-\sigma \tag{12}$$

Where $\lambda=\sqrt{\alpha}$ and $\sigma=\frac{\beta}{\alpha}$. Now using boundary conditions to solve for A and B, we obtain

$A=\frac{[1-\exp(-\lambda l)](V_{bi,s-Si}+\sigma)+V_{DS}}{exp(\lambda l)-exp(-\lambda l)}$

$B=\frac{[1-\exp(\lambda l)](V_{bi,s-Si}+\sigma)+V_{DS}}{exp(-\lambda l)-exp(\lambda l)}$

Thus Electric Field can be calculated as

C. Threshold Equation Model

To obtain a model for the threshold voltage, we need to find the minimum surface potential from equation (12) by substituting

$$\frac{d\varphi_s\left(x\right)}{dx}=0 \tag{13}$$

This will be the minimum surface potential as

$$\varphi_{s,min}=2\sqrt{AB}-\sigma \tag{14}$$

The threshold voltage V_{th} is that value of the gate voltage V_{GS} at which a conducting channel is induced under the gate oxide at the surface of SOI MOSFET. In an FD thin-film SOI MOSFET, it is desirable that the front channel turns on before the back channel and that only the front channel contributes to the current conduction. Therefore, in a conventional unstrained silicon MOSFET, the threshold voltage is taken to be that value of gate to source voltage for which the front-channel surface potential $\varphi s,min=2_{\varphi F,Si}$, where $\varphi F,Si$ is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level [127, 173–176]. For the single-layer s-SOI MOSFET, the condition for threshold under the front gate is modified as

$$\varphi_{s,min}=2\varphi_{F,Si}+\Delta\varphi_{s-Si}=\varphi_{th} \tag{15}$$

Where $\Delta\varphi_{s-Si}=\frac{-(\Delta E_g)_{\mathrm{s-Si}}}{q}+V_TLn\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$

and φ_{th} is that value of surface potential at which the volumetric inversion electron charge density in the strained-Si device is the same as that in the unstrained-Si at threshold, i.e., equal to the body doping. Thus, the threshold voltage is defined as the value of V_{GS} at which the minimum surface potential φ_s,min equals φ_{th}. Hence, we can determine the value of threshold voltage by substituting (14) into (15) and solving for V_{GS} as [127, 174–176].

$$V_{th}=\frac{-K_2+\sqrt{K^2{}_2-4K_1K_3}}{2K_1} \tag{16}$$

where $K_1=b^2\left[4\left(N-N^2\right)-1\right]$

$K_2=b\left\{4\left(NV_{bi,s-Si}+M-2MN\right)-2\varphi_{th}\right\}+2ab\left\{4\left(N-N^2\right)-1\right\}$

$K_3=a\left\{4\left(NV_{bi,s-Si}+M-2MN\right)-2\varphi_{th}\right\}-\varphi^2{}_{th}-4\left(M^2-MV_{bi,s-Si}\right)+a^2\left\{4\left(N-N^2\right)-1\right\}$

$M=\frac{[1-exp(-\lambda l)]V_{bi,s-Si}+V_{DS}}{2sinhx}$, $N=\frac{1-exp(-\lambda l)}{2sinhx}$

$b=-\frac{1}{\alpha}\left[\frac{C_bC_f}{t_{s-Si}\varepsilon_{Si}(2C_{Si}+C_b)}+\frac{C_f}{t_{s-Si}\varepsilon_{Si}}\right]$

Appendix B

A. *Surface Potential Formulation*

Flat band voltage (front channel)

$$(V_{FB,f})_{si} = \phi_M - \phi_{si} \tag{1}$$

where $\phi_{f-Si} = V_T \ln({}^{N_a}\!/_{n_i})$, $\phi_{Si} = \frac{\chi_{si}}{q} + \frac{E_{g,Si}}{2q} + \phi_{f-Si}$

Back channel flat band voltage (back channel)

$$(V_{FB,b})_{si} = \phi_{sub} - \phi_{si} \tag{2}$$

where $\phi_{sub} = \frac{\chi_{si}}{q} + \frac{E_{g,Si}}{2q} + \phi_{f-sub}$, $\phi_{f-sub} = V_T \ln({}^{N_{sub}}\!/_{n_i})$

Built in voltage across source-body and drain body junction

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \phi_{f-Si} \tag{3}$$

Considering the effect of oxide charges in the $Si - SiO_2$ interface, 2-D Poisson's equation for the potential distribution in the silicon regions can be written as [35]:

$$\frac{\partial^2\phi_1(x,y)}{\partial x^2} + \frac{\partial^2\phi_1(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}} \quad \text{for} \ \ 0 \le x \le L_1, 0 \le y \le t_{Si} \tag{4}$$

$$\frac{\partial^2\phi_2(x,y)}{\partial x^2} + \frac{\partial^2\phi_2(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}} \quad \text{for} \ \ L_1 \le x \le L, 0 \le y \le t_{Si} \tag{5}$$

The potential profile in the vertical direction can be approximated by a parabolic function

$$\varphi_1(x,y) = \phi_{s1}(x) + a_{11}(x)y + a_{12}(x)y^2 \quad \text{for} \ \ 0 \le x \le L_1, 0 \le y \le t_{Si} \tag{6}$$

$$\varphi_2(x,y) = \phi_{s2}(x) + a_{12}(x)y + a_{22}(x)y^2 \quad \text{for} \ \ L_1 \le x \le L, 0 \le y \le t_{Si} \tag{7}$$

Poisson's equation can be solved by following the boundary condition

1. Electric flux(displacement) at the gate oxide/strained Si film interface is continuous

$$\left.\frac{d\varphi_1(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s1}(x) - V'_{GS1}}{t_f} \tag{8}$$

$$\left.\frac{d\varphi_2(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s2}(x) - V'_{GS2}}{t_f} \tag{9}$$

   where $V'_{GS1} = V_{GS} - (V_{FB1,f})_{si}$, $V'_{GS2} = V_{GS} - (V_{FB2,f})_{si}$
   and the effect of trapped charges are to be considered as
   $(V_{FB1,f})_{si} = \phi_M - \phi_{si}$, $(V_{FB2,f})_{si} = \phi_M - \phi_{si} - \frac{qN_f}{C_{ox}}$

2. Electric field at the interface of the buried oxide and the back channel is continuous

$$\left.\frac{d\varphi_2(x,y)}{dy}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{-\phi_B(x) + V'_{SUB}}{t_b} \tag{10}$$

$$\left.\frac{d\varphi_2(x,y)}{dy}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{-\phi_B(x) + V'_{SUB}}{t_b} \tag{11}$$

   where $V'_{GS1} = V_{GS} - (V_{FB1,f})_{si}$

3. Electric flux (displacement) and the electric potential at the trapped charged interface is continuous

$$\left.\frac{d\varphi_1(x,y)}{dx}\right|_{x=L_1} = \left.\frac{d\varphi_2(x,y)}{dx}\right|_{x=L_1} \tag{12}$$

$$\phi_1(L_1,0) = \phi_2(L_1,0) \tag{13}$$

4. The surface potential at the source end is

$$\phi_1(0,0) = \phi_{s1}(0) = V_{bi,si} \tag{14}$$

5. The surface potential at the drain end is

$$\phi_2(L,0) = \phi_{s2}(L) = V_{bi,si} + V_{DS} \tag{15}$$

Using the boundary conditions 8-11 we obtain coefficients and obtain the expressions for $\phi_1(x,y)$ and $\phi_2(x,y)$. Substituting $\phi_1(x,y)$ and $\phi_2(x,y)$ into 4 and 5 respectively and subsisting $y=0$ we obtain

$$\frac{d^2\phi_{s1}(x)}{dx^2} - \alpha\phi_{s1}(x) = \beta_1 \tag{16}$$

$$\frac{d^2\phi_{s2}(x)}{dx^2} - \alpha\phi_{s2}(x) = \beta_2 \tag{17}$$

where $\alpha = \frac{2(C_f C_{Si} + C_f C_b + C_b C_{si})}{t_{si}^2 C_{si}(2C_{si}+C_b)}$,
$\beta_1 = \frac{qN_A}{\varepsilon_{si}} - 2V'_{GS1}\frac{C_f(C_{si}+C_b)}{t_{si}^2 C_{si}(2C_{si}+C_b)} - 2V'_{SUB}\frac{C_b}{t_{si}^2 C_{si}(2C_{si}+C_b)}$
$\beta_2 = \frac{qN_A}{\varepsilon_{si}} - 2V'_{GS2}\frac{C_f(C_{si}+C_b)}{t_{si}^2 C_{si}(2C_{si}+C_b)} - 2V'_{SUB}\frac{C_b}{t_{si}^2 C_{si}(2C_{si}+C_b)}$

The solution for 16 and 17 are simple second order non-homogeneous differential equation with constant coefficients which can be expressed as

$$\phi_{s1}(x) = A\exp(nx) + B\exp(-n*x) - \frac{\beta_1}{\alpha} \tag{18}$$

$$\phi_{s2}(x) = C\exp(n(x-L_1)) + D\exp(-n(x-L_1)) - \frac{\beta_2}{\alpha} \tag{19}$$

where $n = \sqrt{\alpha}$, $p_1 = \frac{\beta_1}{\alpha}$, $p_2 = \frac{\beta_2}{\alpha}$

Using the boundary condition 15-18 we solve for A, B, C, and D

$$\begin{aligned} A = ((&V_{bi,si}(1-\exp(-nL)) + V_{DS} + (p_1-p_2)\cosh(nL_2) \\ &+p_2 - p_1\exp(-nL))/(2\sinh(nL)) \end{aligned} \tag{20}$$

$$\begin{aligned} B = ((&V_{bi,si}(\exp(nL)-1) + p_1\exp(nL) - p_2 - V_{DS} - (p_1-p_2)\cosh(nL_2)) \\ &/(2\sinh(nL)) \end{aligned} \tag{21}$$

$$C = A\exp(nL_1) + \frac{p_2 - p_1}{2} \tag{22}$$

$$D = B\exp(-nL_1) + (\frac{p_2-p_1}{2}) \tag{23}$$

B. Surface Potential Formulation

Electric field horizontal component under metal gates M1/M2 can be expressed as

$$E_1(x) = An\exp(nx) - Bn\exp(-nx) \tag{24}$$

$$E_2(x) = Cn\exp(n(x-L_1)) - Dn\exp(-n(x-L_1)) \tag{25}$$

The minimum potential of front channel can be expressed as

$$x_{\min} = \frac{1}{2n}\ln(\frac{B}{A}) \tag{26}$$

$$\phi_{s,\min} = 2\sqrt{AB} - p_1 \tag{27}$$

C. Threshold Voltage Formulation

For strained-Si SOI MOSFET the threshold condition under the front gate is modified as

$$\phi_{s,\min} = \phi_{th} = 2\phi_{f,si} \tag{28}$$

$$V_{TH} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma} \tag{29}$$

where $\gamma = \exp(-nL)$, $\sigma = \frac{1}{\gamma} + \gamma - 2 - \sinh^2(nL)$,
$V_{bi1} = V_{bi,si}(1-\gamma) + V_{DS} - (u-v)\cosh(nL_2) - v + u\gamma$,
$V_{bi2} = V_{bi,si}(\frac{1}{\gamma} - 1) - V_{DS} + (u-v)\cosh(nL_2) + v - \frac{u}{\gamma}$,
$u = \frac{C_b}{C_f}V'_{SUB} - \frac{qN_A t_{si}}{C_f} - V_{FB1,si}$ $v = \frac{C_b}{C_f}V'_{SUB} - \frac{qN_A t_{si}}{C_f} - V_{FB2,si}$,
$\xi = V_{bi1}V_{bi2} - \sinh^2(nL)(\phi_{th} - u)^2$,
$\eta = V_{bi1}(-\frac{1}{\gamma} + 1) + 2\sinh^2(nL)(\phi_{th} - u) - V_{bi2}(1-\gamma)$

Appendix C

SIMULATION METHODOLOGY

A. Working Principle for Sentaurus TCAD

Modeling and simulation bridge the need for development and fabrication engineers by improving semiconductor process control in manufacturing. Sentaurus TCAD is a powerful GUI-driven simulation environment for managing simulation tasks and analyzing results. Sentaurus TCAD simulations afford crucial insights on the nature of semiconductor devices, which can lead to new concepts. However, it needs to be properly calibrated for simulation.

Advantages of Sentaurus TCAD

- Reduces technology development time and cost.
- Provides full flow 3-D process and device simulation with advanced structure generation, meshing, and numeric.
- Supports insight into advanced physical phenomena, improving device design, yield, and reliability.
- Provides fast prototyping, development and optimization of semiconductor technologies.

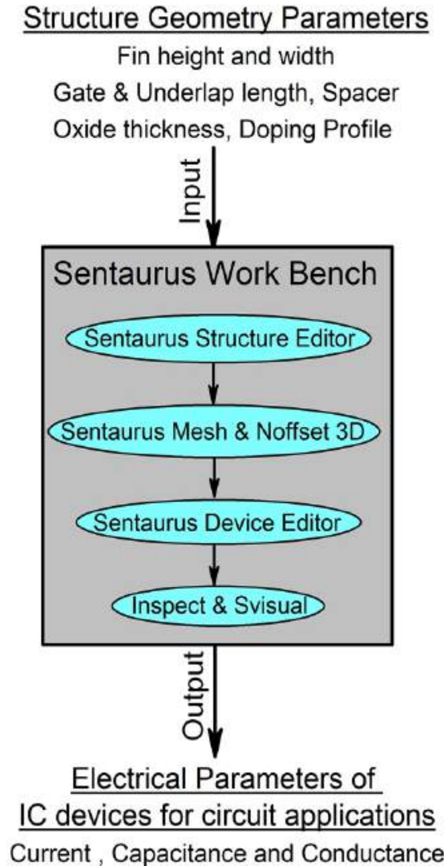

Figure 1: Simulation procedure in Sentaurus TCAD

Fig. 1 demonstrates the complete flow chart of working principle of Sentaurus TCAD i.e., creation of the device structure (including the doping profiles), and definition of the electrical contact are done through Sentaurus Structure Editor. Sentaurus Mesh and Noffset-3D generates the meshing for solving diffusion and transport equations through validation of various physical models (like bandgap narrowing, Fermi-Dirac, Band-to-Band tunneling, Drift-Diffusion, carrier mobility and velocity saturation). Sentaurus Device solves multiple, coupled physical equations based on the meshing, to properly estimate the device performance. Sentaurus Inspect and SVISUAL used to extract critical device performance parameters.

Physical Models and Methods Considered for this Work

The technology parameters and the supply voltages used for the device simulations are according to the analog ITRS roadmap [7] for below 50 nm gate length devices. The V_{DD} is

taken as 0.7 V. The work functions of the metal gates are adjusted to achieve the desired V_{th} value. The numerical simulation uses the drift-diffusion approach [138] and the models activated in simulation comprise of field dependent mobility, concentration Dependant mobility and velocity saturation model [139]. Suitable empirical parameter β is selected to calibrate the drift-diffusion transport model. The inversion layer mobility models Lombardi (constant voltage and temperature, CVT) [177], along with Shockley-Read-Hall (SRH) [140, 141] and Auger recombination models are included.

The silicon bandgap narrowing model which determines the intrinsic carrier concentration is actuated. A set of partial differential equations for the modeled device solves self-consistently on the discrete mesh in an iterative fashion. The currents, voltages and charges for each electrode are calculated after each step of bias ramp through quasi-stationary. The Poisson equation, continuity equations, and the different thermal and energy equations are included in the simulation [123]. All the structure junctions are assumed as abrupt, the biasing conditions are reckoned at room temperature and the generation of smooth mesh [142] is done in the simulation. The simulated results of FinFETs at low (50 mV) and high (0.35 V) drain biases are analyzed further.

Sentaurus Device Editor Code for FinFET

```
(define Lg 0.020)
(define Lus 0.005)
(define Lud 0.005)
(define Wstrip 0.007)
(define Hstrip 0.030)
(define Na 1e15) ; Body doping [cm-3] ;
Na= 1e17, 1e16, 1e15
(define Nsd 1e20) ; Body doping [cm-3]
(sdegeo:set-default-boolean "ABA")

(sdegeo:create-cuboid (position 1 1 1) (position (+ 1.08 Lus Lg Lud) 0.93 (+ Wstrip 1.0252)
"Silicon" "substrate.region"))
(sdegeo:create-cuboid (position 1 0.93 1) (position (+ 1.08 Lus Lg Lud) 0.89 (+ Wstrip
1.0252)) "SiO2" "box.region")
(sdegeo:create-cuboid (position 1.04 0.89 1) (position (+ 1.04 Lus) (- 0.8774 Hstrip) (+ Wstrip
1.0252)) "HfO2" "metals.region")
(sdegeo:create-cuboid (position (+ 1.04 Lus Lg) 0.89 1) (position (+ 1.04 Lus Lg Lud) (-
0.8774 Hstrip) (+ Wstrip 1.0252)) "HfO2" "metald.region")
(sdegeo:create-cuboid (position (+ 1.04 Lus) 0.89 1) (position (+ 1.04 Lus Lg) (- 0.8774
Hstrip) (+ Wstrip 1.0252)) "Metal" "copper.region")
(sdegeo:create-cuboid (position (+ 1.04 Lus) 0.89 1.0117) (position (+ 1.04 Lus Lg) (- 0.8891
Hstrip) (+ Wstrip 1.0135)) "SiO2" "sio2.region") (sdegeo:create-cuboid (position 1 0.89
1.0126) (position (+ 1.08 Lus Lg Lud) (- 0.89 Hstrip) (+ Wstrip 1.0126)) "Silicon"
"insertedsilicon.region")

(sdegeo:define-contact-set "source" 4.0 (color:rgb 1 1 0) "–")
(sdegeo:set-current-contact-set "source")
(sdegeo:define-3d-contact (find-face-id (position 1.02 (- 0.89 Hstrip) (+ Wstrip 1.0125)))
"source")
(sdegeo:define-contact-set "drain" 4.0 (color:rgb 0 1 1) "–")
(sdegeo:set-current-contact-set "drain")
(sdegeo:define-3d-contact (find-face-id (position (+ 1.06 Lus Lg Lud) (- 0.89 Hstrip) (+ Wstrip
1.0125))) "drain")
(sdegeo:define-contact-set "substrate" 4.0 (color:rgb 1 0 1) "–")
(sdegeo:set-current-contact-set "substrate")
(sdegeo:define-3d-contact (find-face-id (position (+ 1.06 Lus Lg Lud) 1 1.001)) "substrate")
(sdegeo:define-contact-set "gate" 4.0 (color:rgb 0 1 1) "–")
(sdegeo:set-current-contact-set "gate")
(sdegeo:define-3d-contact (list (car (find-face-id (position (+ 1.041 Lus) (- 0.8774 Hstrip)
1.001))) (car (find-face-id (position (+ 1.041 Lus) (- 0.8776 Hstrip) (+ Wstrip 1.0252)))) (car
(find-face-id (position (+ 1.041 Lus) (- 0.8776 Hstrip) 1)))) "gate")
(sdedr:define-refeval-window "ssource" "Cuboid" (position 1 0.89 1.0126) (position 1.04 (- 0.89
Hstrip) (+ 1.0126 Wstrip)))
(sdedr:define-constant-profile "arsenic.doping" "ArsenicActiveConcentration" Nsd)
(sdedr:define-constant-profile-placement "placementsource.ap" "arsenic.doping" "ssource")
(sdedr:define-refeval-window "sdrain" "Cuboid" (position (+ 1.04 Lus Lg Lud) 0.89 1.0126)
```

```
(position (+ 1.08 Lus Lg Lud) (- 0.89 Hstrip) (+ 1.0126 Wstrip)))
(sdedr:define-constant-profile-placement "placementdrain.ap" "arsenic.doping" "sdrain")
(sdedr:define-refeval-window "schannel" "Cuboid" (position (+ 1.04 Lus) 0.89 1.0126) (position (+ 1.04 Lus Lg) (- 0.89 Hstrip) (+ 1.0126 Wstrip)))
(sdedr:define-constant-profile "boron.doping" "BoronActiveConcentration" Na)
(sdedr:define-constant-profile-placement "placementchannel.ap" "boron.doping" "schannel")

(sdedr:define-refinement-size "mesh.dimen" 0.08 0.08 0.08 0.24 0.24 0.24)
(sdedr:define-refinement-placement "meshs.ap" "mesh.dimen" "ssource")
(sdedr:define-refinement-placement "meshd.ap" "mesh.dimen" "sdrain")
(sdedr:define-refinement-size "mesh1.dimen" 0.008 0.008 0.008 0.024 0.024 0.024)
(sdedr:define-refinement-placement "meshc.ap" "mesh1.dimen" "schannel")
(sde:set-meshing-command "snmesh -a -c boxmethod")
(sdedr:append-cmd-file "")
(sde:build-mesh "snmesh" "-a -c boxmethod" "sdemodel")
(sdedr:write-cmd-file "@commands/o@")
(sde:build-mesh "snmesh" " " "n@node@msh")
```

Sentaurus Device Command Code for FinFET

```
Sentaurus Device command file for Id versus Vg
USING DRIFT-DIFUSSION MODEL

File { Grid = "@tdr@"
Plot = "@tdrdat@"
Current = "@plot@"
Output = "@log@" }

Electrode { { Name="source" Voltage=0.0 }
{ Name="drain" Voltage=0.0 }
{ Name="gate" Voltage=0.0 }
{ Name="substrate" Voltage=0.0 }}

* DriftDiffusion
Physics (Material = "Metal") { MetalWorkFunction ( WorkFunction = @Wf@)}
Physics{ eQCvanDort EffectiveIntrinsicDensity( OldSlotboom ) Mobility( DopingDep eHighFieldsaturation( GradQuasiFermi ) hHighFieldsaturation( GradQuasiFermi ) Enormal) Recombination(SRH(DopingDep TempDependence ))}

Math { Extrapolate Iterations=220 Notdamped =100
RelErrControl ErRef(Electron)=1.e10 ErRef(Hole)=1.e10 }

Plot{ *–Density and Currents, etc eDensity hDensity TotalCurrent/Vector eCurrent/Vector hCurrent/Vector eMobility hMobility eVelocity hVelocity ElectricField Potential SpaceCharge eQuasiFermi hQuasiFermi
*–Temperature eTemperature Temperature hTemperature
*–Fields and charges ElectricField/Vector Potential SpaceCharge
*–Doping Profiles Doping DonorConcentration AcceptorConcentration
*–Band structure/Composition
BandGap BandGapNarrowing Affinity
ConductionBand ValenceBand eQuantumPotential hQuantumPotential}

Solve { *- Creating initial guess:
Coupled(Iterations= 100) Poisson
Coupled Poisson Electron Hole
*- Ramp to drain to Vd
Quasistationary( InitialStep= 0.1 Decrement= 1.5 MinStep= 1e-5 MaxStep= 1 Goal { Name="drain" Voltage=@Vd@ } ){ Coupled {Poisson Electron Hole} }
*- Vg sweep NewCurrentFile="IdVg"
Quasistationary(
DoZero InitialStep= 0.005 Decrement= 1.5 MinStep= 1e-5 MaxStep= 0.001 Goal Name="gate" Voltage= 1.0 ){ Coupled Poisson Electron Hole CurrentPlot (time=(range = (0 1) intervals=40))}}

Sentaurus Device command file for Id versus Vg
USING DRIFTDIFUSSION MODEL

File { Grid = "@tdr@"
Plot = "@tdrdat@"
Current = "@plot@"
```

Output = "@log@" }

Electrode { { Name="source" Voltage=0.0 } { Name="drain" Voltage=0.0 } { Name="gate" Voltage=0.0 } { Name="substrate" Voltage=0.0 }}

* DriftDiffusion
Physics (Material = "Metal") { MetalWorkFunction (WorkFunction = 4.3)}
Physics{ eQCvanDort EffectiveIntrinsicDensity(OldSlotboom) Mobility(DopingDep eHighFieldsaturation(GradQuasiFermi) hHighFieldsaturation(GradQuasiFermi) Enormal) Recombination(SRH(DopingDep TempDependence)) }

Math { Extrapolate Iterations=500 Notdamped =100 RelErrControl ErRef(Electron)=1.e10 ErRef(Hole)=1.e10 }

Plot{ *–Density and Currents, etc eDensity hDensity TotalCurrent/Vector eCurrent/Vector hCurrent/Vector eMobility hMobility eVelocity hVelocity ElectricField Potential SpaceCharge eQuasiFermi hQuasiFermi
*–Temperature eTemperature Temperature hTemperature
*–Fields and charges ElectricField/Vector Potential SpaceCharge
*–Doping Profiles Doping DonorConcentration AcceptorConcentration
*–Band structure/Composition BandGap BandGapNarrowing Affinity ConductionBand ValenceBand eQuantumPotential hQuantumPotential}

Solve { initial gate voltage Vgs=0.35 V
Poisson Coupled { Poisson Electron }
Coupled { Poisson Electron }
Save (FilePrefix="vg0")
ramp gate and save solutions:
second gate voltage Vgs=0.7 V
Quasistationary
(InitialStep=0.1 Maxstep=0.1 MinStep=0.01 Increment=1.3 Goal name="gate" voltage=0.7) Coupled Poisson Electron Save(FilePrefix="vg1")
third gate voltage Vgs=1.0 V Quasistationary (InitialStep=0.1 Maxstep=0.1 MinStep=0.01 Increment=1.3
Goal { name="gate" voltage=1.0 }) { Coupled { Poisson Electron } } Save(FilePrefix="vg2")

Load saved structures and ramp drain to create family of curves:first curve
Load(FilePrefix="vg0")
NewCurrentPrefix="vg0"
Quasistationary (InitialStep=0.1 Maxstep=0.1 MinStep=0.01 Goal{ name="drain" voltage=1.0}){ Coupled {Poisson Electron } CurrentPlot (time=(range = (0 1) intervals=40))}

second curve
Load(FilePrefix="vg1")
NewCurrentPrefix="vg1"
Quasistationary (InitialStep=0.1 Maxstep=0.1 MinStep=0.01 Goal{ name="drain" voltage=1.0 }){Coupled {Poisson Electron } CurrentPlot (time=(range = (0 1) intervals=40))}

third curve Load(FilePrefix="vg2")
NewCurrentPrefix="vg2"
Quasistationary (InitialStep=0.1 Maxstep=0.1 MinStep=0.01 Goal{ name="drain" voltage=1.0 }){ Coupled {Poisson Electron } CurrentPlot (time=(range = (0 1) intervals=40))}}

Device NMOS { Electrode { { name="source" Voltage=0.0 } { name="drain" Voltage=0.0 } { name="gate" Voltage=0.0 } { Name="substrate" Voltage=0.0 }}

File { Grid = "@tdr@"
Plot = "@tdrdat@"
Current = "@plot@"}

Physics { Mobility(DopingDep HighFieldSaturation Enormal) EffectiveIntrinsicDensity(oldSlotboom)}}

Math { Extrapolate RelErrControl Notdamped=50 Iterations=20}

Plot { eDensity hDensity eCurrent hCurrent ElectricField eEnormal hEnormal eQuasiFermi hQuasiFermi Potential Doping SpaceCharge SRH Auger AvalancheGeneration eMobility

hMobility DonorConcentration AcceptorConcentration Doping eVelocity hVelocity}

File { Output = "@log@"
ACExtract = "@acplot@"}
System { NMOS nmos1 (drain=d source=s gate=g substrate=b)
Vsource-pset vd (d 0){ dc = 0 } Vsource-pset vs (s 0){ dc = 0 } Vsource-pset vg (g 0){ dc = 0 } Vsource-pset vb (b 0){ dc = 0 }}

Solve { NewCurrentPrefix="init"
Coupled(Iterations=100){ Poisson }
Coupled{ Poisson Electron Hole }
*- Ramping gate to starting operating point:
Quasistationary(InitialStep= 0.01 Increment= 1.4 MinStep= 1e-6 MaxStep= 0.25 Goal{ Parameter= vg.dc Voltage= 0} Goal{ Parameter= vd.dc Voltage= @Vd@ }){ Coupled { Poisson Electron Hole } }
ramp gate
NewCurrentPrefix=""
Quasistationary (InitialStep=0.01 Increment=1.3 MaxStep=0.05 Minstep=1.e-5
Goal { Parameter=vg.dc Voltage=0.7})

{ ACCoupled (StartFrequency=1e6 EndFrequency=1e6 NumberOfPoints=1 Decade Node(d s g b) Exclude(vd vs vg vb) ACCompute (Time = (Range = (0 1) Intervals = 40))){ Poisson Electron Hole }}}

B. SILVACO'S ATLAS Device Simulator

ATLAS is Silvaco International's primary TCAD device simulator and has the ability to model devices of many different materials and physical characteristics [Ref–Silvaco atlas manual]. The ATLAS simulator is activated by using Silvaco's Deckbuild operating environment. Devices can either be completely constructed in Deckbuild to be run by ATLAS or they can be built using Silvaco's ATHENA device frame work simulator. Fig. 2 shows a flow chart that describes how the different programs of Silvaco's TCAD suite interact with the ATLAS device simulator.

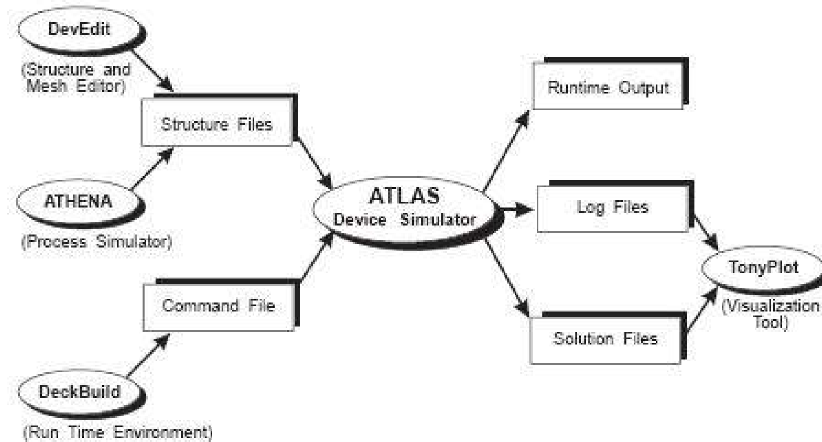

Figure 2: Modules of Silvaco

Modes of Operation

All simulations in this thesis were run using Deckbuild to provide the device structure information to the device simulator ATLAS. ATLAS has the ability to run in several different modes that are with Deckbuild including Interactive Mode. Each time to run ATLAS inside Deckbuild the first programming line should be:

go atlas

This input will start ATLAS simulator and allow it to input the rest of the conditions stated in the code in Deckbuild.

Silvaco breaks the commands into five groups and each group will have several statements in that group. The statements in each group in most cases must be run in order. Fig. 3 shows the groups and the order in which they should be inputted into Deckbuild.

The key parameters in the structure command group include the following; a two or three dimensional grid, called the mesh, the mesh must be divided into regions, electrode locations

Group	Statements
1. Structure Specification	MESH REGION ELECTRODE DOPING
2. Material Models Specification	MATERIAL MODELS CONTACT INTERFACE
3. Numerical Method Selection	METHOD
4. Solution Specification	LOG SOLVE LOAD SAVE
5. Results Analysis	EXTRACT TONYPLOT

Figure 3: Five groups of Atlas

and materials must be defined, doping levels and dopants must be defined. Mesh statements are entered in as vertical and horizontal lines in microns and as distance from the center line. ATLAS will automatically adjust the grids to represent the desired resolution the user has entered.

The next have to define the regions of the device. The regions will be used to assign materials and properties to the device. The regions must be defined along the mesh lines and the statements will be similar to those used for the mesh statements. The designer must specify the electrode name and where it is located. The next action, doping, is one of the most important actions a designer does to affect the electrical properties of the structure they are designing. Silvaco allow the designer to specify the type of dopant and the concentration. It also allows the designer to specify the distribution of the doping material. ATLAS has the ability to distribute the dopants in a uniform or Gaussian profile.

The next statement to investigate is the models statement. ATLAS has over seventy models that a designer can choose to use to improve the accuracy of the structure they are trying to simulate. These models would change the parameters of the device using the following command statements: models, mobility, impact, and material. ATLAS allows several different methods for calculating the solution for semiconductor device problems. For each model type there are three types of solution techniques: decoupled, fully coupled and block.

The method to view the results of a simulation is using Tonyplot. It is viewing program for ATLAS that allows the designer to view the structure and log files that are created by ATLAS. The structure files allow you to view the mesh diagram, doping concentrations, current densities, and other parameters. The log files allow you to view the results of ATLAS's electrical analysis in a graph format. It can show both log and linear scaling. It can also produce cylindrical graphs. Tonyplot has the ability to do cutlines to look at a specific slice of the device and see what is electrical occurring at the slice point or plane.

DECKBUILD CODING FOR ATLAS

Atlas code for DG-MOSFET under study for various performance analyses

```
go atlas
*********** define the mesh *****
mesh space.mult=1.0
x.mesh loc=0.000 spac=0.01
x.mesh loc=0.030 spac=0.01
x.mesh loc=0.0399 spac=0.01
x.mesh loc=0.040 spac=0.001
x.mesh loc=0.080 spac=0.001
x.mesh loc=0.0801 spac=0.01
x.mesh loc=0.090 spac=0.01
x.mesh loc=0.120 spac=0.01

y.mesh loc=0.000 spac=0.1
y.mesh loc=0.001 spac=0.1
y.mesh loc=0.0019 spac=0.1
y.mesh loc=0.002 spac=0.0002
y.mesh loc=0.012 spac=0.0002
```

```
y.mesh loc=0.0121 spac=0.1
y.mesh loc=0.013 spac=0.1
y.mesh loc=0.014 spac=0.1

TITLE GS-DG
region num=1 x.min=0.000 x.max=0.120 y.min=0.002 y.max=0.012 material=silicon
region num=2 x.min=0.000 x.max=0.120 y.min=0.000 y.max=0.001 material=Air
region num=3 x.min=0.000 x.max=0.120 y.min=0.001 y.max=0.002 material=SiO2
region num=4 x.min=0.000 x.max=0.120 y.min=0.012 y.max=0.013 material=SiO2
region num=5 x.min=0.000 x.max=0.120 y.min=0.013 y.max=0.014 material=Air

*********** define the electrodes ************
electrode name=fgate x.min=0.040 x.max=0.080 y.min=0.000 y.max=0.000
electrode name=bgate x.min=0.040 x.max=0.080 y.min=0.014 y.max=0.014
electrode name=source x.min=0.000 x.max=0.000 y.min=0.002 y.max=0.012
electrode name=drain x.min=0.120 x.max=0.120 y.min=0.002 y.max=0.012
contact name=fgate workfunction=4.8
contact name=bgate workfunction=4.8
contact name=bgate common=fgate

*********** define the doping concentrations *****
doping uniform conc=1e16 p.type x.min=0.040 x.max=0.080 y.min=0.002 y.max=0.012
doping uniform conc=1e20 n.type x.min=0.000 x.max=0.040 y.min=0.002 y.max=0.012
doping uniform conc=1e20 n.type x.min=0.080 x.max=0.120 y.min=0.002 y.max=0.012
save outf=GS-DG.str
go atlas
TITLE DM-GS-DG
region num=1 x.min=0.000 x.max=0.120 y.min=0.002 y.max=0.012 material=silicon
region num=2 x.min=0.000 x.max=0.120 y.min=0.000 y.max=0.001 material=Air
region num=3 x.min=0.000 x.max=0.120 y.min=0.001 y.max=0.002 material=SiO2
region num=4 x.min=0.000 x.max=0.120 y.min=0.012 y.max=0.013 material=SiO2
region num=5 x.min=0.000 x.max=0.120 y.min=0.013 y.max=0.014 material=Air

*********** define the electrodes ************
electrode name=fgate top x.min=0.040 x.max=0.060
electrode name=gate1 top x.min=0.060 x.max=0.080
electrode name=bgate bottom x.min=0.040 x.max=0.060
electrode name=gate2 bottom x.min=0.060 x.max=0.080
electrode name=source x.min=0.000 x.max=0.000 y.min=0.002 y.max=0.012
electrode name=drain x.min=0.120 x.max=0.120 y.min=0.002 y.max=0.012

contact name=fgate workfunction=4.8
contact name=gate1 common=fgate workfunction=4.6
contact name=bgate workfunction=4.8
contact name=gate2 common=bgate workfunction=4.6
contact name=bgate common=fgate

*********** define the doping concentrations *****
doping uniform conc=1e16 p.type x.min=0.040 x.max=0.080 y.min=0.002 y.max=0.012
doping uniform conc=1e20 n.type x.min=0.000 x.max=0.040 y.min=0.002 y.max=0.012
doping uniform conc=1e20 n.type x.min=0.080 x.max=0.120 y.min=0.002 y.max=0.012
save outf=DM-GS-DG.str

go atlas
TITLE DM-GS-DG-SH
mesh space.mult=1.0
region num=1 x.min=0.000 x.max=0.120 y.min=0.002 y.max=0.012 material=silicon
region num=2 x.min=0.000 x.max=0.120 y.min=0.000 y.max=0.001 material=Air
region num=3 x.min=0.000 x.max=0.120 y.min=0.001 y.max=0.002 material=SiO2
region num=4 x.min=0.000 x.max=0.120 y.min=0.012 y.max=0.013 material=SiO2
region num=5 x.min=0.000 x.max=0.120 y.min=0.013 y.max=0.014 material=Air

*********** define the electrodes ************
electrode name=fgate top x.min=0.040 x.max=0.060
electrode name=gate1 top x.min=0.060 x.max=0.080
electrode name=bgate bottom x.min=0.040 x.max=0.060
electrode name=gate2 bottom x.min=0.060 x.max=0.080
electrode name=source x.min=0.000 x.max=0.000 y.min=0.002 y.max=0.012
electrode name=drain x.min=0.120 x.max=0.120 y.min=0.002 y.max=0.012

contact name=fgate workfunction=4.8
contact name=gate1 common=fgate workfunction=4.6
contact name=bgate workfunction=4.8
```

```
contact name=gate2 common=bgate workfunction=4.6
contact name=bgate common=fgate

*********** define the doping concentrations *****
doping uniform conc=1e18 p.type x.min=0.040 x.max=0.050 y.min=0.002 y.max=0.012
doping uniform conc=1e16 p.type x.min=0.050 x.max=0.080 y.min=0.002 y.max=0.012
doping uniform conc=1e20 n.type x.min=0.000 x.max=0.040 y.min=0.002 y.max=0.012
doping uniform conc=1e20 n.type x.min=0.080 x.max=0.120 y.min=0.002 y.max=0.012
save outf=DM-GS-DG-SH.str

go atlas
TITLE DM-GS-DG-DH
region num=1 x.min=0.000 x.max=0.120 y.min=0.002 y.max=0.012 material=silicon
region num=2 x.min=0.000 x.max=0.120 y.min=0.000 y.max=0.001 material=Air
region num=3 x.min=0.000 x.max=0.120 y.min=0.001 y.max=0.002 material=SiO2
region num=4 x.min=0.000 x.max=0.120 y.min=0.012 y.max=0.013 material=SiO2
region num=5 x.min=0.000 x.max=0.120 y.min=0.013 y.max=0.014 material=Air

*********** define the electrodes ************
electrode name=fgate top x.min=0.040 x.max=0.060
electrode name=gate1 top x.min=0.060 x.max=0.080
electrode name=bgate bottom x.min=0.040 x.max=0.060
electrode name=gate2 bottom x.min=0.060 x.max=0.080
electrode name=source x.min=0.000 x.max=0.000 y.min=0.002 y.max=0.012
electrode name=drain x.min=0.120 x.max=0.120 y.min=0.002 y.max=0.012

contact name=fgate workfunction=4.8
contact name=gate1 common=fgate workfunction=4.6
contact name=bgate workfunction=4.8
contact name=gate2 common=bgate workfunction=4.6
contact name=bgate common=fgate

*********** define the doping concentrations *****
doping uniform conc=1e18 p.type x.min=0.040 x.max=0.050 y.min=0.002 y.max=0.012
doping uniform conc=1e16 p.type x.min=0.050 x.max=0.070 y.min=0.002 y.max=0.012
doping uniform conc=1e18 p.type x.min=0.070 x.max=0.080 y.min=0.002 y.max=0.012
doping uniform conc=1e20 n.type x.min=0.000 x.max=0.040 y.min=0.002 y.max=0.012
doping uniform conc=1e20 n.type x.min=0.080 x.max=0.120 y.min=0.002 y.max=0.012
save outf=DM-GS-DG-DH.str

MATERIAL MATERIAL=Air
MATERIAL MATERIAL=Air PERMITTIVITY=24
Models activated for Miscellaneous Device Design
models CVT SRH FERMIDIRAC AUGER print
method gummel newton
Models activated for Trap Charge and Temperature
interface y.max=0.004 qf=4e11 s.n=1e4 s.p=1e4
interface y.min=0.006 qf=4e11 s.n=1e4 s.p=1e4
models Temperature=400, 300, 200, 100 print
method gummel newton

solve init
Id-Vg Characteristics
log outfile=gatesweep1.log master
solve name=fgate vfgate=0 vstep=0.025 vfinal=1.0 vdrain=0.1
output band.param band.temp charge e.field e.velocity e.mobility
save outf=GS-DG-1.str master

log outfile=gatesweep2.log master
solve name=fgate vfgate=0 vstep=0.025 vfinal=1.0 vdrain=0.5
output band.param band.temp charge e.field e.velocity e.mobility
save outf=GS-DG-2.str master

log off
solve init
Id-Vd Characteristics
log outfile=drainsweep1.log master
solve name=drain vdrain=0 vstep=0.025 vfinal=1 vfgate=0.5

log off
Leakage Current
solve init
log outfile=GS-DG-Leakagedrainsweep1.log
solve name=drain vdrain=0 vstep=0.025 vfinal=0.5 vfgate=0
```

```
log off
solve init
log outfile= AC-1.log master
solve name=fgate vfgate=0 vstep=0.025 vfinal=1 vdrain=0.5 ac freq=1.0e6 fstep=10 mult.f
nfstep=5 VSS=0.01 previous

extraction of Vt,SS,Gm,Ion.
extract init inf=" gatesweep1.log"
extract name=" nvt1" x.val from curve (abs(v."fgate"),abs(i."drain")) where y.val=1e-6
extract name=" SS1" 1.0/slope(maxslope(curve(abs(v."fgate"),log10(abs(i."drain")))))
extract name=" gm1" slope(maxslope(curve(abs(v."fgate"),abs(i."drain"))))
extract name=" Ion1" max(i."drain")
extract name="dydx" deriv(v."fgate",i."drain") outfile="Gm1.dat"

extraction Id-Vd
extract init inf="drainsweep1.log"
extract name=" gd1" slope(maxslope(curve(abs(v."drain"),abs(i."drain"))))
extract name="dydx" deriv(v."drain",i."drain") outfile="Gd1.dat"
extraction of Ioff
extract init inf="Leakagedrainsweep1.log"
extract name="GS-DG-Ioff1" max(i."drain")

TONYPLOT
tonyplot overlay gatesweep1.log
gatesweep2.log
tonyplot Gm1.dat
tonyplot drainsweep1.log
tonyplot Gd1.dat
tonyplot Leakagedrainsweep1.log
quit
```