Mathematical modeling of Source/Drain extension regions in SOI MOSFETs.

A thesis submitted in partial fulfilment of
the requirement for the degree of

B.Tech

by

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Under the guidance of

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Certificate

This is to certify that the thesis entitled "**Mathematical Modeling of Source/Drain extension region in SOI MOSFETs**", submitted by Rahul Kumar to National Institute of Technology Rourkela, is a record of bonafide research work carried under my supervision and is worthy of consideration for the award of the degree of Doctor of Philosophy of the Institute. The research reports and the results presented in this thesis have not been submitted in parts or in full to any other University or Institute for the award of any other degree or diploma.

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Working on a project is like filling the gap between theoretical and practical working of the real world things. With this inspiration in my mind I started working on this project to get an insight into the working of the MOSFETs and how the device and circuit simulators works.

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ABSTRACT

Silicon-on-insulator has been used drastically in the CMOS technology due to its excellent properties. It has drastically reduced short channel effects. Also FD SOI MOSFET due to its superior scalability property than bulk MOSFET led to its extensive use in mixed-mode circuits.

However, as we scale the device below the 65-nm t node, the devices face serious short channel effects in SOI MOSFETs in addition to other challenges. It seriously degrades analog figure of merit such as transconductance and cutoff frequency etc. There have been several proposed solution to this problem like laterally asymmetric-channel or graded-channel design. But in the case of nanoscale device, it is impossible to control the concentration profile at the source and the drain region.

In the last few years, there have been several modeling approach to study these effects and propose a suitable model. However, the reduction in channel length have been the main problem.

In case of bulk MOSFETs, charge sharing effects is negligible from Source/Drain regions due to better control of the active part of the device by the front gate. As now the thickness of the channel region is reduced to the order of 10 nm, it is difficult to fabricate the device and study the channel region without considering the effect of source/Drain doping gradient in the channel region. In the present work we have taken into account this effect and have effectively modeled the channel region to study the device in the weak inversion region.

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List of important symbols

Substrate doping concentration	N_{asub}	Drain doping concentration	N_d
Silicon-body doping concentration	N_a	Source doping concentration	Ns
Channel length	L	Front-gate flat-band voltage	V_{fb}
Drain to source voltage	V_{DS}	Threshold voltage	V_{th}
Gate voltage	V_g	Electrostatic potential in the silicon-body	$\psi(x,y)$
Built-in potential	Vbi	Front-gate surface potential at the gate-oxide-silicon- body interface	ψ_f
Buried-oxide thickness	t_{box}	Back-gate surface potential at the silicon-body buried- oxide interface	ψ_b
Silicon oxide thickness	t_{Si}		

Chapter I

Introduction

SOI MOSFET

Silicon on insulator (SOI) is the introduction of a thin layer of insulator above the substrate in between the channel and substrate in the conventional MOSFETs so that channel is followed by the insulator and then the substrate in the device structure during the semiconductor manufacturing. It drastically reduces parasitic capacitance of the device and hence improving the device performance. Usually silicon dioxide is used as the insulator and now the silicon channel is above this layer. We can also choose a different material for the insulator layer which depends on the application of the device. Sapphire is usually used for radiation-sensitive applications and radio frequency based devices whereas silicon dioxide for reducing the short channel effects in devices.

SOI MOSFET can be of two types:

- Partially depleted SOI MOSFET
- Fully depleted SOI MOSFETs.

Partially depleted SOI MOSFET:
In case of the n-type PDSOI MOSFET, the thickness of p-type silicon channel is large enough. Hence, the depletion region is not formed in the complete channel region. Due to presence of depletion region in few portion of the channel region, PDSOI MOSFET behaves like bulk MOSFET. But it has some advantages over the conventional MOSFETs.

Fully depleted SOI MOSFETs:

In this case the thickness of the silicon film in the channel region is thin enough. Hence, the depletion region can now be formed in the whole film. FD SOI MOSFET helps in the reduction of several of the drawbacks of the conventional MOSFETs like threshold voltage roll off, higher sub-threshold slop body effect, etc. Here interaction between the electric field of source and drain is reduced due to the presence of buried oxide layer. Among major disadvantages of the FD SOI MOSFET is the presence of floating body effect as the silicon film is not provided with any of the electrical supplies. The SOI MOSFET is a quickly replacing the massive silicon based technology.

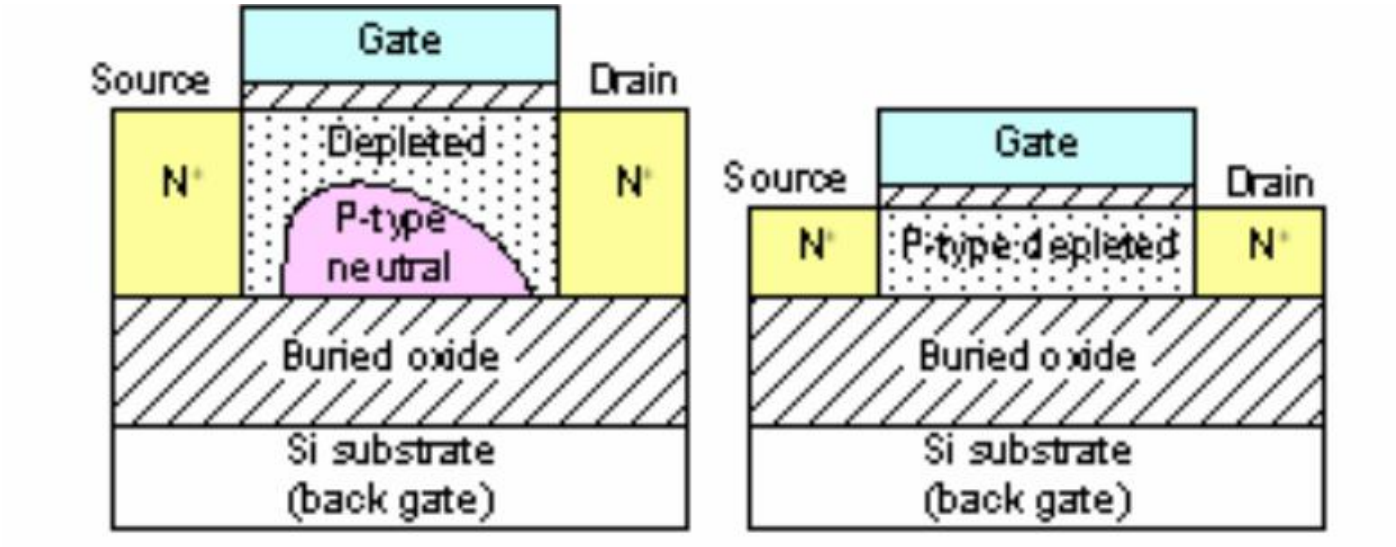


Fig1.1 showing a typical view of partially depleted and side by side fully depleted SOI MOSFET.

Advantages of SOI MOSFET

- The device technology is simple technology having no trenches or wells.
- The device performance is also better especially the dielectric isolation in both directions
- It has no latch up.
- It has tolerance to radiation.
- It allows lower operation at lower voltage.
- It has lesser sub-threshold swing.
- Latch up free CMOS Technology
- Reduced parasitic capacitances
- It eliminates the need of parasitic thyristor.
- Lesser of drain /source junction
- High temperature operation is possible.
- 3D integration
- Short channel effects drastically reduces.
- Saturation current is high than MOS/Si Transistor
- Lesser carriers effects
- Lesser substrate polarization effect.
- Minor Passive current.

Chapter II

Gaussian distribution

It is a mathematical function of the form as described below:

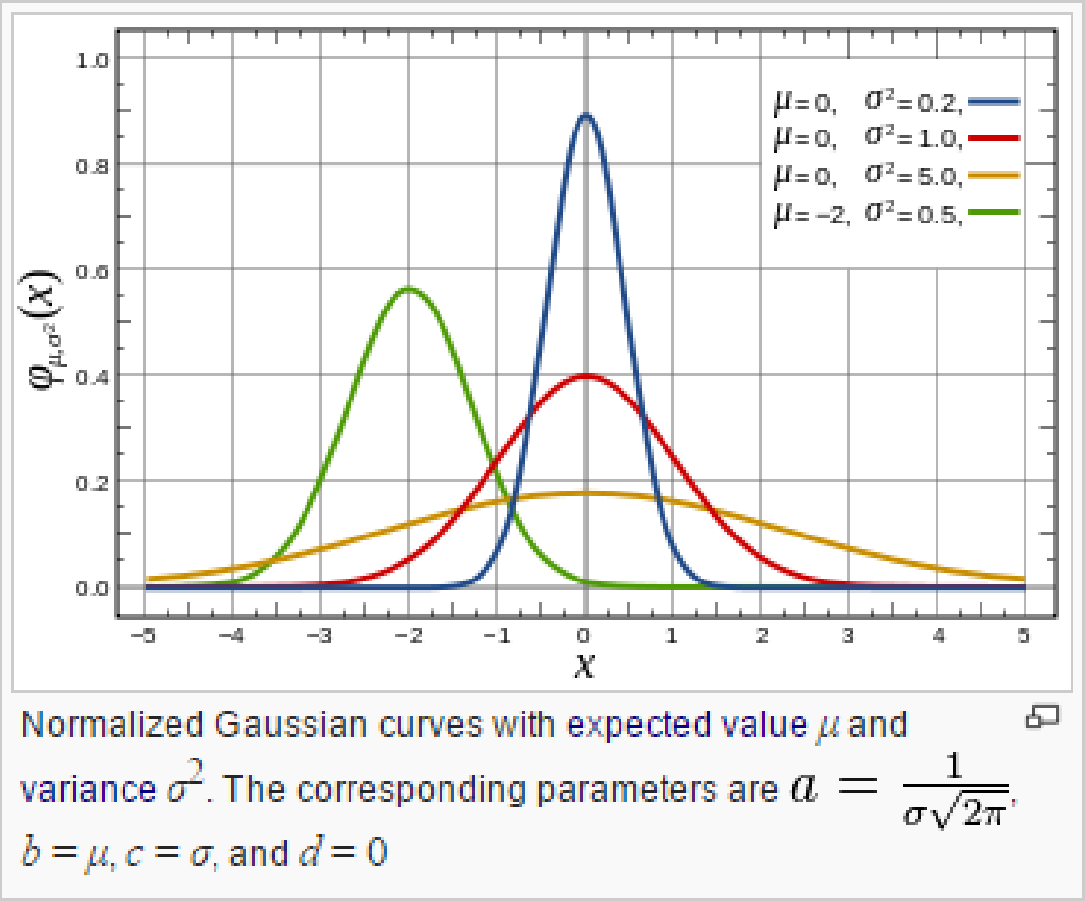
$$f(x) = a \exp\left(-\frac{(x-b)^2}{2c^2}\right)$$

Where a, b and c are arbitrary real constants.

This function is also referred to as the normal probability density function or simply the normal PDF. It is the vertically normalized PDF that is obtained from a signal or measurement that has purely random errors. The Gaussian distribution is a continuous function and is the approximate version of the binomial distribution of a large number of events.

It is a symmetric bell shaped curve with the parameter a, b and c which deals with the height of the curve, the position of the center of the peak and the width of the curve respectively. The logarithm of the Gaussian functions are concave quadratic function. The function is modeled by using a concave quadratic function in the exponential function.

This function finds its use in the statistics for representing the normal distributions, in the signal processing for representing Gaussian filters, in image processing for Gaussian blurs, and in mathematics to solve diffusion equations and heat equations and to define the Weierstrass transform.



Normalized Gaussian curves with expected value μ and variance σ^2. The corresponding parameters are $a = \frac{1}{\sigma\sqrt{2\pi}}$, $b = \mu$, $c = \sigma$, and $d = 0$

Fig 1.2 Gaussian curves (normalized) for different values of lateral straggle.

Chapter III

Motivation for Present Research

FD SOI MOSFET have much better immunity towards short-channel effects, drive current, subthreshold slope, transconductance, volume inversion than bulk SOI MOSFET and hence is considered to be the next generation device technology. There have been several papers on compact modeling of SOI MOSFET. If we take the case of Young's [1] model where he modeled the potential in the channel region using the 2^{nd} order polynomial function. Further Yan related the potential distribution of the Young [1] with threshold voltage. From his model the concept of characteristic length emerged which further helped in comparing the short channel effect among various devices on the basis of the value of their characteristic length. But there was a shortcoming in the Young's model as he didn't incorporated the modeling of the buried oxide in his model. But due to the shrinking of the device dimension is shrinking the 2D effects in the BOX region can't be ignored which was pointed out by Joachim et al. He incorporated an empirical model to include the effect of buried oxide electric field.

Suzuki et al. incorporated 2D model in both channel and the buried oxide region to develop the surface potential model. However, now a days there is a huge increase in the stand-by power consumption of the SOI devices due to increasing tendency towards lowering of threshold voltage. We can control the short channel effects by controlling the thickness of the silicon film and the off-current.

But below 65 nm m node, it is quite difficult to fabricate defect free devices. Also, parasitic resistances degrades the drain current. To control the parasitic resistance the doping in the source/drain is kept very high. However below 65 nm node, the formation of ultrashallow junction is observed which further enhances the short channel effects.

Advanced annealing techniques can be used to improve the ultrashallow junction formation. Hence, we can't further neglect the lateral source/drain doping effect on the channel region while deriving the analytical modeling of SOI devices. The effect of S/D doping is modeled in terms of effective S/D ends, ionized dopant species and effective channel length calculation considering dopant degeneracy effects.

Chapter IV

Topic of Research in the present work.

In the current work, using the 2D mathematical approach including the effect of lateral S/D Gaussian doping profile in SOI MOSFET is examined. The above mentioned approach is implemented by a physics based 2D numerical modelling the front surface potential in the channel region.

Modelling of surface potential in FD SOI MOSFET including lateral S/D Gaussian Doping profile.

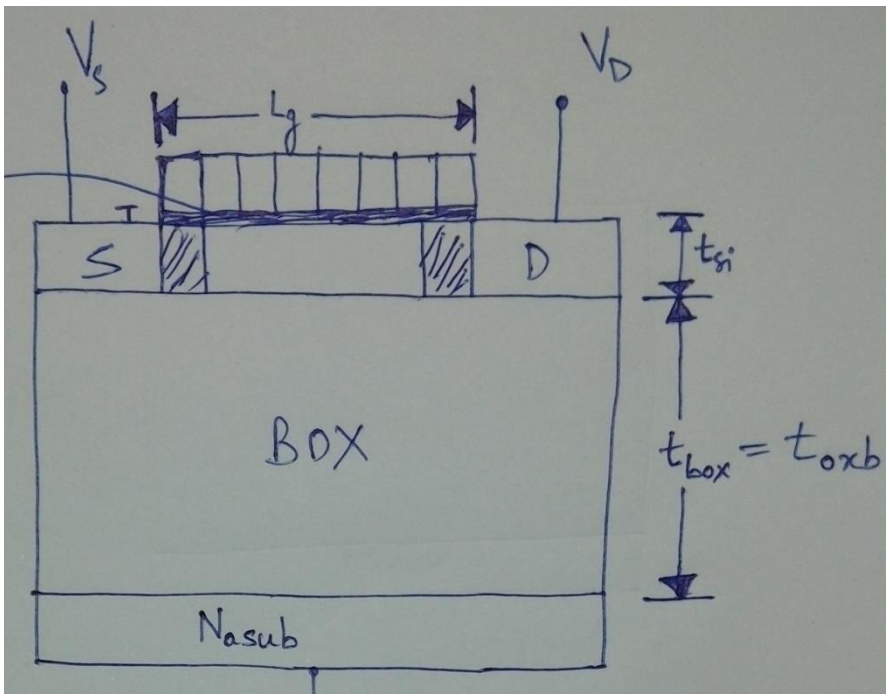


Fig1.3 FD SOI MOSFET studied in the present work with finite value of lateral straggle. Here t_{Si} is the channel thickness and t_{box} is the thickness of buried oxide, N_{Sub} , N_a , N_d are substrate, channel, source/drain doping

respectively.

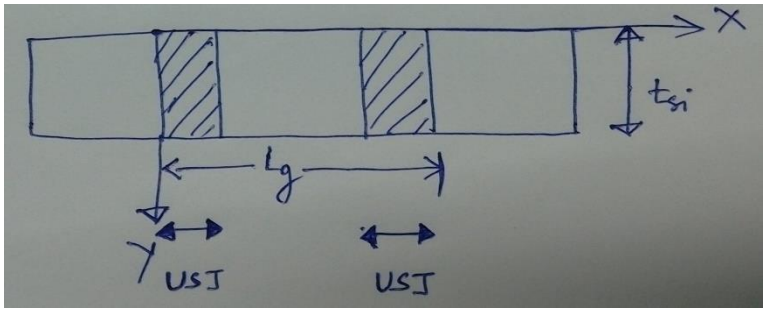


Fig 1.4The channel region of MOSFET showing the formation of Ultra Shallow junction at the Source/Drain end.

Mathematical Model

Here we have used a physics based 2D model to develop the surface potential based model in the FD SOI MOSFET. Here we have solved the 2D Poisson's equation both in the channel region and BOX region.

The potential function in the silicon thin film and the buried oxide, before the onset of strong inversion can be expressed as

$$\frac{\partial^2 \Psi_1(x,y)}{\partial x^2} + \frac{\partial^2 \Psi_1(x,y)}{\partial y^2} = \frac{q^* N_A}{\epsilon_{si}} - \frac{q^* N_{SD}^+(\mathrm{x})}{\epsilon_{si}}$$

$$\frac{\partial^2 \Psi_2(x,y)}{\partial x^2} + \frac{\partial^2 \Psi_2(x,y)}{\partial y^2} = 0$$

Where N_a is the channel doping, tis the film thickness, ε_{Si} is the dielectric constant of silicon and L is the channel length.

The potential distribution considered here is in the vertical direction. Value of ϕ also varies in the vertical direction as proposed by Young [1] for FD

SOI MOSFET's is

$\Psi_1(x,y) = \Psi_s + a_{11}(x)y + a_{12}(x)y^2$ $\quad 0 < y < t_{si}$

$\Psi_2(x,y) = b_{20}(x) + a_{21}(x)y + b_{22}(x)y^2.$ $\quad t_{si} < y < t_{si} + t_0$

where $\psi_1(x.y)$ and $\psi_2(x.y)$ are the surface potential distribution in the channel and BOX layer respectively. ψ_s , a_{11} , a_{12} , b_{20} , a_{21} , b_{22} are the independent arbitrary constants.

We have solved the Poisson's equation separately in the channel region and the buried oxide region using the boundary conditions described below

1. Using the continuity of Electric flux at the gate-oxide interface, we can write

$$\frac{d\Psi(x,y)}{dx} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\Psi_f(y) - V_g^1}{t_f}$$

where ε_{eox} and ε_{Si} are the dielectric constant of the oxide and silicon layer respectively, t_f is the gate oxide thickness.

$$V_g^1 = V_g - V_{fb.f}$$

V_g denotes the gate-to-source bias voltage, $V_{fb,f}$ is the front-channel flat-band voltage.

2. Using the continuity of Electric flux at the interface of buried oxide and the back-channel , we can write

$$\frac{d\Psi(x,y)}{dx} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{V_s^1 - \Psi_b(y)}{t_b}$$

$$V_s^1 = V_s - V_{fb.b}$$

Where t_b is the buried oxide thickness, $\psi(x,y)$ is the back surface potential at the buried oxide-silicon interface, and V_s is the voltage applied at the substrate and $V_{fb,b}$ is the back-channel flat-band voltage.

3. Value of surface potential at the source side is

$\Psi(Seff)$=Vbi

4. Value of surface potential at the drain side is

$\Psi(Deff)$ =Vbi+Vds

Where $\text{Vbi}=\frac{kT}{q}\ln(\frac{N_A}{{n_i}^2})$ denotes the built-in potential.

Where N_a^- denotes the ionized acceptor concentration and N+SD(x) is the ionized donor concentration expressed as [17]

$$N_{SD}^{+} = \frac{N_{SD}(p)e^{\frac{-x^2}{2\sigma_L^2}} + N_{SD}(p)e^{\frac{-(L_g-x)^2}{2\sigma_L^2}}}{1+s_D e^{(\frac{E_F-E_D}{kt})})}$$

Peak value of Gaussian profile ($N_{SD(p)}$)	10^20
Degenerated doping value(N_{de})	2.7*10^19
Spin degenerated factor(S_D)	2
For Arsenic,E10	0.054 eV
Gate work function	4.6 eV
E10	0.054 eV
Gate Length	60e-7

Gate oxide thickness	5e-7 cm-3
Silicon film thickness	10e-7 cm-3

Table 1.1: Typical values used in device modelling.

The parameter sigma used in the expression of N^{+}_{SD} expresses the extent of contribution of the source/drain doping profile in the silicon thin film. When S/D doping becomes equal to N_{de} , the effective S/D is taken from that point and hence the effective channel length is from S_{eff} to $Deff$. Also, here we have taken the approximated value of the built in potential as $V_{bi} = V_T \frac{N_{de} N_a}{n^2_{i,eff}}$, where $V_T = \frac{kT}{q}$ represents the thermal voltage.

Arbitrary constants can be evaluated using the boundary conditions described above. Substituting the values of constants in eq1 and eq2 in the second order parabolic equation for the channel and buried oxide layer and further substituting them in the Poisson's equation for the channel and buried oxide layer, we can obtain the front and back surface potential distribution as

$$\frac{d^2\Psi_s}{dx^2} + \frac{V_G^1 - \Psi_s}{(lem)_f^2} = \frac{\delta t_{ox} t_{si}(t_{si} + 2\delta t_{ox}) q^* N_A^-}{2(lem)_b^2 (t_{si} + \delta t_{ox} + \delta t_0)\epsilon_{si}} + \frac{(\delta t_{ox})(V_G^1 - V_s^1)}{(lem)_f^2 (t_{si} + \delta t_{ox} + \delta t_0)}$$

$$\frac{d^2\Psi_b}{dx^2} + \frac{V_G^1 - \Psi_b}{(lem)_b^2} = \frac{\delta t_0 t_{si}(t_{si} + 2\delta t_{ox}) q^* N_A}{2(lem)_b^2 (t_{si} + \delta t_{ox} + \delta t_0)\epsilon_{si}} + \frac{(t_{si} + \delta t_{ox})(V_G^1 - V_s^1)}{(lem)_b^2 (t_{si} + \delta t_{ox} + \delta t_0)}$$

$$(lem)_f^2 = \frac{\delta\delta^2 t_{ox} t_{si}(t_{si}+2\delta t_0)[\delta^2 t_{si}(t_{si}+2\delta t_0)+(\delta t_0)^2]+(\delta t_0)^3[\delta^2 t_{si}(t_{si}+2\delta t_{ox})+\delta t_0((t_{si}+2\delta t_{ox}))}{2\delta^2(t_{si}+\delta t_{ox}+\delta t_0)[\delta^2 t_{si}(t_{si}+2\delta t_0)+(\delta t_0)^2]}$$

$$(lem)_b^2 = \frac{\delta t_0[\delta^2 t_{si}(t_{si}+2\delta t_{ox})+\delta t_0(t_{si}+\delta t_{ox})}{2\delta^2(t_{si}+\delta t_{ox}+\delta t_0)}$$

$\delta = \frac{\epsilon_{si}}{\epsilon_{ox}}$

Above non-homogenous differential equation of 2nd order having coefficients whose value is previously determined can be solved using the standard solution as

For the front surface potential as

$$\Psi_k = d_4 e^{-x^*(lem)_f} + d_5\, e^{x^*(lem)_b} - PI_k$$

Where

$$PI_k = V_G^1 - \frac{q^* L}{\epsilon_{si}}\left[(N_A^- - N_{SD}^+(x)\right) + M^*(V_G^1 - V_s^1)$$

For the back surface potential as

$$\Psi_o = d_4 e^{-x^*(lem)_f} + d_5\, e^{x^*(lem)_b} - PI_o$$

Where

$$PI_o = V_G^1 - \frac{q^* R}{\epsilon_{si}}\left[(N_A^- - N_{SD}^+(x)\right) + T^*(V_G^1 - V_s^1)$$

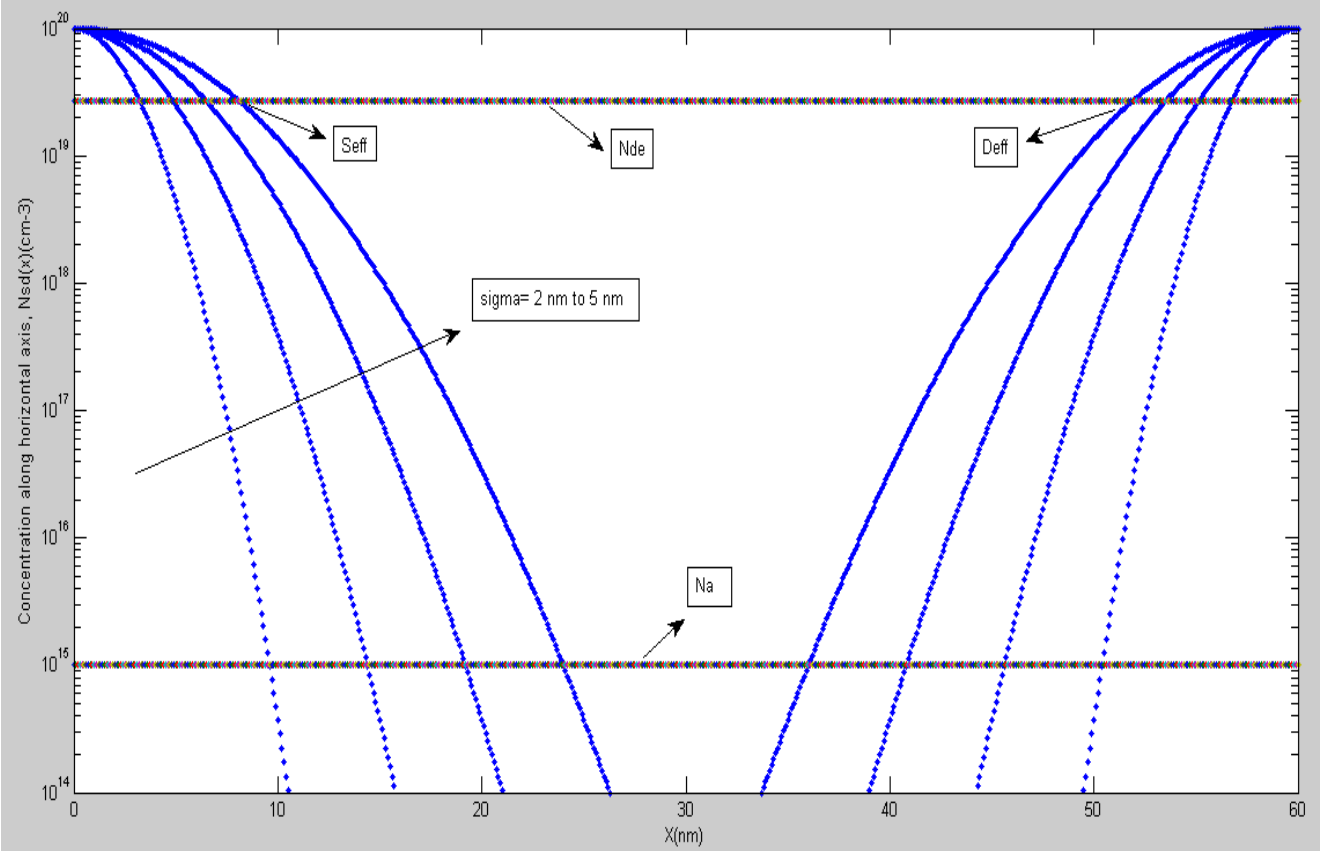


Fig 1.5 Variation of source/drain doping gradient for different lateral struggle values. The value of S_{eff} and D_{eff} is also shown when the N^{+}_{SD} is equal to N_{de} .

Lateral straggle(Sigma)	Seff	Deff
1(abrupt)	0	60
2	3.236	56.764
3	4.854	55.145
4	6.472	53.527
5	8.091	51.909

Table1.2 showing the variation in Value of Seff/Deff with lateral straggle. All values are in nm.

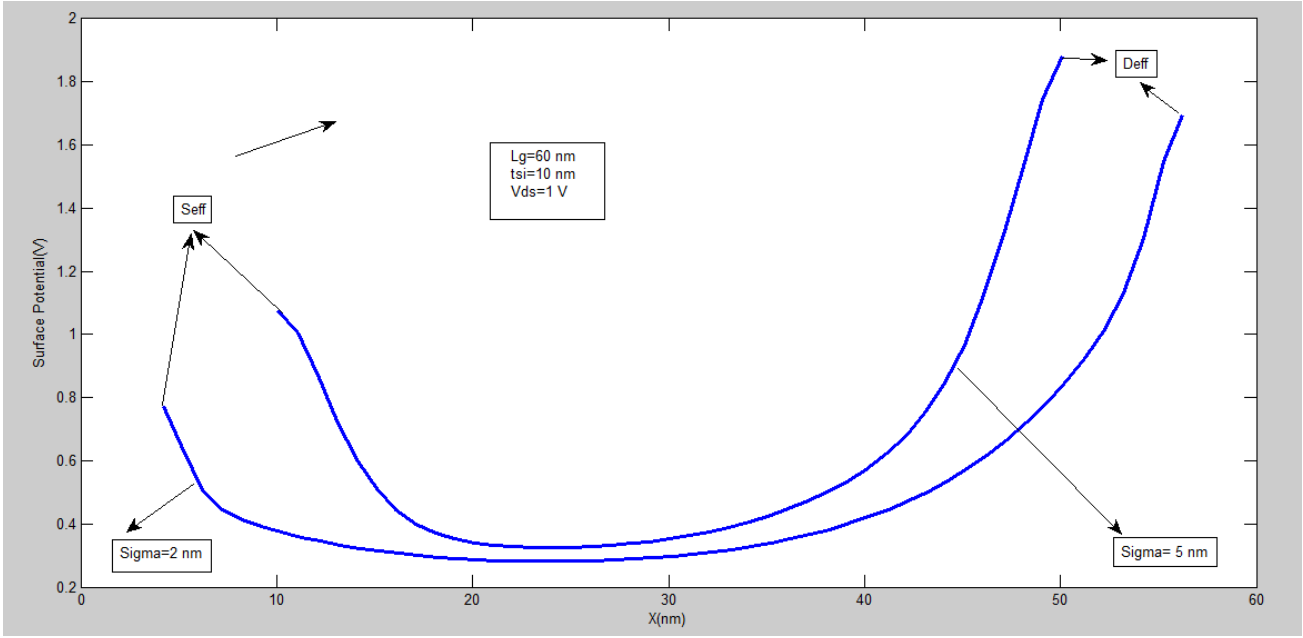


Fig 1.6 Front surface potential variation.(Vds=0.1 V)

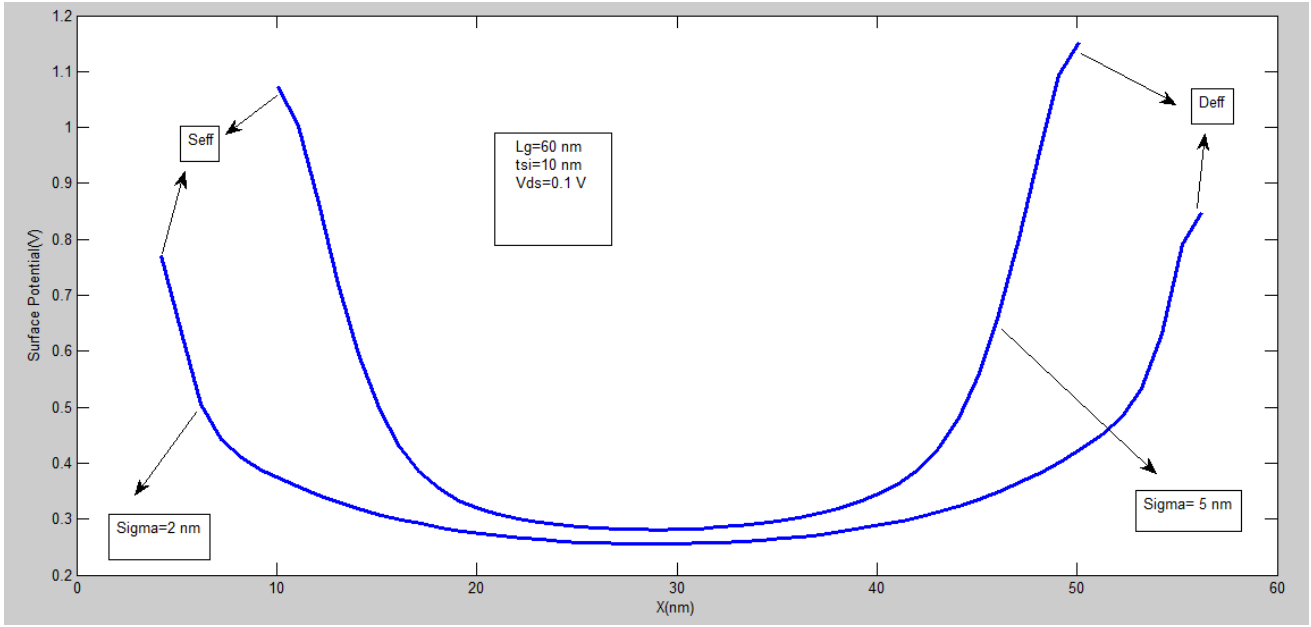


Fig 1.7 Front surface potential variation.(Vds=1 V)

Chapter V

Simulation of Device in ATLAS TCAD device simulator.

Brief introduction of simulation of device

Atlas belongs to the family of physics based 2D device simulator that is used to predict the electrical characteristics of semiconductor devices at different pre-specified bias point.

Physics based simulation performed in the ATLAS is based on different approach then empirical modeling. Usually, the purpose of the empirical modeling is to draw an analytic formulae which can fit into the existing data keeping in mind good accuracy and with minimum complexity. For that purpose such simulators extensively uses the approximation and interpolation techniques. The reason why we are focusing on the physically-based simulation is that it is much cheaper and faster than performing the actual experiments. This type of simulator can also calculate the parameters which otherwise is difficult to measure in actual experiments also. It also has few drawbacks like one has to use all the physics based equations into the simulator. Also, all the techniques used to solve the associated equations have to be incorporated in the simulator.

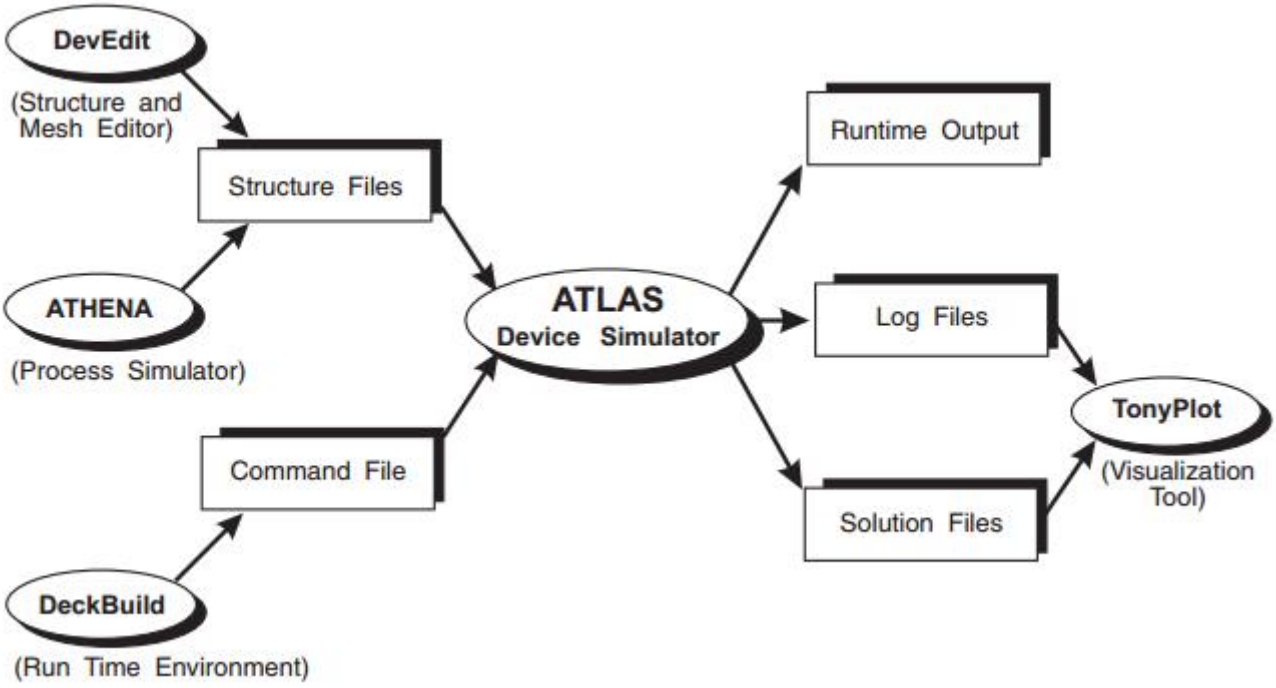


Fig1.8 ATLAS Inputs and Outputs

Simulation in ATLAS consists of the following steps

- Input file generation
- Running Atlas simulation
- Examine the output file

It is necessary to state the simulation problem in the beginning in the input file, stating the steps:

- The physical structure of the device used in simulation.
- The physical models required.
- The numerical methods to be used while solving the physical equations.
- The operating point for characterization of electrical parameters.

Atlas contains the following input files

- A structure file
- A text file

After simulation in Atlas, we can get output files of the following 3 types.

- As the simulation advances, the runtime output that shows error and warning messages.
- The log file that holds currents and voltages.
- The structure file containing the 2D and 3D data.

Always we have to compromise between what the accuracy needs and numerical efficiency. Accuracy needs a fine grid whereas numerical efficiency is much greater when lesser grid points are present in the simulation. Hence, during simulation to compensate the above problem we usually assign a fine grid only in the sensitive areas and a coarser grid at rest of the structure. Critical areas are usually located around metallurgical junctions in reverse biased state.

Distinctive critical areas

- Transverse electric field developed under the gate electrode.
- Areas where there is substantial recombination effects.
- Areas of high impact ionization

Structure files (extension,.str): It is used to get the structure of the device in image formate at a particular operating point. It can be used to see any calculated quantity within the structure of the device which may be electric fields, electron concentrations and band parameters etc.

- Structure files can be plotted using Tonyplot.
- Several quantities are saved by default within the structure file (doping, electron concentration, potential, electric field).
- Additional quantities can be specified by using the OUTPUT statement.

Log files (extension,.log).Calculation of the terminal characteristics is performed and stored by Atlas using log file .The characteristics are voltages and current at each electrode in DC analysis and in case of transient analysis time is calculated and stored. Value of conductance and capacitances is also stored in the AC analysis.

Tonyplot is used to plot log files.

Using LOG OUTF=<FILENAME>, a log file can be opened. Also, for every SOLVE statements defined in simulation program, LOG file saves the terminal characteristics from all of them. We can also use LOG OFF statement to tell the simulator not to save any of the terminal characteristics. It should be noted that the simulation program requires the use of separate log file for every bias sweep.

Physical models are broadly arranged into 5 classes in the ATLAS

- Recombination
- Mobility
- Impact ionization
- Tunneling
- Carrier statistics

MODEL statement is used in ATLAS to specify all the models except impact ionization. This model is defined using the IMPACT statement. With so many MODEL available in ATLAS, it is quite difficult to select the group of MODELs for a particular device simulation. However, there is an easy way to do it. We can select a basic set of mobility, carrier statistics, recombination and tunneling models for BIPOLAR and MOSFET devices using the BIPOLAR and MOS parameters of the MODELS statement.

MODELS BIPOLAR PRINT: It is used to enables the AUGER, FLDMOB, CONSRH, CONMOB and BGN models

MODELS MOS PRINT: It is used to enables the SRH, FERMI and CVT models

During the initial phase of the run-time output, we can use the print option in the MODELS statement to see the details the mobility models and material parameters.

Boundary Conditions

Several boundary conditions can be found in the ATLAS.

- Current boundary conditions
- Ohmic contacts
- Lumped elements between applied biases and device contacts.
- Schottky contacts

Numerical Methods

- Depending on the semiconductor device simulation requirement, we can select different numerical methods
- The numerical solution starts from an initial guess which refines the estimate of the solution in the successive phase. The nature of iteration is non-linear.
- The numerical iteration in the ATLAS proceeds as long as the criteria for the convergence is not satisfied or until the solution obtained is correct enough. The iteration will also proceed in case it is not clear that the solution will converge or not.
- We can try completely different initial guess or different grid, or different iteration, in the case the solution fails to converge.

3 types of techniques are usually applied in ATLAS

- Gummel.
- Newton.
- Block.

In the input file, METHOD statement is used to specify the numerical methods. In case of multiple methods s specified one after the other in the statement, then each method is executed one after the another till the convergence is achieved. The usual order in which the methods are applied is Gummel then Block then Newton. Newton is the default method which will be used by the simulation program in case no method is specified.

Obtaining Solutions

Finding solutions in ATLAS is the same as applying voltages and the currents at each electrode and then measuring the value of current at each electrode. In addition to the current, it also calculates the other quantities like carrier concentrations and electric fields in the device. These parameters are otherwise tedious to measure.

Solution statements

The simulation program can made an initial guess for carrier concentration and the potential, in case when there is no previous solution exists.
SOLVE INIT

We can obtain solutions by stepping the biases on electrodes from the initial equilibrium condition. Applied voltage value on the electrodes can be defined by the use of following statement:

SOLVE <NAME> =CATHODE VCATHODE=0 VFINAL=-100 VSTEP =-40

Atlas Statements

Input file consists of statements whose usual format is specified below. It should be noted that the statements are executed in the sequential order. Each statement has a keyword and identifier. The usual way of writing of the statement is:

<STATEMENT> <PARAMETER> = <VALUE>.

While defining statements in the input file, we should take care of the proper sequence of the statements. The order in which the group of statements occur must be preserved as specified below

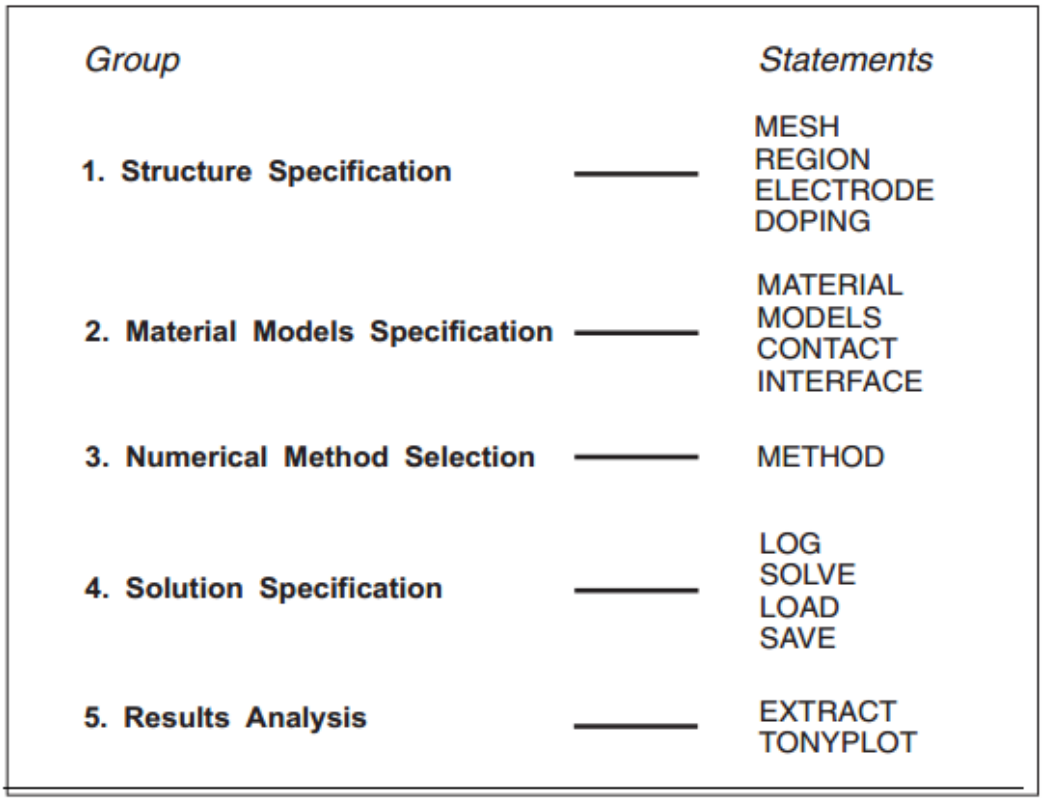


Fig1.9 Atlas Command Groups

Run-time output

At the bottom of the Deckbuild window, we can see several errors which can occur during the simulation. ATLAS interpret the simulation program on the line by line basis. Hence, it analyses each statement line by line during run time. During simulation some of the error prone statements can be ignored and we can get unexpected results. Hence, it is always suggested to observe the run-time output and interpret any error and warnings.

When ATLAS is dealing with the SOLVE statements, it displays the error number of every equation. It also displays the convergence issues, if there is any.

Run-time output

One can interpret the output as follows:

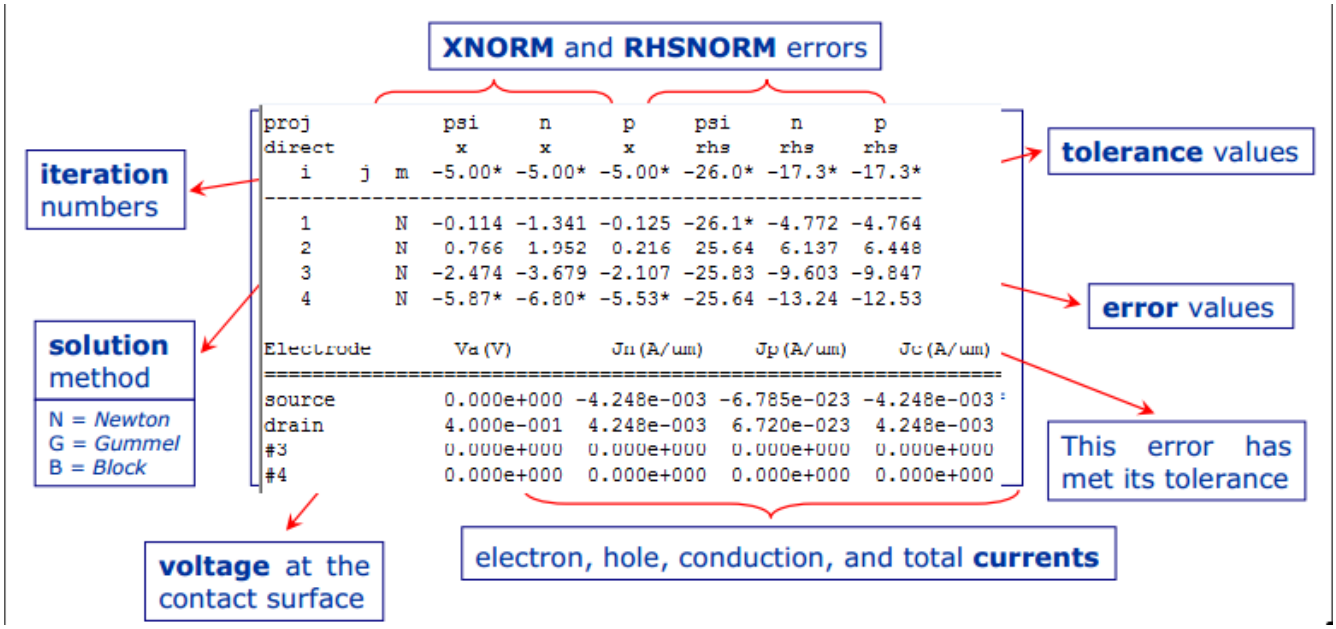


Fig1.10 showing output during run-time in ATLAS

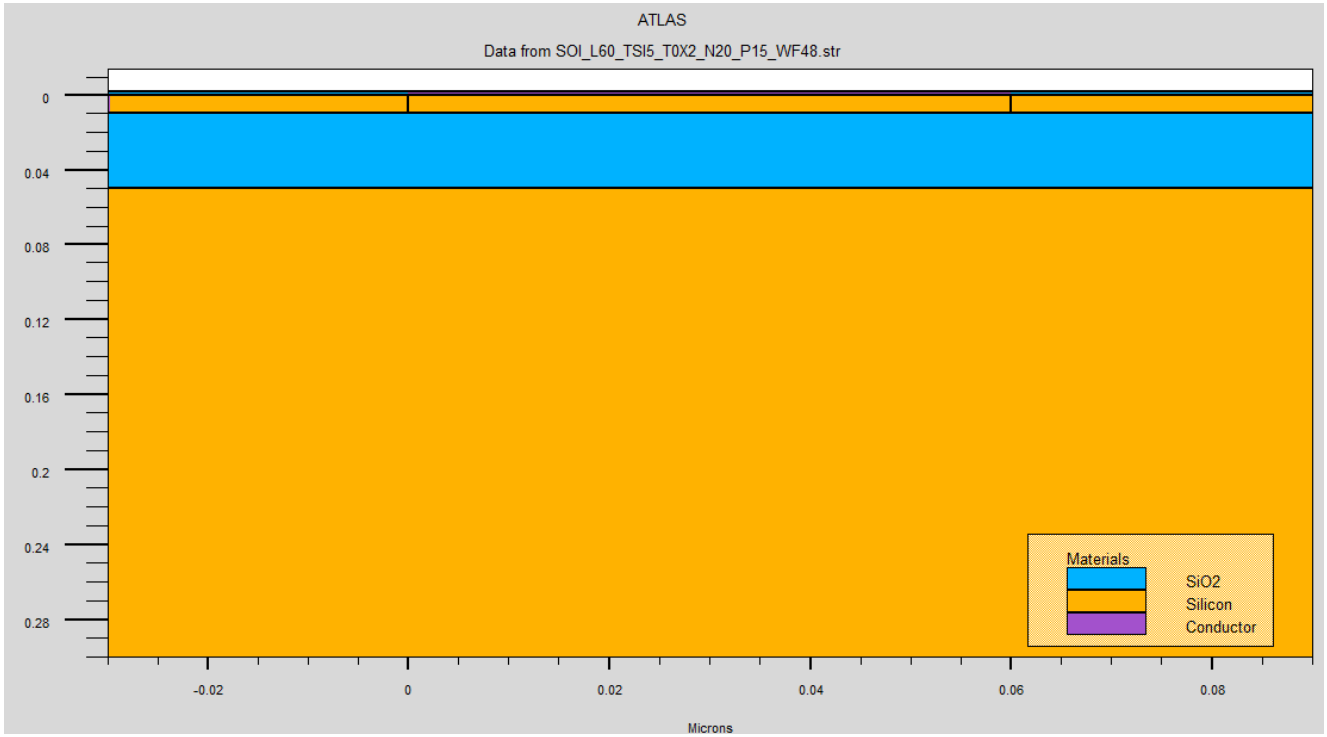


Fig1.11 Device structure of FD SOI MOSFET simulated in ATLAS TCAD.

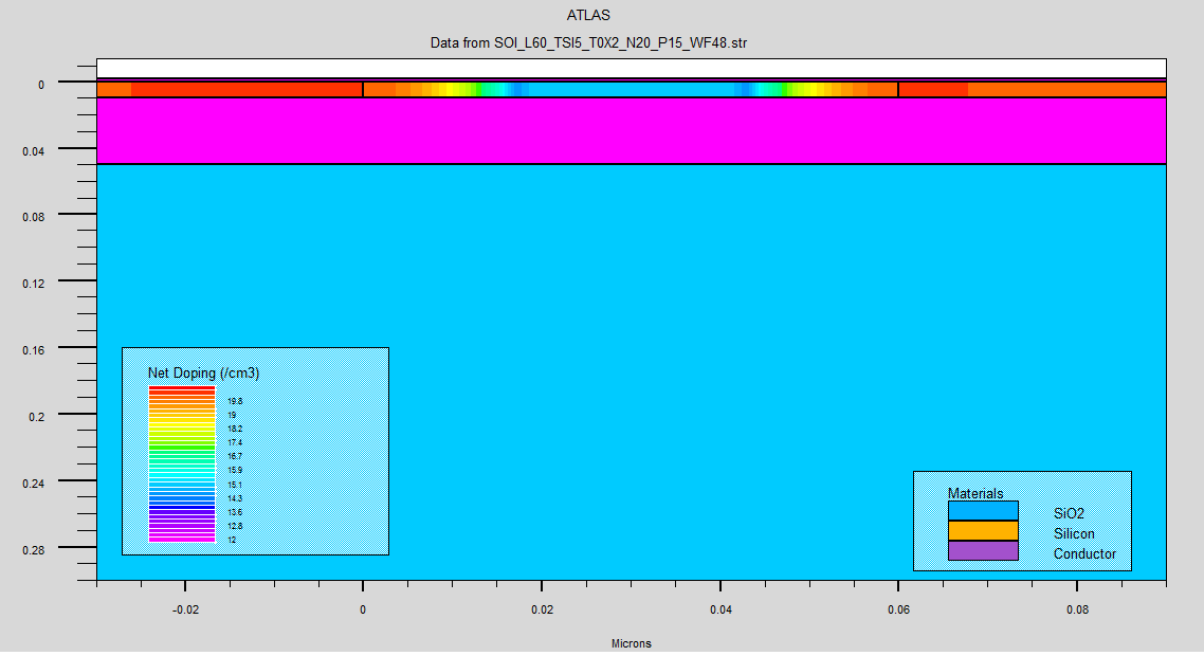


Fig.1.12 Device structure showing the concentration level in different region of FD SOI MOSFET.

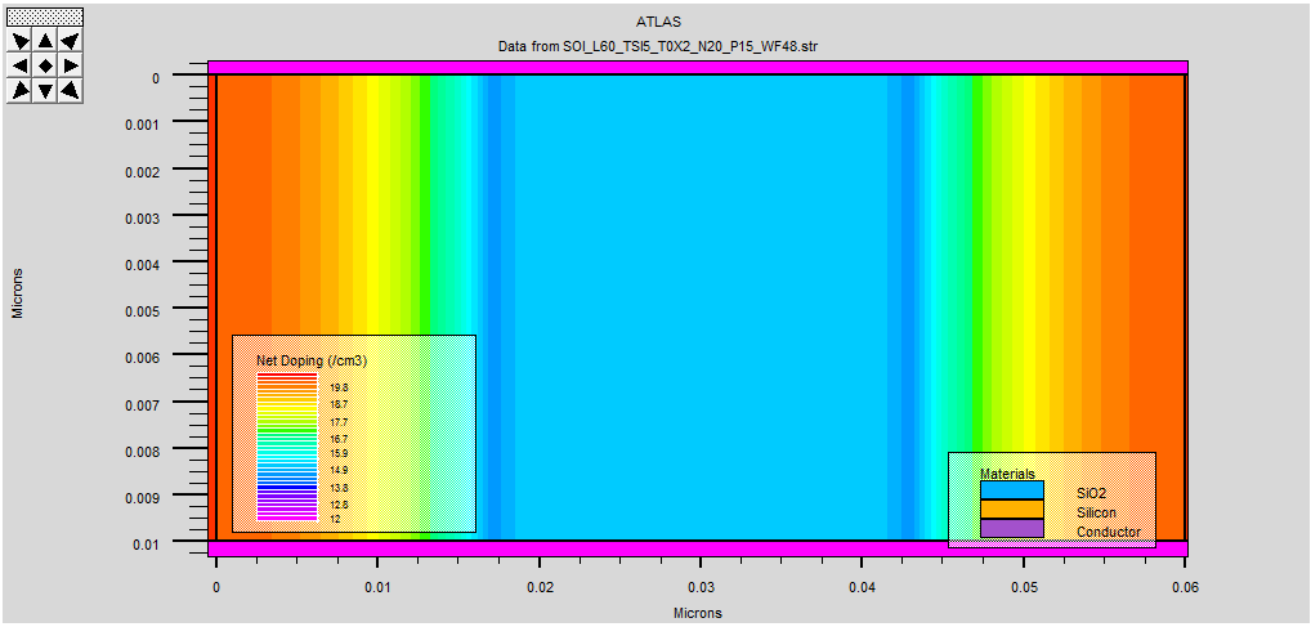


Fig.1.13 Device structure of FD SOI MOSFET showing the effect of S/D extension in the channel region.

Summary

In the present work we have shown that abrupt junction approximation can't be used below 65 nm technology as projected by ITRS. We have to include the effect of S/D extension in the channel region during the analytical modeling of nanoscale SOI MOSFETs taking into account S/D doping gradient.

We have developed the mathematical modeling for SOI MOSFET in the nanoscale region including the extension of S/D in the channel region. In the mathematical model developed, we have shown that the channel length defined by abrupt junction approximation has been replaced by effective channel length which is governed by the S/D doping profile and its lateral straggle. We have developed our model in MATLAB using the 2D Poisson's equation with suitable boundary conditions based on the electric field continuity at interface of gate oxide-Si and Si-SIo2 interface. In the developed model, lateral straggle will be the deciding factor for the device characteristics.

The developed model will be an important guideline for the future research work to further study the developed mathematical model with the suitable device simulator and further optimize the device parameter for below 65nm technological node. Further, we have simulated the device in the ATLAS TCAD device simulator and have shown the effect of S/D doping in the channel region.

Scope for Future Work

A mathematical model for FD SOI MOSFET has been developed in the nanoscale region using 2D Poisson's equation in the channel region and buried oxide region. In the future work, one can also study the developed model comparing with the suitable device simulator. The following points should be kept in mind during the future research.

- We can use spacer of suitable length at both the source and drain end to further control and shift the source/Drain concentration profile in the silicon channel. Spacers can be further effective in introducing asymmetry in the S/D doping profile. The asymmetry and variation in the spacer length and lateral straggle on the analog figure of merit can be studied.

- How the variation of spacer length and lateral straggle can be used to optimize the trade-off among various device parameters such as intrinsic voltage gain and cut-off frequency.

- Finding the optimum operating conditions for devices including the effect of S/D extension in the channel region.
- Comparing the performance of SOI MOSFETs with no spacer in between the S/D and the channel with one having spacer of equal length at both between Source-channel and the Drain-channel interface. We can also further extend this study taking into account spacer of different length at the source and the drain region.

References:

[1] K. K. Young, “Short-channel effect in fully depleted SOI MOSFETs,”IEEE Trans. Electron Devices, vol. 36, no. 2, pp. 399–402, Feb. 1989.
[2] Y. Wang, X.-W. He, and C. Shan, “A simulation study of SoI-like bulk silicon MOSFET with improved performance,” IEEE Trans. Electron Devices, vol. 61, no. 9, pp. 3339–3344, Sep. 2014.
[3] Ashutosh Nandi, Ashok K. Saxena, and Sudeb Dasgupta, Analytical Modeling of a Double Gate MOSFET Considering Source/Drain Lateral Gaussian Doping Profile, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 11, NOVEMBER 2013
[4] Engineering source/drain extension regions in nanoscale double gate (DG) SOI MOSFETs: Analytical model and design considerations, Abhinav Kranti *, G. Alastair Armstrong, Solid-State Electronics 50 (2006) 437–447
[5] K. Suzuki, “Short channel epi-MOSFET model,” IEEE Trans. Electron Devices, vol. 47, pp. 2372–2378, Dec. 2000.
[6] A Simulation Study of Hot Carrier Effects in SoI-Like Bulk Silicon nMOS Device, Ying Wang, Xiao-Wen He, and Chan Shan, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 62, NO. 1, JANUARY 2015
[7] Parameter sensitivity for optimal design of 65 nm node double gate SOI transistors, Tao Chuan Lim *, G. Alastair Armstrong, Solid-State Electronics 49 (2005) 1034–1043.
[8] R. H. Yan, A. Ourmazd, and K. F. Lee, “Scaling the Si MOSFET: From bulk to SOI to bulk,” IEEE Trans. Electron Devices, vol. 39, pp. 1704–1710, 1992.
[9] Current progress in modeling self-heating effects in FD SOI devices and nanowire transistors, D. Vasileska · K. Raleva · A. Hossain · S.M. Goodnick, J Comput Electron (2012) 11:238–248.
[10] ATLAS User’s Manual: Device Simulation Software, Silvaco Int., Santa Clara, CA, USA, 2008.
[11] K. Suzuki, Y. Tosaka, T. Tanaka, H. Horie, and Y. Arimoto, “Scaling theory for double-gate SOI MOSFETs,” IEEE Trans. Electron Devices, vol. 40, pp. 2326–2329, 1993.
[12] Semiconductor Device Realizing Characteristics like a SOI MOSFET, US Patient 6,930,361 B2.
[13] K. Suzuki and T. Sugii, “Analytical models for n -p double-gate SOI MOSFETs,” IEEE Trans. Electron Devices, vol. 42, pp. 1940–1948, 1995.

[14] E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology. New York, NY, USA: Wiley, 1982.

[15] S. R. Banna, P. C. H. Chan, P. K. Ko, C. T. Nguyen, and M. Chan, "Threshold voltage model for deep-submicrometer fully depleted SOI MOSFETs," IEEE Trans. Electron Devices, vol. 42, pp. 1949–1955, 1995.

[16] Pérez-Tomás et al., "Si/SiC bonded wafer: A route to carbon free SiO2 on SiC," Appl. Phys. Lett., vol. 94, no. 10, p. 103510, 2009.

[17] S. M. Sze, and K. K. Ng, Physics of Semiconductor Devices. New York, NY, USA: Wiley, 2007.

[18] Kranti, T. M. Chung, and J. P. Raskin, "Analysis of static and dynamic performance of short channel double gate silicon-on-insulator metal oxide semiconductor field effect transistors for improved cutoff frequency," Jpn. J. Appl. Phys., vol. 44, no. 4B, pp. 2340–2346, Apr.2005.

[19] K. Suzuki and T. Sugii, "Analytical models for n+-p+ double gate SOI MOSFET's," IEEE Trans. Electron Devices, vol. 42, no. 11, pp. 1940–1948, Nov. 1995.

[20] M. Yoshimoto, R. Araki, T. Kurumi, and H. Kinoshita, "Structure of directly bonded interfaces between Si and SiC," ECS Trans., vol. 50, no. 7, pp. 61–70, 2013.

[21] Analytical Modelling and simulation of short-channel effects in a FD DMG SOI MOSFET, Anurag Chaudhry, Master's dissertation, IIT Delhi.

[22] F. J. Morin and J. P. Maita, "Electrical properties of silicon containing Arsenic and boron," Phy. Rev., vol. 96, no. 1, pp. 28–35, Oct. 1954.

[23] J. W. Slotboom and H. C. Graff, "Measurements of bandgap narrowing in Si bipolar transistors," J. Solid State Electron., vol. 19, no. 10, pp. 857–862, Oct. 1976.