Modeling and Control of Low side Active Clamp Forward Converter with Synchronous Rectification

Thesis submitted in partial fulfillment of the requirements for the degree of

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in

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(Specialization: Control & Automation)

by

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Certificate

This is to certify that the work in the thesis entitled "Study and Comparison of various Digital Control Techniques for DC-DC Converters" by Maturi Krishnaja is a record of an original research work carried out by him under my supervision and guidance in partial fulfillment of the requirements for the award of the degree of Master of Technology with the specialization of Control & Automation in the department of Electrical Engineering, National Institute of Technology Rourkela. Neither this thesis nor any part of it has been submitted for any degree or academic award elsewhere.

Place: NIT Rourkela

Date: May, 2015

Prof. Susovon Samanta

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Abstract

Present work deals with the modeling and control of Low side Active Clamp Forward Converter (ACFC) with Synchronous rectification (SR) which is highly popular in telecommunication and point of use power supplies. The Forward converter is an isolated dc-dc buck converter and can provide wide range of output voltages based on the transformer turns ratio and duty cycle. The Forward converter is widely used as it provides galvanic isolation between input and output, simple, and gives high efficiency. The conventional forward converter i.e., tertiary reset topology has limitations like duty cycle should not be greater than 0.5 due to saturation and hard switching which causes voltage spikes during turn on and turn off of the MOSFET switch causing power loss. In order to overcome the saturation phenomena a clamp capacitor is connected in the primary to reset the transformer magnetizing inductance and ZVS phenomena takes place due to the resonance between the resonant inductance i.e., sum of the magnetizing and leakage inductance of the transformer and resonant capacitance i.e., sum of the parasitic capacitance of the switches and transformer resulting in soft switching. In the secondary side of the forward converter the diodes are replaced with synchronous rectifiers i.e., mostly N-MOSFET's which has low on state resistance in the order of milli-ohms resulting in low power loss. The steady state and transient analysis of the Low side Active Clamp Forward Converter topology with self-driven Synchronous Rectification has been analyzed in detail. The design of the topology was done and ZVS switching, reset of the transformer magnetizing inductance has been studied. The small signal modeling of the proposed converter topology under ideal conditions has been done and the control to output transfer function was derived using state space averaging model analysis. The PID controller is designed using frequency domain analysis. A single output voltage mode controlled Low side ACFC with SR is designed and implemented in PSPICE.

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List of abbreviations

CCM	Continuous Conduction Mode
DC	Direct Current
SR	Synchronous Rectification
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ZVS	Zero voltage Switching
EMI	Electromagnetic Interference
RCD	Resistor Capacitor Diode
ACFC	Active Clamp Forward Converter
KHz	Kilo Hertz
PM	Phase margin

List of Symbols

V_g	Input voltage
i_{Lr}	Current through the resonant inductor
i_{Lm}	Current through the magnetizing inductance of the transformer
n	Turns ratio of the transformer
L_m	Magnetizing inductance of the transformer
i_{S1}	Current through the main switch S1
i_{S2}	Current through the Auxiliary switch S2
i_{S3}	Current through the synchronous rectifier S3
i_{S4}	Current through the synchronous rectifier S4
I_0	Output current
D	Duty cycle
ΔI_L	Output inductor ripple
Δv_o	Output voltage ripple
F_S	Switching frequency
T_S	Time period
L	Output inductor
C	Output Capacitor
R	Load resistor

I_L	Output inductor current
V_o	Output voltage
C_{CL}	Clamp Capacitor
C_r	Resonant capacitance
i_C	Current through the clamp capacitor
v_p	Voltage across the primary of the transformer
v_s	Voltage across the secondary of the transformer
V_{CL}	Voltage across the clamp capacitor
V_{reset}	Reset voltage applied to the transformer
f_{gc}	Gain cross over frequency
$\varphi_{C,\max}$	Maximum phase of the lead compensator
S1	Main switch
S2	Auxiliary switch
S3,S4	Synchronous rectifiers
D1	Body diode of main switch
D2	Body diode of Auxiliary switch
D3,D4	Body diodes of synchronous rectifiers
$R_{DS,on}$	MOSFET on resistance

Chapter 1

Introduction

Chapter 1

1. Introduction

1.1 Background

Due to the vast growth in the telecommunications, computer systems there is a large demand of point of use power supplies from few decades. The distributed point of use power supplies requires high power density, high efficiency and constant operating frequency at lower power level .The requirements are satisfied by DC-DC converters hence various topologies have been developed and are used for these applications as they supply regulated DC output voltage from unregulated input DC voltage. There are two types of dc-dc converters called non-isolated and isolated converters. Isolated power converters provide galvanic isolation between the input and output where as non-isolated has no isolation and the load is not protected from high voltages. Isolated power converters provide less ripple DC compared to non-isolated as it has high EMI blocking capability. Thus many isolated topologies are developed based on the non-isolated DC-DC converters like Buck, Boost, Buck-Boost, SEPIC converters. The basic isolated topologies are Fly-back and Forward converters and many pulse width modulation topologies have been designed such as single switch, double switch, push-pull, half bridge, full bridge forward and flyback topologies which are listed in the sequence from low power level to high power level for unique power level application .

1.2 Motivation

As the standard flyback and forward topologies are operated with hard switching, that is, there are significant overlaps between the switch current and voltage during the tum-on and turn-off transients. These overlaps cause the switching losses. Thus, it is difficult to achieve high power density and high efficiency with standard topologies. In order to achieve high power densities, the power supplies are operated at increasingly higher frequencies. However, when the switching frequency increases, the losses associated with the tum-on and turn-off of the power switching devices in the hard switching MOSFET converters also increases. These losses are very significant and hence the operation of the converters above 50 Hz are prohibitive, as it leads to low conversion

efficiency and high cooling requirements. Over the years, the resistor-capacitor-diode snubber (RCD) has been employed to reduce the turn-off voltage stress and switching losses in the switches of converters. However, the power removed from the switching losses due to RCD dissipates completely in RCD itself. Thus, RCD has no contributions on efficiency nor reduce the size of the cooling devices. Also with the practical forward converter the duty cycle is less and maximum duty cycle possible is 50%.To overcome the problem of duty cycle and switching losses we are moving to the Active clamp reset technique with synchronous rectification which reduces the losses and improves the efficiency and duty cycle using the zero voltage switching phenomena via soft switching

1.3 Contribution to the thesis

- To design a Low side Active clamp forward converter with Synchronous rectification (Low side ACFC with SR) topology
- To study the steady and transient state analysis of the proposed topology
- Small signal modeling of Low side ACFC with SR
- To do the small signal modeling and derive the control to output transfer function using state space averaging technique.
- Implementation of voltage mode controlled single output Low side ACFC with SR.

1.4 Literature Review

In recent years due to the increase in the growth of telecommunications and switched mode power supplies there is an increase in demand for switching dc-dc power converters. There are different switching pulse width modulation topologies among which the forward converter and flyback converters are being widely used because of galvanic isolation, low cost, less complexity and simple in construction which provides variable power based on the transformers turns ratio and different duty cycle. It is widely used in commercial application as multiple isolated outputs are possible

The ideal forward converters has a single power MOSFET switch which transfers the power from input to output through the transformer during the on period and during the off period the stored energy of the output inductor serves the load. But conventional forward converters

saturates quickly as there is no alternative for discharge of stored energy of the transformer. So we move to tertiary reset forward converter topology in which the energy stored in the transformer is reset with the help of the tertiary or reset winding incorporated in the transformer. In this topology there is a limitation that the converter cannot be operated above a duty cycle of 0.5 otherwise the transformer gets saturated.

To overcome the problem of varied duty cycle range and saturation another new topology called RCD clamp was designed in which the resistance and capacitor are connected in parallel to the magnetizing inductance of the transformer. In this topology the stored energy is discharged in the resistor and capacitor connected during the off switch period. But it suffers from less efficiency as more power loss takes place. This topology can be operated for duty ratio above 0.5. This topology is discussed in [1-2]. Then comes the resonant reset technique in which there is no tertiary winding or RCD clamp but hard switching takes place and it is discussed in [3].All the conventional topologies from the tertiary forward converter are compared and discussed in [4]

As all the conventional topologies undergoes hard switching and hence to reduce the power loss and improve the efficiency a new topology was designed called Active clamp reset technique in which the clamp capacitor connected resets the magnetizing inductance of the transformer to the clamp voltage and also ZVS can be achieved during the resonance which reduces the switching losses of the converter. The active clamp reset topology is discussed in [5].

Basically there are two types of reset topologies possible with active clamp and they are low side active clamp and high side active clamp. The topologies differ in the connection of auxiliary switch and clamp capacitor in the primary side. The differences between the two topologies are discussed in [6].

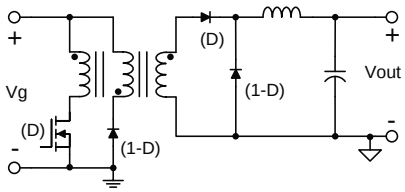
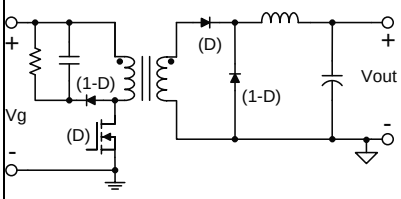
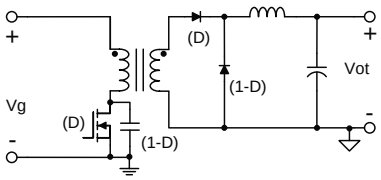
To improve the efficiency the diodes in the secondary of the forward converter are replaced with synchronous rectifiers which has lower switching and conduction loss. There are two types of synchronous rectification namely self driven and control driven synchronous rectification. The synchronous rectification is discussed in [7-10]. With synchronous rectification the efficiency will be improved as it has low $R_{DS,on}$ and fast switching takes place.

My research work includes the design, implementation and control of Low side Active Clamp Forward Converter with Synchronous Rectification. The analysis of Low side ACFC with SR in steady state is discussed in detail in [11] and design is explained in [12-15].The small signal modeling and the controller design is discussed in [16-19].

1.5 Comparison of different forward converter topologies

The differences between the three basic forward converter configurations are tabulated.

Table 1.1 Comparison of tertiary winding, RCD clamp and resonant reset topologies

Tertiary winding	RCD clamp	Resonant Reset
		
Advantages: 1.Low Complexity 2.Low Voltage Stress 3.Recycled Inductive Energy Disadvantages: 1.Hard-switching 2.50% Duty Cycle Limit 3.Lower Transformer Turns Ratio 4.Increased Transformer Leakage	Advantages: 1.>50% Duty Cycle 2.Simple Transformer Design Disadvantages: 1.Hard-switching 2.Higher Voltage Stress 3.Dissipative Inductive Energy 4.Clamp R Losses	Advantages: 1.Fewest components 2.Simple Transformer design 3.Recycled Inductive energy 4. .>50% Duty Cycle Disadvantages: 1.Hard-switching 2.Parasitic L and C Variation 3.Higher Voltage Stress 4.Self-Driven Synchronous Rectification not Intuitive

1.6 Organization of the thesis

Chapter 2 deals with the different modes of operation of Low side ACFC with SR. Along with the modes of operation the detailed steady state analysis has been presented. The design of the various components of the topology are presented in detail.

Chapter 3 deals with the detailed small signal modeling of the Low side ACFC with SR by state space analysis by neglecting the dead time between the on state and the off state. The state space analysis is done for the ideal topology and the transfer functions are derived.

Chapter 4 deals with the closed loop voltage mode control for Low side ACFC with SR. The various components of the closed loop control are presented and controller design is presented in detail.

Chapter 5 deals with the simulation and results of open loop and voltage mode controlled closed loop Low side ACFC with SR

Chapter 6 deals with conclusion and future scope of the project.

Chapter 2

Steady state analysis and Design of LACFC with SR

Chapter 2

2. Steady state analysis and Design of LACFC with SR

2.1 Introduction

Active clamp forward converter is a resonant reset forward topology in which a clamp capacitor in series with an active switch is connected in the primary of the converter to reset the transformer magnetizing inductance.

Advantages of Active clamp reset technique over RCD clamp:-

1. Soft switching is possible with reduced Electromagnetic interference.
2. Energy stored in the transformer is completely reset by the clamp capacitor.
3. Duty ratio above 0.5 are possible.
4. Efficiency is improved by ZVS phenomena.

Basically there are two types of Active clamp reset topologies for a forward converter. They are high side and low side configurations. In high side the auxiliary MOSFET switch in series with capacitor is connected across primary of the transformer where as in low side it is connected across the main switch. The thesis deals with the operation, design and analysis of low side active clamp configuration with self driven Synchronous rectification. With the help of Self-driven Synchronous rectification the secondary side MOSFETS are turned on and off by the voltage across the secondary of the transformer.

2.2 Operation and analysis of Low side Active Clamp configuration with synchronous rectification

The Low side ACFC with SR topology is as shown in the Fig 2.1. The current directions and voltage conventions shown in Fig 2.1 are treated as positive.

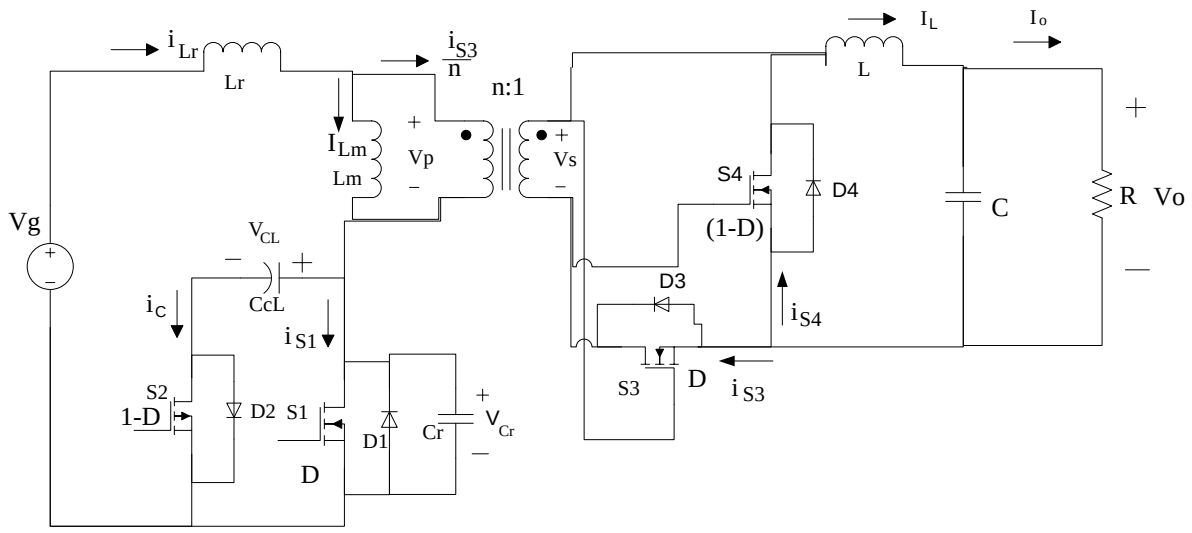


Figure 2.1 Schematic representation of Low side ACFC with SR

The operation of the converter over a switching period T_S is presented and the operation is divided into 12 modes for detailed steady state and transient state analysis of the converter and the operational waveforms are shown in Fig 2.2.

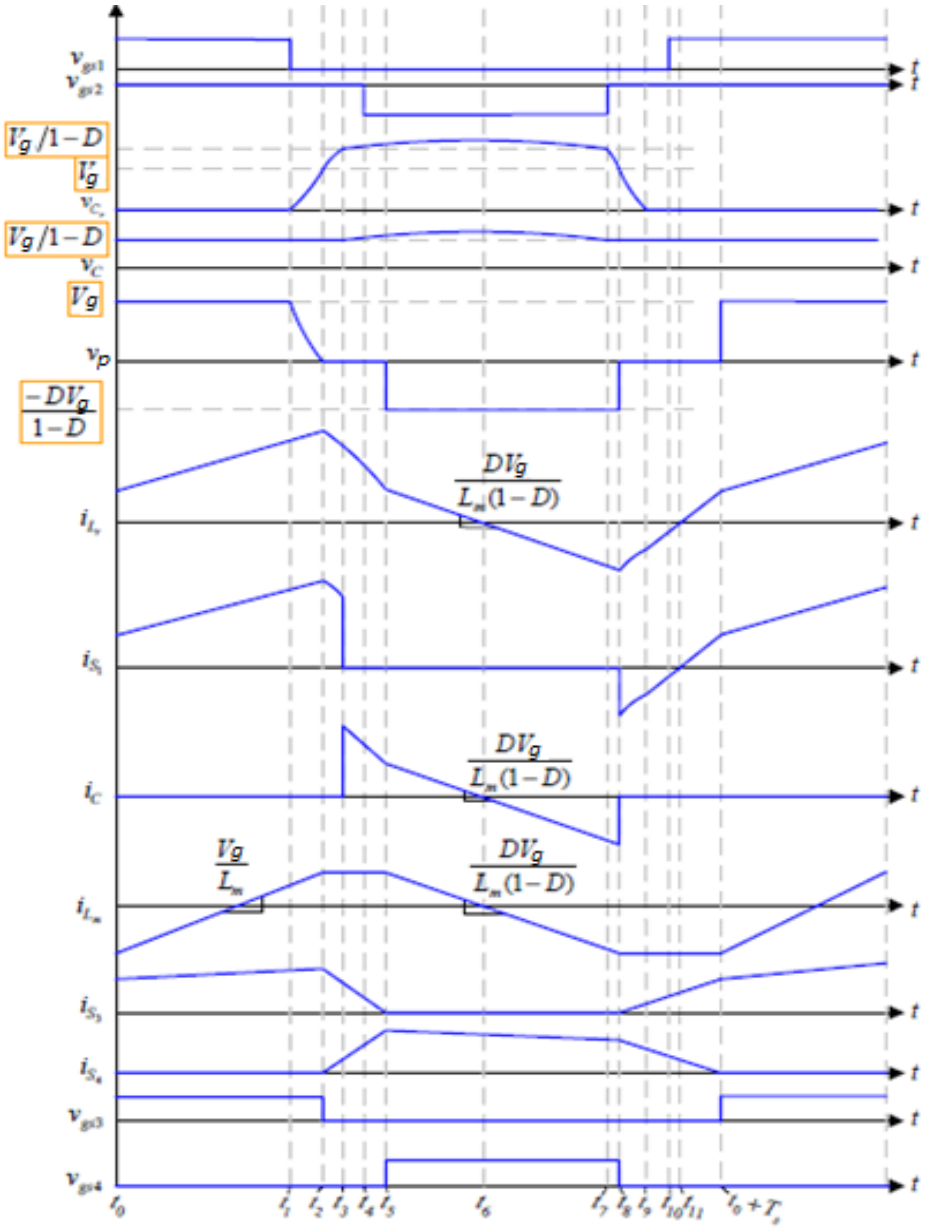


Figure 2.2 Operational waveforms of Low side ACFC with SR

The turning on and off of the switches during these 12 modes are presents in Table 2.1

Table 2.1 ON and OFF states of MOSFTES and body diodes during different modes of operation

Modes	S1	D1	S2	D2	S3	D3	S4	D4
$t_0 - t_1$	ON	OFF	OFF	OFF	OFF→ON	OFF	OFF	OFF
$t_1 - t_2$	ON→OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
$t_2 - t_3$	OFF	OFF	OFF	OFF	ON→OFF	OFF→ON	OFF	OFF→ON
$t_3 - t_4$	OFF	OFF	OFF	OFF→ON	OFF	ON	OFF	ON
$t_4 - t_5$	OFF	OFF	OFF→ON	ON→OFF	OFF	ON	OFF	ON
$t_5 - t_6$	OFF	OFF	ON	OFF	OFF	ON→OFF	OFF →ON	ON→OFF
$t_6 - t_7$	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
$t_7 - t_8$	OFF	OFF	ON→OFF	OFF	OFF	OFF	ON	OFF
$t_8 - t_9$	OFF	OFF	OFF	OFF	OFF	OFF→ON	ON→ OFF	OFF→ON
$t_9 - t_{10}$	OFF	OFF→ ON	OFF	OFF	OFF	ON	OFF	ON
$t_{10} - t_{11}$	OFF→ ON	ON→ OFF	OFF	OFF	OFF	ON	OFF	ON
$t_{11} - t_0 + T_s$	ON	OFF	OFF	OFF	OFF	ON	OFF	ON

2.2.1 Assumptions for the analysis of the Low side ACFC with SR

The steady state analysis of the converter is based on the following assumptions.

1. All the MOSFET switches are ideal
2. The output inductor L and output capacitor C are large enough to maintain the output current and voltage nearly constant.
3. The magnetizing inductance L_m of the transformer is greater than the resonant inductance L_r and also the clamp capacitor value C_{CL} is larger than the resonant capacitance C_r of the converter.
4. The energy stored in resonant inductor is greater than the energy stored in resonant capacitance for ZVS operation

2.3 Modes of operation and analysis of the low side ACFC with SR

The different modes of operation over a switching period T_s is completely analyzed and presented.

Mode 1($t_0 < t \le t_1$)

This mode starts when the main switch S1 turns on and the input voltage is applied across the primary of the transformer due to which the magnetizing current of the transformer starts increasing linearly. Also the power is transferred from input to the output through the transformer and conduction of rectifying switch S3 and energy is stored in output inductor during this period. This mode ends when main switch S1 is turned off at $t = t_1$.

The voltage across the resonant capacitor v_{Cr} during mode 1 is

$$v_{Cr}(\mathrm{t}) = 0 \tag{2.1}$$

The current through the resonant inductor i_{Lr} during mode 1 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{S1}(\mathrm{t}) = \mathrm{i}_{Lm}(\mathrm{t}) + \frac{I_0}{n} \approx \mathrm{i}_{Lm}(\mathrm{t}_0) + \frac{V_g}{L_m}(\mathrm{t}-\mathrm{t}_0) + \frac{I_0}{n} \tag{2.2}$$

Mode 2($t_1 < t \le t_2$)

During this mode the output current still flows through the switch S3 and in the input side there occurs a resonance between resonant capacitance, resonant inductance and magnetizing inductance. The resonant capacitance is charged by i_{Lr} and voltage v_{Cr} builds up to input voltage V_g during this period. The voltage across resonating capacitance v_{Cr} during mode 2 is

$$v_{Cr}(\mathrm{t}) = V_g[1-\cos\omega_{r1}(\mathrm{t}-\mathrm{t}_1)] + \mathrm{i}_{Lr}(\mathrm{t}_1)\,\mathrm{Z}_{r1}\sin\omega_{r1}(\mathrm{t}-\mathrm{t}_1) \tag{2.3}$$

The current through resonant inductor i_{Lr} during mode 2 is given by

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_1)\cos\omega_{r1}(\mathrm{t}-\mathrm{t}_1) + \frac{V_g}{\mathrm{Z}_{r1}}\sin\omega_{r1}(\mathrm{t}-\mathrm{t}_1) \tag{2.4}$$

where resonating frequency ω_{r1} during this period is

$$\omega_{r1} = \frac{1}{\sqrt{(\mathrm{L}_r+\mathrm{L}_m)\,\mathrm{C}_r}},\ \mathrm{Z}_{r1} = \sqrt{\frac{\mathrm{L}_r+\mathrm{L}_m}{\mathrm{C}_r}} \tag{2.5}$$

The time interval of mode 2 is

$$\Delta t_1^2 = \frac{1}{\omega_{r1}}\tan^{-1}\left(\frac{V_g}{\mathrm{i}_{Lr}(\mathrm{t}_1)\,\mathrm{Z}_{r1}}\right) \tag{2.6}$$

Mode 3($t_2 < t \le t_3$)

This mode starts when $v_{Cr} = V_g$ and the primary of the transformer becomes shorted due to which the secondary is also shorted hence the rectifying switch S3 and freewheeling switch S4 does not conduct so the body diodes D3 and D4 conducts the output current. In this mode the resonance occurs between L_r and C_r. Also during resonance as v_{Cr} is increased i_{Lr} is decreased. The relationship between transformer primary and secondary currents in this mode is given by

$$i_{S3} = n(i_{Lr} - i_{Lm}) \tag{2.7}$$

So as i_{Lr} is decreased during resonance i_{S3} also decreases and so i_{S4} increases linearly supply total output current and commutation of switch S3 takes place. The energy stored in the output inductor is transferred to the load.

The voltage across resonating capacitance v_{Cr} during mode 3 is

$$v_{Cr}(\mathrm{t}) = V_g + \mathrm{i}_{Lr}(\mathrm{t}_2)\,\mathrm{Z}_{r2}\sin\omega_{r2}(\mathrm{t}-\mathrm{t}_2) \tag{2.8}$$

The current through resonant inductance i_{Lr} during mode 3 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_2)\cos\omega_{r2}(\mathrm{t}-\mathrm{t}_2) \tag{2.9}$$

where resonating frequency ω_{r2} during this period is

$$\omega_{r2} = \frac{1}{\sqrt{\mathrm{L}_r\mathrm{C}_r}},\ \mathrm{Z}_{r2} = \sqrt{\frac{\mathrm{L}_r}{\mathrm{C}_r}} \tag{2.10}$$

The time interval of mode 3 is

$$\Delta t_2^3 = \frac{1}{\omega_{r2}}\sin^{-1}\left(\frac{DV_g}{1-D}\frac{1}{\mathrm{i}_{Lr}(\mathrm{t}_2)\,\mathrm{Z}_{r2}}\right) \tag{2.11}$$

The mode 3 ends when $v_{Cr} = \dfrac{V_g}{1-D}$ at $t = t_3$

Mode 4($t_3 < t \le t_4$)

This mode starts as the resonant capacitor is charged to the voltage across the clamp capacitor and hence the body diode D2 of switch S2 is shorted. During this mode i_{Lr} starts charging clamp capacitor and resonance occurs between L_r and C_{CL}.

The voltage across clamp capacitor v_{CL} during mode 4 is

$$v_{CL}(\mathrm{t}) = V_g - [V_g - v_{CL}(\mathrm{t}_3)]\cos\omega_{r3}(\mathrm{t}-\mathrm{t}_3)] + \mathrm{i}_{Lr}(\mathrm{t}_3)\,\mathrm{Z}_{r3}\sin\omega_{r3}(\mathrm{t}-\mathrm{t}_3) \tag{2.12}$$

The current through resonant inductance i_{Lr} during mode 4 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_3)\cos\omega_{r3}(\mathrm{t}-\mathrm{t}_3) - \frac{V_g - v_{CL}(\mathrm{t}_3)}{\mathrm{Z}_{r3}}\sin\omega_{r3}(\mathrm{t}-\mathrm{t}_3) \tag{2.13}$$

where resonating frequency ω_{r3} during this mode is

$$\omega_{r3} = \frac{1}{\sqrt{\mathrm{L}_r\mathrm{C}_{CL}}}, \mathrm{Z}_{r3} = \sqrt{\frac{\mathrm{L}_r}{\mathrm{C}_{CL}}} \tag{2.14}$$

Mode 5($t_4 < t \le t_5$)

This mode starts when auxiliary switch S2 is turned on and resonance occurs between L_r and C_{CL} .In this mode the current through D3 is decreased and current through D4 is increased to output current. This mode ends when the resonating current is equal to the magnetizing current of the transformer.

The voltage across clamp capacitor v_{CL} during mode 5 is

$$v_{CL}(\mathrm{t}) = V_g - [V_g - v_{CL}(\mathrm{t}_4)]\cos\omega_{r3}(\mathrm{t}-\mathrm{t}_4)] + \mathrm{i}_{Lr}(\mathrm{t}_4)\,\mathrm{Z}_{r3}\sin\omega_{r3}(\mathrm{t}-\mathrm{t}_3) \tag{2.15}$$

The current through resonant inductance i_{Lr} during mode 5 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_4)\cos\omega_{r3}(\mathrm{t}-\mathrm{t}_4) - \frac{V_g - v_{CL}(\mathrm{t}_4)}{\mathrm{Z}_{r3}}\sin\omega_{r3}(\mathrm{t}-\mathrm{t}_3) \tag{2.16}$$

Mode 6($t_5 < t \le t_6$)

In this mode the output body diodes stop conducting and switch S4 is turned on due to reflected negative secondary voltage from the primary side.

The primary and secondary voltages are respectively

$$v_p = -\frac{DV_g}{1-D}, v_s = \frac{v_p}{n} \tag{2.17}$$

During this mode the resonance occurs between L_r , L_m and C_{CL} .

The voltage across clamp capacitor v_{CL} during mode 6 is

$$v_{CL}(\mathrm{t}) = V_g - [V_g - v_{CL}(\mathrm{t}_5)]\cos\omega_{r4}(\mathrm{t}-\mathrm{t}_5)] + \mathrm{i}_{Lr}(\mathrm{t}_5)\,\mathrm{Z}_{r4}\sin\omega_{r4}(\mathrm{t}-\mathrm{t}_5) \tag{2.18}$$

The current through resonant inductance i_{Lr} during mode 6 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_5)\cos\omega_{r4}(\mathrm{t}-\mathrm{t}_5) + \frac{[V_g - v_{CL}(\mathrm{t}_5)]}{\mathrm{Z}_{r4}}\sin\omega_{r4}(\mathrm{t}-\mathrm{t}_5) \tag{2.19}$$

where resonating frequency ω_{r4} during this period is

$$\omega_{r4} = \frac{1}{\sqrt{(\mathrm{L}_r + \mathrm{L}_m)\,\mathrm{C}_{CL}}}, \mathrm{Z}_{r4} = \sqrt{\frac{\mathrm{L}_r + \mathrm{L}_m}{\mathrm{C}_{CL}}} \tag{2.20}$$

The time interval of mode 6 is

$$\Delta t_5^6 = \frac{1}{\omega_{r4}}\tan^{-1}\left(\frac{1-D}{D}\frac{\mathrm{Z}_{r4}\mathrm{i}_{Lr}(\mathrm{t}_5)}{V_g}\right) \tag{2.21}$$

Mode 7($t_6 < t \le t_7$)

This mode starts when the resonant inductor becomes zero and then goes negative.

The voltage across clamp capacitor v_{CL} during mode 7 is

$$v_{CL}(\mathrm{t}) = V_g - [V_g - v_{CL}(\mathrm{t}_6)]\cos\omega_{r4}(\mathrm{t}-\mathrm{t}_6)] + \mathrm{i}_{Lr}(\mathrm{t}_6)\,\mathrm{Z}_{r4}\sin\omega_{r4}(\mathrm{t}-\mathrm{t}_6) \tag{2.22}$$

The current through resonant inductance i_{Lr} during mode 7 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_6)\cos\omega_{r4}(\mathrm{t}-\mathrm{t}_6) + \frac{[V_g - v_{CL}(\mathrm{t}_6)]}{\mathrm{Z}_{r4}}\sin\omega_{r4}(\mathrm{t}-\mathrm{t}_6) \tag{2.23}$$

Mode 8($t_7 < t \le t_8$)

This mode starts when auxiliary switch S2 gets turned off. A negative voltage continues to be applied across the primary of the transformer thus making S4 on and S3 off. The resonance occurs among L_r , L_m and C_r .

The voltage across resonant capacitor v_{Cr} during mode 8 is

$$v_{Cr}(\mathrm{t}) = V_g + \frac{DV_g}{1-D}\cos\omega_{r1}(\mathrm{t}-\mathrm{t}_7)] + \mathrm{i}_{Lr}(\mathrm{t}_7)\,\mathrm{Z}_{r1}\sin\omega_{r1}(\mathrm{t}-\mathrm{t}_7) \tag{2.24}$$

The current through resonant inductance i_{Lr} during mode 8 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_7)\cos\omega_{r1}(\mathrm{t}-\mathrm{t}_7) + \frac{DV_g}{1-\mathrm{D}}\frac{1}{\mathrm{Z}_{r1}}\sin\omega_{r1}(\mathrm{t}-\mathrm{t}_7) \tag{2.25}$$

The time interval of mode 8 is

$$\Delta t_7^8 = \frac{1}{\omega_{r1}}\tan^{-1}\left(-\frac{DV_g}{(1-\mathrm{D})\,\mathrm{i}_{Lr}(\mathrm{t}_7)\,\mathrm{Z}_{r1}}\right) \tag{2.26}$$

Mode 9($t_8 < t \le t_9$)

This mode starts when the voltage across the resonant capacitor reaches input voltage, hence the transformer gets virtually shorted resulting in the conduction of body diodes D3 and D4 simultaneously. During this mode the resonance occurs between L_r and C_r .The current through S3 starts linearly increasing while the current through S4 linearly decreasing and this mode ends when the voltage across the resonant capacitor becomes zero.

The voltage across resonant capacitor v_{Cr} during mode 9 is

$$v_{Cr}(\mathrm{t}) = V_g + \mathrm{i}_{Lr}(\mathrm{t}_8)\,\mathrm{Z}_{r2}\sin\omega_{r2}(\mathrm{t}-\mathrm{t}_8) \tag{2.27}$$

The current through resonant inductance i_{Lr} during mode 9 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_8)\cos\omega_{r2}(\mathrm{t}-\mathrm{t}_8) \tag{2.28}$$

The time interval of mode 9 is

$$\Delta t_8^9 = \frac{1}{\omega_{r2}} \sin^{-1}(-\frac{V_g}{\mathrm{i}_{Lr}(\mathrm{t}_8)\,\mathrm{Z}_{r2}}) \tag{2.29}$$

Mode 10 ($t_9 < t \le t_{10}$)

In this mode body diode D1, D3 and D4 are conducting making transformer virtually shorted. As a result the input voltage is totally applied across the resonant inductor and hence the current through it increases linearly and this mode ends when S1 is turned on. The current through resonant inductance i_{Lr} during mode 10 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_9) + \frac{V_g}{L_r}(\mathrm{t} - \mathrm{t}_9) \tag{2.30}$$

The time interval of mode 10 is

$$\Delta t_9^{10} = t_{10} - t_9 = \frac{L_r}{V_g}[i_{Lr}(\mathrm{t}_{10}) - \mathrm{i}_{Lr}(\mathrm{t}_9)] \tag{2.31}$$

Mode 11($t_{10} < t \le t_{11}$)

During this mode S1 starts conducting and D3, D4 still conducts and transformer is still virtually shorted and this mode ends when current through resonant inductor becomes zero.

The current through resonant inductance i_{Lr} during mode 11 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_{10}) + \frac{V_g}{L_r}(\mathrm{t} - \mathrm{t}_{10}) \tag{2.32}$$

The time interval of mode 11 is

$$\Delta t_{10}^{11} = -\frac{L_r}{V_g} i_{Lr}(\mathrm{t}_{10}) \tag{2.33}$$

Mode 12($t_{11} < t \le t_o + T_s$)

In this mode the current through the resonant inductor increases as the current through the body diode D3 is increased and is reflected to the primary of the transformer and this mode ends when current through D4 becomes zero and is the end of the one switching cycle.

The voltage across the resonant capacitor is $v_{Cr}(\mathrm{t}) = 0$ and current through resonant inductance i_{Lr} during mode 12 is

$$i_{Lr}(\mathrm{t}) = \mathrm{i}_{Lr}(\mathrm{t}_{11}) + \frac{V_g}{L_r}(\mathrm{t} - \mathrm{t}_{11}) \tag{2.34}$$

The time interval of mode 12 is

$$\Delta t_{11}^{t_0+T_s} = \frac{L_r}{V_g}\left[\frac{I_{Lo}}{n} - \mathrm{i}_{Lm}(\mathrm{t}_0 + \mathrm{T}_s) - i_{Lr}(\mathrm{t}_{11})\right] \tag{2.35}$$

2.4 Active clamp Circuit

a) Clamp voltage

Apply the volt second balance across the magnetizing inductance of the transformer by neglecting the winding resistances and leakage inductances we have

$$D * V_g = (1 - \mathrm{D}) * (\mathrm{V}_{CL} - \mathrm{V}_g) \tag{2.36}$$

The voltage across the clamp capacitor is given by

$$\mathrm{V}_{CL} = \frac{V_g}{1 - D} \tag{2.37}$$

b) Reset voltage

The reset voltage is defined as the voltage applied across the transformer primary when the main switch is off.

$$V_{reset} = V_{CL} - V_g = \frac{D}{1 - D} V_g \tag{2.38}$$

c) For single ended forward converter the transfer function is given by

$$V_o = \frac{D * V_g}{n} \tag{2.39}$$

Therefore duty cycle is given by

$$D = \left(\frac{V_o}{V_g} \right) n \tag{2.40}$$

2.5 Components design of Low side ACFC with SR

The components of the Low side ACFC with SR are designed as follows

a) Output inductor L

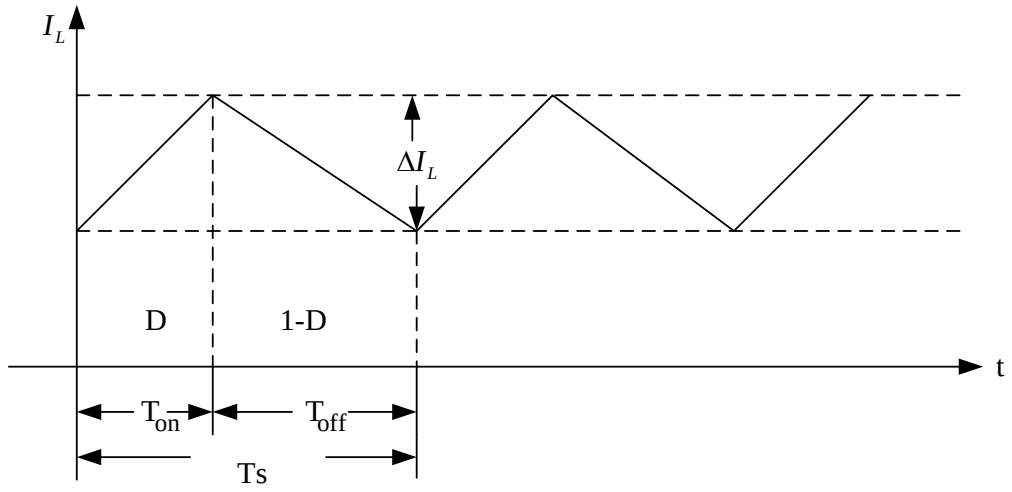


Figure 2.3 Waveform showing ripple in output inductor current

The value of the filter inductor L is large to maintain constant output load current and derived based on the tolerated peak to peak ripple current(ΔI_L) over a switching period and inductor current waveform is shown in Fig 2.15

Considering the negative slope of the output current we have

$$\Delta I_L = \frac{V_0}{L}(1-\mathrm{D}_{\min})\,\mathrm{T}_s$$
$$L = \frac{V_O}{\Delta I_L * F_S}(1-\mathrm{D}_{\min}) \tag{2.41}$$

The RMS current flowing through the inductor is

$$I_L = \sqrt{I_o{}^2 + \frac{\Delta I_L{}^2}{3}} \tag{2.42}$$

b) Output capacitor C

The filter capacitor is chosen large to maintain constant output voltage and is derived based on tolerance output ripple voltage over a switching period and waveform is shown in Fig 2.16

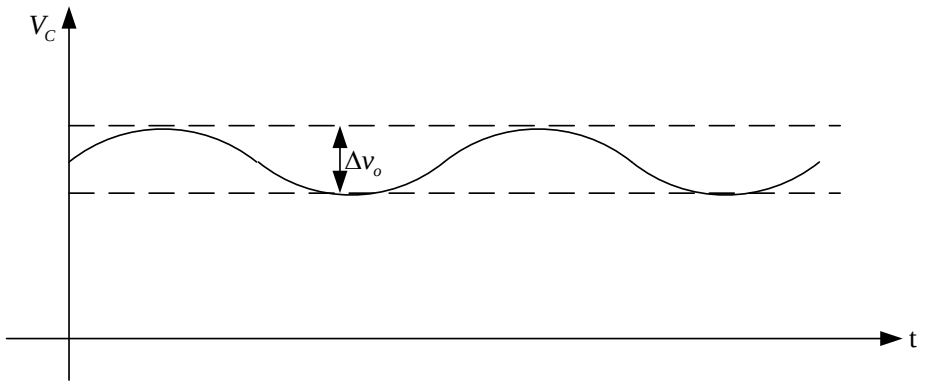


Figure 2.4 Waveform showing the voltage across the output capacitor

The filter output capacitor is given by

$$C = \frac{\Delta I_L}{8 * F_S * \Delta v_o} \tag{2.43}$$

c) Turns ratio of the transformer n

As we know the transformer turns ratio is the ratio of the voltage across the primary to the voltage across the secondary of the transformer respectively.

The voltage across the secondary is derived by applying the voltage second balance across the output inductor by neglecting the voltage drop across the switches and is given by

$$(V_s - V_o)D = V_o(1-\mathrm{D})$$
$$V_{s,\min} = \frac{V_0}{D_{\max}} \tag{2.44}$$

As we can see the voltage across the secondary will be minimum when the duty cycle is maximum. From this the turns ratio can be calculated as the minimum primary voltage will be the minimum input voltage itself.

d) Clamp Capacitor C_{CL}

The clamp capacitor value is chosen such that the resonant time period is much greater i.e., more than ten times of the main switch off period so the clamp capacitor almost acts as a constant voltage source.

$$2\pi\sqrt{L_m * C_{CL}} > t_{OFF(\mathrm{MAX})}$$

Therefore,

$$C_{CL} > 100 * \left[\frac{(1-\mathrm{D}_{min})^2}{L_m * (2\pi F_S)^2} \right] \tag{2.45}$$

e) Self driven Synchronous rectifiers

The synchronous rectifiers i.e., MOSFET switches are basically designed based on the basis of switching frequency, the current and voltage stresses.

In self driven synchronous rectification the voltage across the secondary of the transformer is given as gate to source voltages of the switches S3 and S4 directly to drive them into conduction. Hence the switch S3 is selected such that it is driven by the input voltage divided by the transformer turns ratio as it conducts when the main switch S1 is ON and switch S4 is selected such that it is driven by the reset voltage divided by the transformer turns ratio. The switches should withstand the maximum currents.

The maximum current flowing through switches S3 and S4 are

$$I_L = I_o + \frac{\Delta I_L}{2} \tag{2.46}$$

The gate to source voltage applied across the MOSFET switch S3 is

$$V_{S3} = \frac{V_g}{n} \tag{2.47}$$

The gate to source voltage applied across the MOSFET switch S4 is

$$V_{S4} = \frac{V_{reset}}{n} = \left(\frac{D}{1-D}\right) * \frac{V_g}{n} \tag{2.48}$$

The RMS current through synchronous rectifier S3 is

$$i_{S3} = I_o * \sqrt{D} \tag{2.49}$$

The RMS current through synchronous rectifier S4 is

$$i_{S4} = I_o * \sqrt{1-D} \tag{2.50}$$

Chapter 3

Small signal modeling of Low side ACFC with Synchronous Rectification

Chapter 3

3. Small signal modeling of Low side ACFC with SR

3.1 Introduction

As every pulse width modulated converter operates as a nonlinear time variant system during different modes of a switching period due to the nonlinear switching devices present in the circuit so to linearize the nonlinear components into linear equations small signal modeling analysis has been done. There are different methods to perform the small signal analysis like state space averaging, circuit averaging, current injection methods etc.

The state space equations are written by considering the following assumptions

1. Assume continuous conduction mode operation of the converter.
2. Assume all the semiconductor switches as ideal i.e., neglect the on resistances of the body diodes and parasitic capacitances.
3. The dead time between the main switch ON and OFF time is neglected.
4. The main switch on time is DT_s and off time is $(1-\mathrm{D})\mathrm{T}_s$ over a switching period.

3.2 State space equations of the converter in ON and OFF state

a) ON state

The active clamp forward converter when the main switch is on is as shown in the fig 3.1 and the connected line shows the current flow during the on state and dotted line shows the open circuited components.

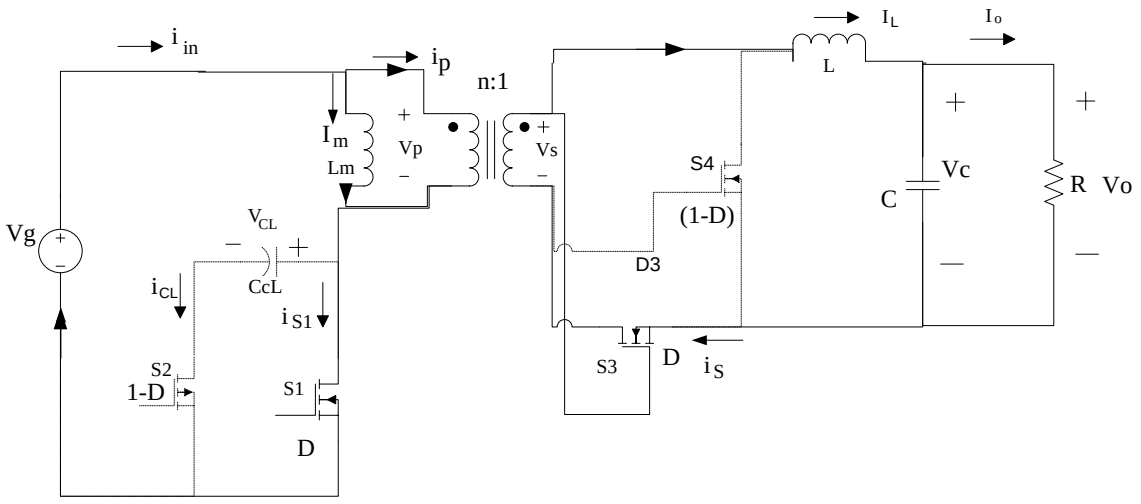


Figure 3.1 Low side ACFC with SR when during on state of switch S1

Applying KVL on the input side of the forward converter we have

$$\frac{di_m}{dt} = \frac{V_g}{L_m} \tag{3.1}$$

The current through the clamp capacitor i_{CL} is zero which is given by

$$\frac{dv_{CL}}{dt} = 0 \tag{3.2}$$

The current through the output capacitor is given by

$$i_C = i_L - i_o = C\frac{dv_C}{dt} \tag{3.3}$$

Also we have

$$i_o = \frac{v_o}{R} \tag{3.4}$$

By solving Eq. 3.4 and Eq. 3.5 we have

$$\frac{dv_c}{dt} = \frac{1}{C}i_L - \frac{1}{RC}v_C \tag{3.5}$$

Apply KVL across the secondary side of the forward converter by considering voltage across the secondary, output inductor and output capacitor we have

$$v_s = L\frac{di_L}{dt} + v_c \tag{3.6}$$

$$\frac{di_L}{dt} = \frac{1}{L}v_s - \frac{1}{L}v_L \tag{3.7}$$

By writing the states and state vectors in matrix form for the converter during on time we have

$$\begin{bmatrix} \frac{di_m}{dt} \\ \frac{dv_{CL}}{dt} \\ \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & \frac{1}{\mathrm{C}} & -\frac{1}{\mathrm{RC}} \end{bmatrix} \begin{bmatrix} i_m \\ v_{CL} \\ i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_g \tag{3.8}$$

The output equation is given by

$$v_o = i_o R \tag{3.9}$$

By substituting i_o from Eq. 3.4 in Eq. 3.10 we have

$$v_o = i_L R - RC\frac{dv_C}{dt} \tag{3.10}$$

Substitute Eq. 3.6 in Eq. 3.11 we have

$$v_o = v_C \tag{3.11}$$

In matrix form the output equation is written as

$$v_o = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_m \\ v_{CL} \\ i_L \\ v_C \end{bmatrix} \tag{3.12}$$

The state space equation of time invariant system during on state is given by

$$\frac{dx}{dt} = A_{on}x + B_{on}u \tag{3.13}$$

The output equation during on state is given by

$$y = C_{on}x \tag{3.14}$$

By comparing Eq. 3.9 with Eq. 3.14 and Eq. 3.10 with Eq. 3.15 we have

$$x = \begin{bmatrix} i_m \\ v_{CL} \\ i_L \\ v_c \end{bmatrix}, y = v_o, u = V_g \tag{3.15}$$

$$A_{on} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & \frac{1}{\mathrm{C}} & -\frac{1}{\mathrm{RC}} \end{bmatrix}, B_{on} = \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix}, C_{on} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.16}$$

b) OFF state

The active clamp forward converter when the main switch S1 is off is as shown in the Fig 3.2 and the dotted line shows the open circuited path and the connected line shows the current flow during the state.

Applying the KVL to input loop through the clamp capacitor, we have

$$\frac{di_m}{dt} = \frac{1}{L_m}v_g - \frac{1}{L_m}v_{CL} \tag{3.17}$$

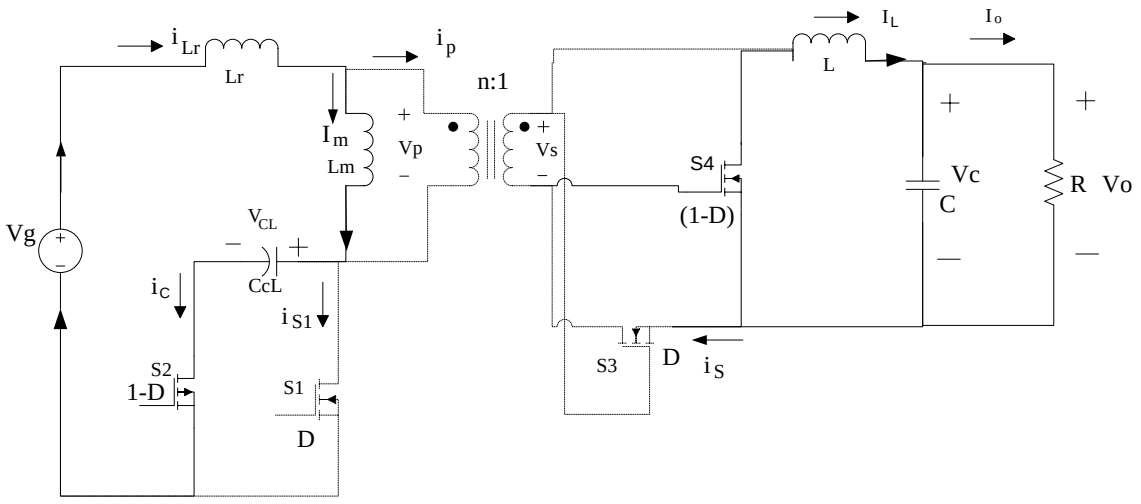


Figure 3.2 Low side ACFC with SR when during off state of switch S1

The current through the clamp capacitor is given by

$$i_m = C_{CL}\frac{dv_{CL}}{dt}$$
$$\frac{dv_{CL}}{dt} = \frac{1}{C_{CL}} i_m \tag{3.18}$$

By applying the KVL to the secondary side of the converter we have

$$L\frac{di_L}{dt} + v_C = 0$$
$$\frac{di_L}{dt} = -\frac{1}{L} v_C \tag{3.19}$$

The current through the output capacitor is given by

$$i_C = i_L - i_o = C\frac{dv_C}{dt} \tag{3.20}$$

$$\frac{dv_C}{dt} = \frac{1}{C} i_L - \frac{1}{RC} v_c \tag{3.21}$$

The state space equations of the ideal low side active clamp forward converter during off time in matrix form is

$$\begin{bmatrix} \frac{di_m}{dt} \\ \frac{dv_{CL}}{dt} \\ \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_m} & 0 & 0 \\ \frac{1}{C_{CL}} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & \frac{1}{\mathrm{C}} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_m \\ v_{CL} \\ i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_g \tag{3.22}$$

The output equation in matrix form is given by

$$v_o = v_C = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_m \\ v_{CL} \\ i_L \\ v_C \end{bmatrix} \tag{3.23}$$

The basic state space equation of time invariant system during off state is given by

$$\frac{dx}{dt} = A_{off} x + B_{off} u \tag{3.24}$$

The output equation during off state is given by

$$y = C_{off} x \tag{3.25}$$

By comparing the Eq. 3.24 with Eq. 3.26 and Eq. 3.25 with Eq. 3.27 we have

$$A_{off} = \begin{bmatrix} 0 & -\frac{1}{L_m} & 0 & 0 \\ \frac{1}{C_{CL}} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & \frac{1}{\mathrm{C}} & -\frac{1}{RC} \end{bmatrix}, B_{off} = \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix}, C_{off} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.26}$$

3.3 State space averaging method

The converter acts as a nonlinear time variant system over a switching period and it is a linear time invariant system when the switch is on and when the switch is off as all the circuit parameters are constant in each state. Hence state space averaging over switching cycle of each state is done to make the converter a time invariant system. After averaging the system is perturbed and linearized around the steady state operating point to make a continuous time invariant system.

The averaged model of the two states of the converter over a switching period is written as

$$\begin{aligned} \frac{dx}{dt} &= [A_{on}d(\mathrm{t}) + A_{off}(1-d(\mathrm{t}))]*\mathrm{x(t)} + [\mathrm{B}_{on}\mathrm{d(t)} + \mathrm{B}_{off}(1-\mathrm{d(t)})]*\mathrm{u(t)} \\ \mathrm{y} &= [C_{on}\,\mathrm{d(t)} + C_{off}(1-d(\mathrm{t}))]*\mathrm{x(t)} \end{aligned} \tag{3.27}$$

When the converter is averaged over the time period, the duty cycle d(t) which is a time invariant system also controls the output signal hence in addition to the control signal u(t),duty cycle d(t) is also added and the new control vector is defined and is given by

$$u' = \begin{bmatrix} u(\mathrm{t}) \\ d(\mathrm{t}) \end{bmatrix} \tag{3.28}$$

Then the linear system defined in Eq. 3.29 is written as function of vectors $x(\mathrm{t}), \mathrm{u}'(\mathrm{t})$ and is given as

$$\begin{aligned} \frac{dx}{dt} &= f(\mathrm{x(t)}, \mathrm{u}'(\mathrm{t})) \\ \mathrm{y(t)} &= \mathrm{g(x(t)}, \mathrm{u}'(\mathrm{t})) \end{aligned} \tag{3.29}$$

Then the linear system defined in Eq. 3.31 is perturbed and is written as

$$\begin{aligned} x(\mathrm{t}) &= \mathrm{X} + \hat{\mathrm{x}}(\mathrm{t}) \\ \mathrm{u}'(\mathrm{t}) &= \mathrm{U}' + \hat{\mathrm{u}}'(\mathrm{t}) \\ \mathrm{y(t)} &= \mathrm{Y} + \hat{\mathrm{y}}(\mathrm{t}) \end{aligned} \tag{3.30}$$

The linear system defined in Eq. 3.29 is linearized around a steady state operating point $x(t) = X, u'(t) = U'$ and steady state equations of Eq. 3.29 are

$$\begin{aligned} 0 &= A*X + B*U \Rightarrow X = -A^{-1}BU \\ Y &= C*X \Rightarrow Y = -CA^{-1}BU \end{aligned} \tag{3.31}$$

where

$$\begin{aligned} A &= A_{on}*D + A_{off}(1-D) \\ B &= B_{on}*D + B_{off}(1-D) \\ C &= C_{on}*D + C_{off}(1-D) \end{aligned} \tag{3.32}$$

The small signal equations are given by

$$\begin{aligned} \frac{d\hat{x}}{dt} &= A'\hat{x}(t) + B'\hat{u}'(t) \\ \hat{y}(t) &= C'\hat{x}(t) \end{aligned} \tag{3.33}$$

After linearizing around the steady state operating point $x(t) = X, u'(t) = U'$ we have

$$\begin{aligned} A' &= A \\ B' &= \begin{bmatrix} B & (A_{on} - A_{off})X + (B_{on} - B_{off})U \end{bmatrix} = \begin{bmatrix} B & H \end{bmatrix} \\ C' &= C \end{aligned} \tag{3.34}$$

Considering the input state as zero the control to output transfer function, audio susceptibility and output impedance transfer functions are derived. Hence the Laplace transform is applied by considering zero state input to the eq 3.35 and we get

$$\begin{aligned} \hat{x}'(s) &= (sI - A)^{-1}B'\hat{u}'(s) \\ y &= C\hat{x}'(s) \end{aligned} \tag{3.35}$$

3.4 Deriving control to output transfer function

The control to output transfer function is obtained by using the equation

$$G_{V_o d} = C(sI - A)^{-1} * H = C(sI - A)^{-1} * [(A_{on} - A_{off})X + (B_{on} - B_{off})U] \tag{3.36}$$

Therefore from Eq. 3.17 and Eq. 3.28 we have,

$$A=\begin{bmatrix} 0 & -\frac{D'}{L_m} & 0 & 0 \\ \frac{D'}{C_{CL}} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}, H=\begin{bmatrix} \frac{1}{L_m}V_{CL} \\ \frac{1}{L_m}i_m \\ \frac{1}{nLC}V_g \\ 0 \end{bmatrix}, C=\begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.37}$$

The control to output transfer function is

$$G_{V_o d}=\frac{V_g \big/ nLC}{s^2+\frac{1}{RC}s+\frac{1}{LC}} \tag{3.38}$$

Chapter 4

Closed loop control of Low side ACFC with Synchronous Rectification

Chapter 4

4. Closed loop control of Low side ACFC with SR

4.1 Introduction

The transfer function derived in chapter 3 using state space analysis is used to analyze the stability analysis of the converter. For any converter the regulation of output voltage, current and stability of the converter according to the application are two important requirements. To satisfy these requirements we move to the closed loop control. The stability of the converter is ensured by modeling a controller satisfying the stability requirements and minimize the error in the output voltage by regulated controlling the pulse-width modulation.

Basically there are many control topologies available to regulate the output voltage using PWM switching like voltage mode control, current mode control etc. In my work I designed a voltage mode control for the low side ACFC topology with SR. The error voltage is regulated by the PID controller. Also as there are two switches that are to be driven in this topology i.e., the main switch is of N-type operated during the on time and the auxiliary switch is of P-type operates during the off time. Hence complementary gate pulses are to be generated so an R-C phase shifting network is used to shift the pulses generated during on time and are given to the auxiliary switch during off time.

4.2 Voltage mode control of single output Low side ACFC with SR

The block diagram of closed loop voltage mode control is shown in Fig 4.1

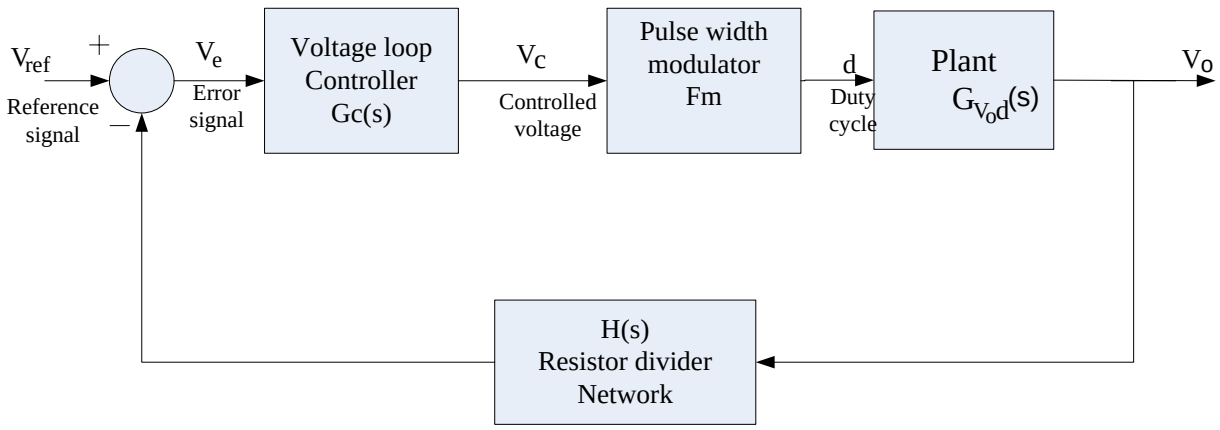


Figure 4.1 Block diagram of closed loop voltage mode control

From fig 4.1 we can say that the output voltage is sensed with the resistor divider network and it is compared with the reference voltage and error voltage is generated. This error voltage is regulated with the help of a controller and controlled voltage

The loop transfer function of the closed loop voltage mode control shown in Fig 4.1 is

$$T = G_{V_o d}(\mathrm{s}) * \mathrm{H(s)} * \mathrm{G}_C(\mathrm{s}) * \mathrm{F}_m \tag{4.1}$$

The phase margin for the whole closed loop system is

$$\begin{aligned} PM &= 180 + \angle G_{V_o d}(\mathrm{j}\omega_{gc}) + \angle H(\mathrm{j}\omega_{gc}) + \angle \mathrm{G}_C(\mathrm{j}\omega_{gc}) + \angle \mathrm{F}_m(\mathrm{j}\omega_{gc}) \\ \mathrm{PM} &= 180 + \angle G_{V_o d}(\mathrm{j}\omega_{gc}) + \angle \mathrm{G}_C(\mathrm{j}\omega_{gc}) \end{aligned} \tag{4.2}$$

From the Eq. 4.2 we can say that the phase of the closed loop system is contributed only by the plant and the controller transfer function as the pulse width modulator gain and the resistor divider network i.e., feedback H(s) does not contribute any phase as they are constants.

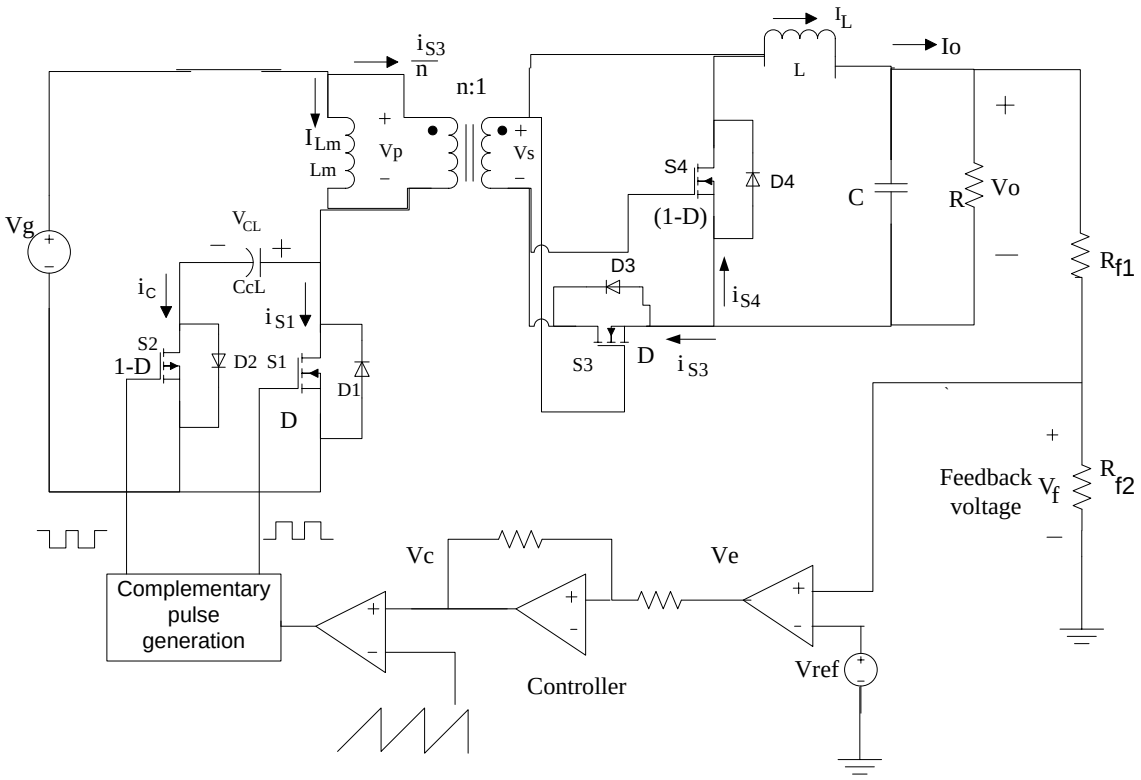


Figure 4.2 Closed loop voltage mode controlled Low side ACFC with SR

The voltage mode controlled single loop Low side ACFC with SR closed loop model is presented in Fig 4.2. As the working and control to transfer function derivation is presented in previous chapters the feedback loop is discussed in detail

4.2.1 Feedback network

The feedback voltage is sensed from the resistor divider network connected across the output voltage. The feedback resistors used are of the order of Kilo and Mega ohms such that very less current flows through and the power loss is minimum.

The sensed feedback voltage is given by

$$V_f = \frac{R_{f2}}{R_{f1} + R_{f2}} V_o \tag{4.3}$$

The transfer function of the feedback network is given by

$$H(\mathrm{s}) = \frac{V_f}{V_o} = \frac{R_{f2}}{R_{f1} + R_{f2}} \tag{4.4}$$

4.2.2 Controller design

A PID controller comprising of PI controller and lead compensator is designed using frequency domain analysis to improve the steady state and transient state behavior. A lead compensator introduces a phase at the specified gain cross over frequency f_{gc}, increase the bandwidth of the system and improve the transient state behavior of the system. The PI controller is used to improve the low frequency gain and also the steady state response of the system.

Lead compensator works similar to PD controller and to design it the gain margin and phase cross over frequency of the closed loop system are to be known. Basically closed loop system is designed for a gain cross over frequency of one tenth of switching frequency and a phase-margin of 60 degree to avoid the aliasing phenomena. The controller is designed from the bode plot of the open loop plant transfer function of the converter.

The structure of lead compensator is given by

$$C = K\frac{(1+ {}^{s}\!/\!_{\omega_z})}{(1+ {}^{s}\!/\!_{\omega_p})} = K\frac{(1+ {}^{s}\!/\!_{a})}{(1+ {}^{s}\!/\!_{\alpha a})}; \alpha > 1 \tag{4.5}$$

The specifications to be considered for designing the lead compensator are

a) Phase margin of the closed loop system
b) Gain cross over frequency of the closed loop system.

The steps that are considered while designing the lead compensator are

a) From the phase margin condition defined in Eq. 4.2 the phase margin to be provided by the compensator i.e., $\varphi_{C,\max}$ at the required gain cross over frequency and phase margin is calculated.

b) Then the value of α is calculated using the equation

$$\alpha = \frac{1+\sin\varphi_{C,\max}}{1-\sin\varphi_{C,\max}} \tag{4.6}$$

c) The value of zero of the lead compensator is calculated using the equation

$$a = \frac{2\pi f_{gc}}{\sqrt{\alpha}} \tag{4.7}$$

d) The value of pole of lead compensator 'αa' is calculated using the values found from Eq. 4.6 and Eq.4.7

e) The value of constant K is found using the equation

$$20\log(|T(s)|)_{@f_{gc}} = [20\log(|G_{V_0 d}(s)|) + 20\log(|G_c(s)|) + 20\log(|H(s)|) + 20\log(|F_m|)]_{@f_{gc}} \tag{4.8}$$

A PI controller is designed at the same gain cross over frequency to improve the low frequency gain of the controller.

4.2.3 Pulse width modulation

The gate driving MOSFET pulses are generated by comparing the controlled error voltage with the saw tooth wave of amplitude V_M repeating with time period T_s.The normal pulse width modulator operation and the transfer function of the pulse width modulator is as shown in Fig 4.3

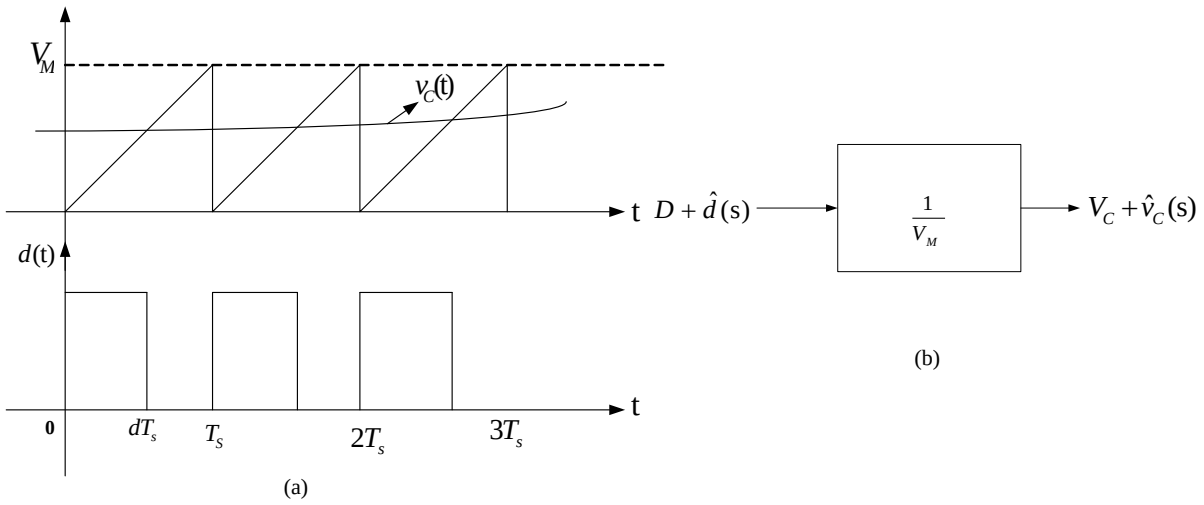


Figure 4.3 Pulse width modulator generating the pulses and the transfer function

The pulses are generated from the pulse width modulator using the condition

$$d(\mathrm{t}) = \frac{v_C(\mathrm{t})}{V_M}, 0 \le v_C(\mathrm{t}) \le V_M \tag{4.9}$$

As shown in the block diagram my topology requires complementary pulse width modulation and positive gate pulses for main N-channel MOSFET switch during on period and negative gate pulses for the auxiliary P-channel MOSFET switch during off period.

Chapter 5

Simulation & Results

Chapter 5

5. Simulation & Results

5.1 Specifications and List of components used in the simulation

The specifications of the designed Low side ACFC with SR are

a) Switching frequency =100KHz
b) Nominal voltage = 48V
c) Output voltage = 3.3V
d) Output current =30 Amps
e) Output current ripple = 30 mA(peak-peak)
f) Output voltage ripple=10% of output voltage

The list of components used in the simulation are tabulated below

Table 5.1 List of components

Symbols	**Components**	**Symbols**	**Components**
S1	IRF3710Z	S2	IRF7425
S3	IRF2804	S4	IRF2804
L	5.34µH	C	672µF
L_m	78.6µH	C_{CL}	66nF

The designed plant control to output transfer function is given by

$$G_{v_o d} = \frac{4.46\text{X}10^{21}}{1.649\text{X}10^{12}s^2 + 2.499\text{X}10^{16}s + 5.148\text{X}10^{20}} \quad (5.1)$$

The designed controller transfer function is

$$G_C(s) = \frac{3.49304(s+2620.75)(s+3141.59)}{s(s+151683.95)} \tag{5.2}$$

For the listed specifications and the component list presented above the Low side ACFC with SR has been designed and implemented in PSPICE.

5.2 Results

1. Open loop step response of the plant control to output transfer function

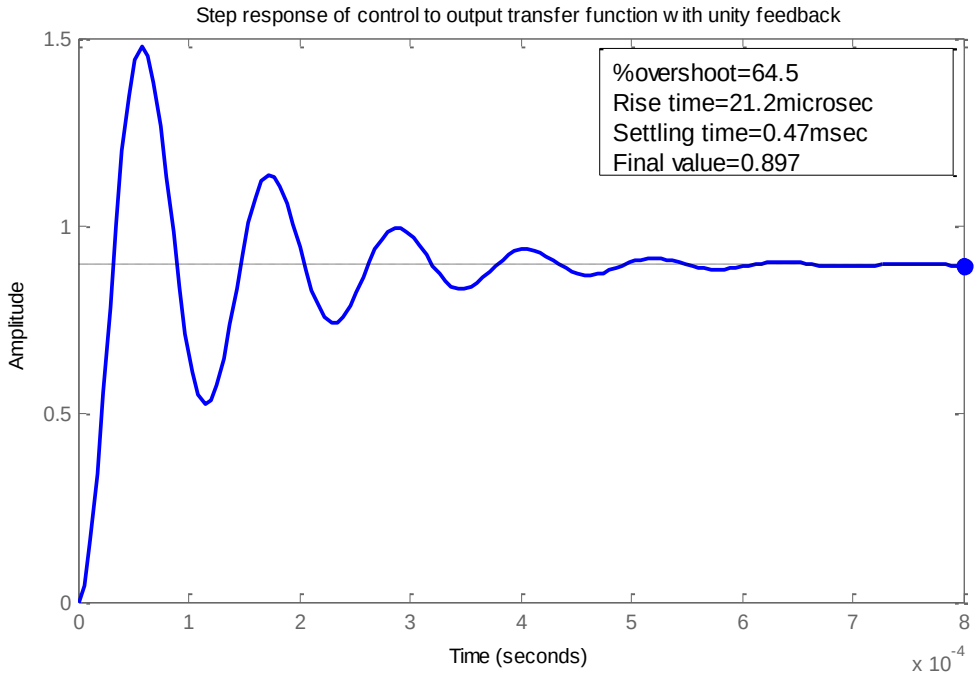


Figure 5.1 Step response of control to output transfer function with unity feedback

The %overshoot of the step response is very high and steady state error is observed to be 10.3% from the graph.

2. Bode plot of the Open loop control to output transfer function of the plant

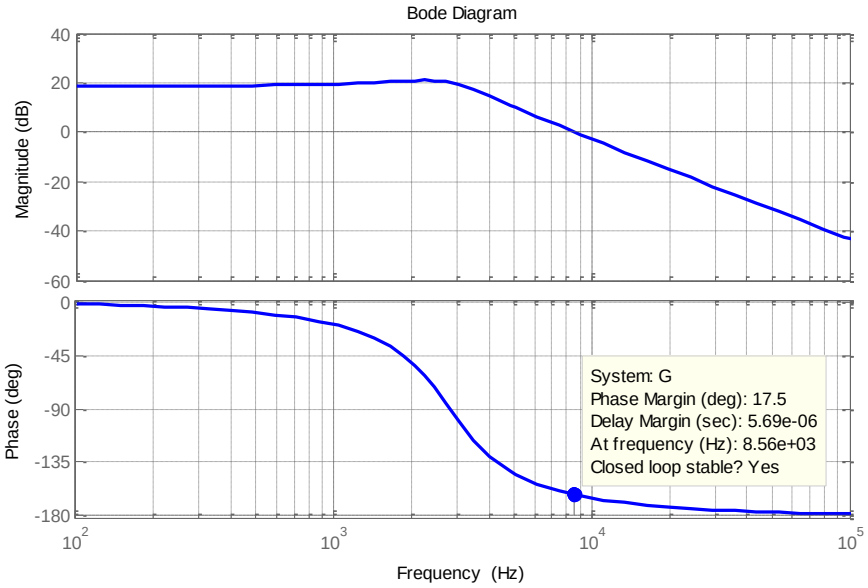


Figure 5.2 Step response of loop transfer function of closed loop converter

3. Closed loop step response of the voltage mode controlled Low side ACFC with SR

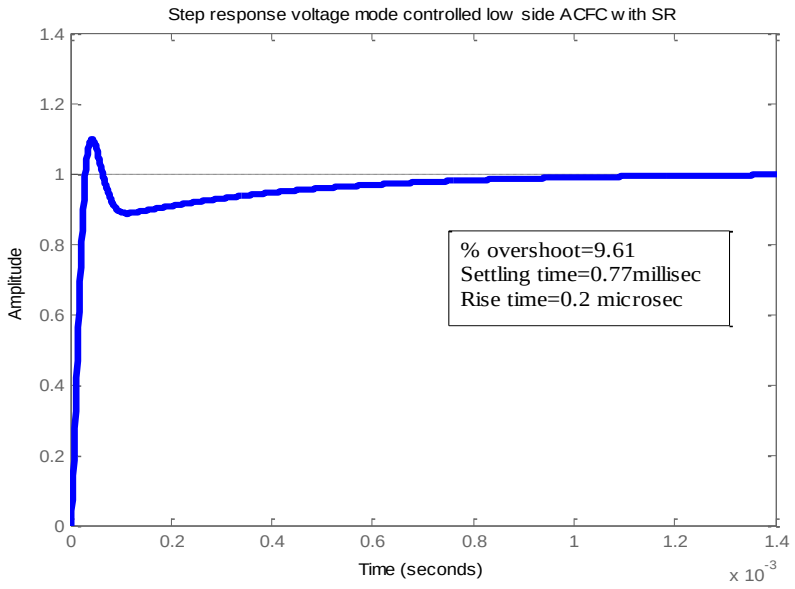


Figure 5.3 Step response of loop transfer function of closed loop converter

4. Bode plot of the voltage mode controlled Low side ACFC with SR loop transfer function

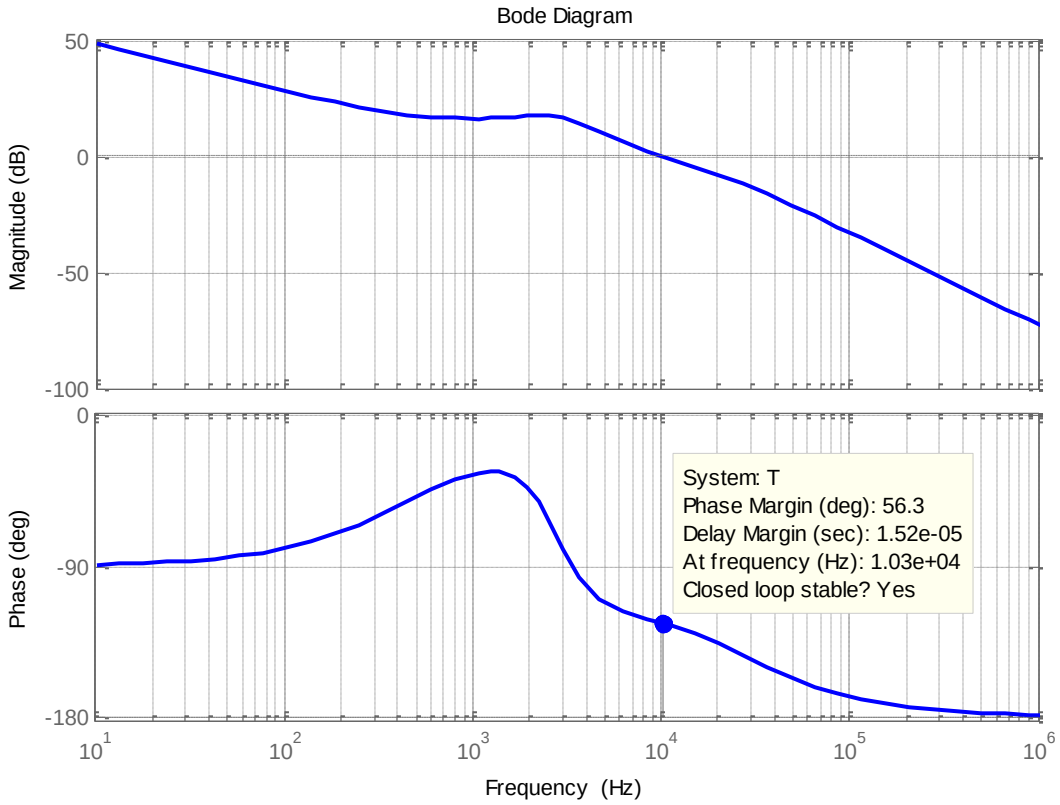


Figure 5.4 Bode plot of loop transfer function

5. Steady state Closed loop Low side ACFC with SR topology simulation results

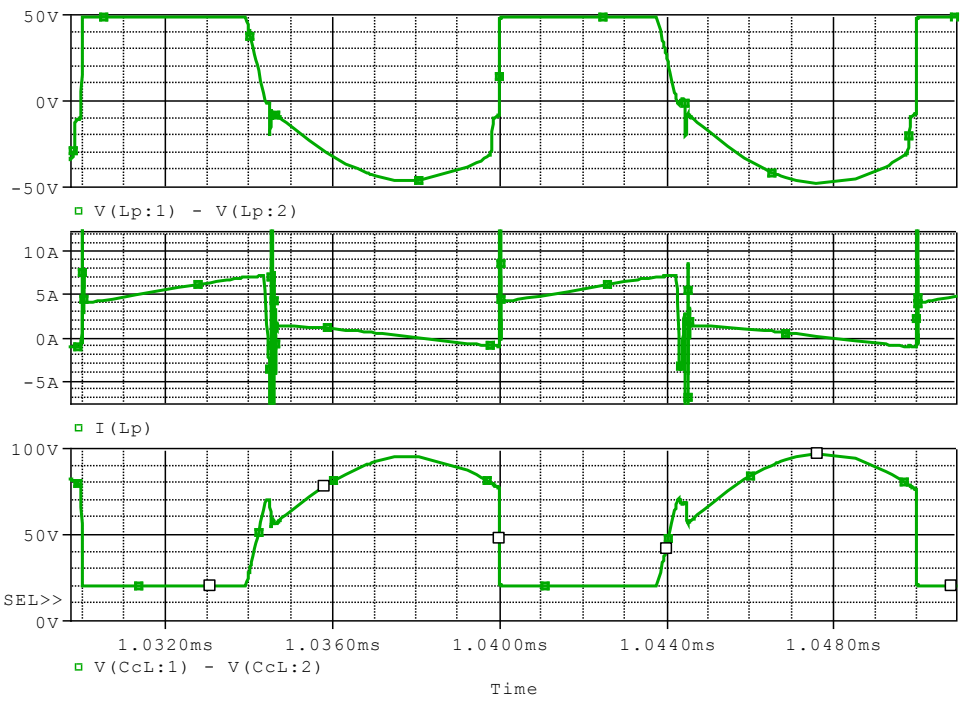


Figure 5.5 Voltage across the transformer primary, Inductor primary current and voltage across the clamp capacitor respectively

From the above figure we can notice that the inductor primary current is going negative and so we can say that the transformer is being reset. The voltage across the clamp capacitor follows the derived relation and resonance can be observed. Also transformer primary voltage is going negative which indicates the demagnetization of the transformer core.

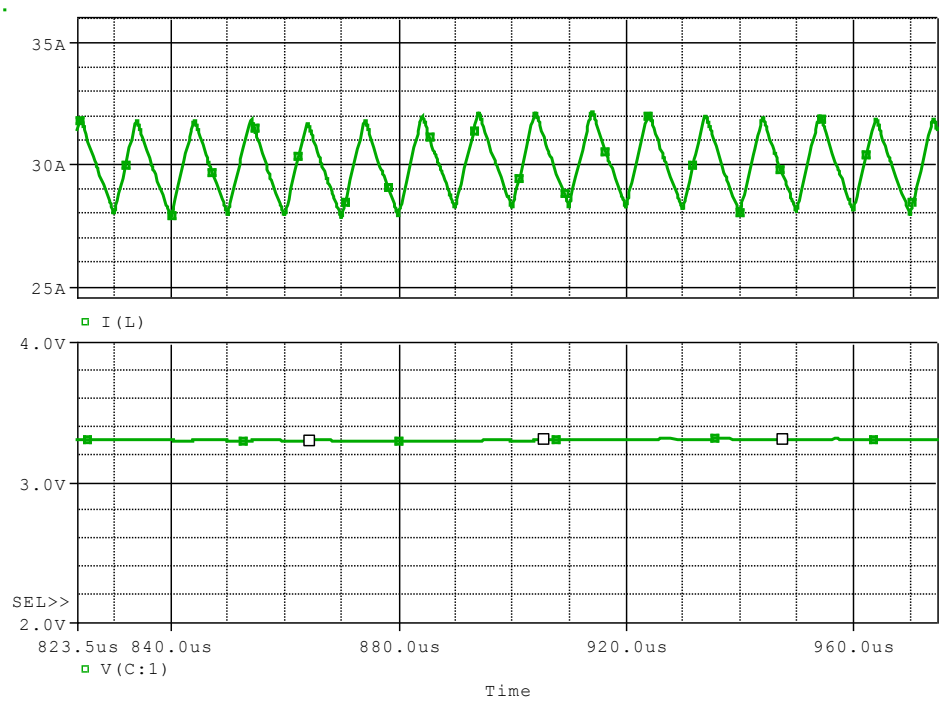


Figure 5.5 Output inductor and output voltage waveform

From the above figure it is observed that the output voltage is 3.3V and the output inductor current is having 30% ripple with an output current of 30 Amps and nearly 100W power is obtained from the converter.

Chapter 6

Conclusion and future work

Chapter 6

6. Conclusion and future work

6. 1 Conclusion

The comparative study of the various classical forward converter topologies have been presented. The design of Low side ACFC topology with SR for a switching frequency of 100 kHz to obtain an output voltage of 3.3volts and output current of 30Amp is done. The detailed steady state and transient state analysis of the topology i.e., 12 modes of operation over a switching period are derived and presented. The small signal modeling of the topology has been done using the state space averaging technique and the control to output transfer function of the converter has been derived. A controller is designed using frequency domain analysis to obtain a phase margin of 60 degree at gain cross over frequency of 10 kHz for the closed loop system. The voltage mode control of Low side ACFC with SR topology has been implemented in PSPICE. The PSPICE simulation results showing the switching of the main MOSFET, Auxiliary MOSFET and synchronous rectifiers and the resetting of the transformer primary magnetizing inductance has been presented.

6.2 Future scope

- To implement the peak current mode control of Low side ACFC topology with SR.
- To do detail analysis of multiple output Low side ACFC topology with SR
- To analyze the effect of cross regulation without and with coupled inductors
- To implement the weighted voltage mode controlled multiple output Low side ACFC with SR topology

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