Modeling and Simulation of Non-Classical MOSFETs for HP and LSTP Applications at 20 nm Gate Length

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Modeling and Simulation of Non-Classical MOSFETs for HP and LSTP Applications at 20 nm Gate Length

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by

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Dedicated
to
My Loving Parents,
Brothers and Sister.

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Certificate

This is to certify that the thesis entitled **"Modeling and Simulation of Non-Classical MOSFETs for HP and LSTP Applications at 20 nm Gate Length "** *by* **Devender Singh**, *submitted to the National Institute of Technology, Rourkela for the award of Master of Technology in Electrical Engineering, is a record of bonafide research work carried out by him in the Department of Electrical Engineering, under my supervision. I believe that this thesis fulfills part of the requirements for the award of degree of Master of Technology.The results embodied in the thesis have not been submitted for the award of any other degree elsewhere.*

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Devender Singh

Abstract

The endless miniaturization of Si-based Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) has the key for urging the electronic uprising. However, scaling of the channel length is the enormous challenge to preserve the performance in terms of speed, power, and electrostatic integrity at each technology nodes. From the commencement of CMOS scaling, the simple planar MOSFETs are not up to the performance because of the increased SCEs and leakage current. To slacken the SCEs and leakage currents, different types of structures i.e. Multi-Gate MOSFETs like double-gate (DG), triple-gate (TG), FinFETs have introduced in the literature. Fully Depleted (FD) Silicon-On-Insulator (SOI) devices have shown potentially significant scalability when compared to bulk MOSFETs. In spite of, the introduced structures in literature are not offering concurrent SCE repression and improved circuit implementation. And some involve tangled processing not suggested for smooth integration into the here and now CMOS technology.

The scaling capability of nanoscale ultra-thin (UT) silicon directly on insulator (SDOI) single gate (SG) and DG MOSFETs is investigated to overcome SCEs and improve power consumption. Dependence of underlap length on drain current, Subthreshold Slope (SS), transition frequency, delay, Energy Delay Product (EDP), etc. is studied for DG MOSFET and FinFET, to find the optimum value of underlap length for low power consumption. DG MOSFET is an excellent candidate for high current drivability whereas FinFET provides better immunity to leakage currents and hence improved delay, EDP over DG MOSFET. Furthermore, FinFET provides a high value of transition frequency which indicates that it is faster than DG MOSFET. III-V channel materials are proposed for the discussed two structures to improve the On current at the same integration density as in Si-based channel FETs. The role of geometry parameters in sub 20 nm SOI FinFET is studied to find the optimum value of height and width of Fin for analog and RF circuit design. This work provides the influence of the height and width of Fin disparity on different performance matrices that comprises of static as well as dynamic figures of merit (FoMs). Based on the Aspect Ratio (W_{Fin}/H_{Fin}), the device can be divided into three parts, i.e., FinFET, Tri-gate, and Planar MOSFET.

CMOS for SG and DG is made using the combination of NMOS and PMOS by engineering the work function in order to have same threshold voltage for N-channel and P-channel MOS. The inverter is without doubt the core of all digital applications. Once its operation and characteristics are understood with clarity, designing more complicated structures such as NAND gates, multipliers, adders, and microprocessors are significantly explained. The performance of CMOS is articulated. All the dimensions are according to the ITRS 2013 datasheet. The work provided here is requisited to give the purpose for forward experimental investigation.

Keywords: High Performance (HP), Low Standby Power (LSTP), MOSFET, Silicon Directly on Insulator (SDOI), FinFET, CMOS, Aspect Ratio (AR), Figure of Merits (FoMs).

List of Acronyms

Acronym	Description
ITRS	International Technology Roadmap for Semiconductors
CMOS	Complementary Metal-Oxide Semiconductor
TCAD	Technology Computer Added Design
IC	Integrated Chip
RF	Radio Frequency
SoC	System on Chip
TFTs	Thin Film Transistors
SOI	Silicon on Insulator
UTB	Ultra Thin Body
MugFETs	Multiple Gate Mosfets
FD-SOI	Fully Depleted Silicon on Insulator
DG MOSFET	Double Gate Metal-Oxide Semiconductor Field Effect Transistor
SS	Sub-threshold Slope
$DIBL$	Drain Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
SCEs	Short Channel Effects
HCEs	Hot Carrier Effects
CLM	Channel Length Modulation
DM	Dual Material
PDP	Power Delay Product
EDP	Energy Delay Product
LP	Low Power
HP	High Performance
LSTP	Low Standby Power
SiGe	Silicon Germanium
FoMs	Figures of Merit
TGF	Transconductance Generation Factor
TCP	Temperature Compensation Point
2-D	Two Dimenssion
3-D	Three Dimenssion
AR	Aspect Ratio

List of Symbols

Symbol	Description
$V_{th} or V_T$	Threshold Voltage
$V_{GS} or V_{gs}$	Gate to Source Voltage
$V_{DS} or V_{ds}$	Drain to Source Voltage
$I_{ds} or I_D$	Drain Current
$t_{ox} or T_{ox}$	Gate-Oxide Thickness
t_b	Buried Oxide Thickness
$L_g or L$	Channel Length
W	Channel Width
N_A	Acceptor Doping Concentration
N_D	Donor Doping Concentration
$t_{Si} or T_{Si}$	Silicon Body Thickness
ϵ_{Si}	Permittivity of Silicon
ϵ_{ox}	Permittivity of Oxide
N_{Sub}	Substrate Doping
I_{on}	On-State Drive Current
I_{off}	Off-State Leakage Current
g_m	Transconductance
g_d	Output Conductance
E_v	Early Voltage
A_V	Intrinsic Gain
C_{gs}	Gate to Source Capacitance
C_{gd}	Gate to Drain Capacitance
f_T	Cut-off Frequency
C_T	Total Internal Capacitance
ϕ_M	Metal Work Function
ϕ_{Si}	Silicon Work Function
V_{bi}	Built-in Potential
X	Germanium Mole Fraction
t_{s-Si}	Strained Silicon Thickness
E_C	Electron Affinity
E_G	Energy Band Gap
η	Body Factor
SiO_2	Silicon Dioxide
Si_3N_4	Silicon Nitride
T_K	Thickness of High-k Dielectric
φ_S	Surface Potential
v_{Sat}	Saturation Velocity

continued on the next page

List of Symbols (*continued*)

Symbol	Description
V_{FB}	Flat Band Voltage
η_i	Intrinsic Carrier Concentration

List of Used Constants with their Values

Constants	**Values**
Electronic Charge (q)	$1.6 * 10^{-19} Coulomb$
Electron Mass (m)	$9.1 * 10^{-31} Kg$
Permeability of Vacuum (μ_0)	$4\pi * 10^{-7} H/m$
Permittivity of Vacuum (ε_0)	$8.85 * 10^{-12} F/m$
Boltzmann Constant (k_B)	$1.38 * 10^{-23} J/K$
Permittivity of Silicon (ε_{Si})	11.68
Permittivity of SiO_2(ε_{SiO_2})	3.9
Permittivity of Si_3N_4($\varepsilon_{Si_3N_4}$)	7.5
Room Temperature (T)	300 K
Thermal Voltage (V_T)	26 mV
Intrinsic Carrier Concentration (η_i)	$1.45 * 10^{10} cm^{-3}$

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Chapter 1
Introduction

1.1 Background

For high density integrated circuits such as microprocessors and semiconductor memories, most important device used is metal-oxide-semiconductor-field-effect transistor (MOSFET). The principle proposed by Lilienfeld and Heil, with subsequently the first MOSFET reported by Kahng and Atalla in 1960. The integrated circuit processing techniques have led to continuing reduction in both horizontal and vertical dimensions of the devices. Both the performance and density of the devices have grown exponentially with the shrink of technological channel length and fabrication cost.

Betterment in the device performance can be cognizable by

- Induction of high charge density for a specified gate voltage through multi-gate device architecture and lower operating temperature.
- Enhancement of the carrier transport through improving the mobility of materials (strain-Si, InGaAs, Ge, GaAs, InP etc.), reducing mobility decelaration factors or ballistic transport (with a small channel length).
- Reduction of parasitic resistance and capacitance (e.g. Extended/Raised source/drain, Silicon-on-Insulator (SOI), multi-gate MOSFETs (MuGFETs) etc.).

Apart from above, various quests have been readily performed out in device region to sustain Moore‘s Law and diversified technologies as ”More than Moore” [1]. To diminish short channel effects (SCEs) in nanoscale MOSFETs multi-gate architecture is the one of emerging novel device structures. Balestra et al. [2] was the first proposer of the double gate (DG) MOSFET. Many investigations have been done for multi-gate devices to comply with static electrical figures of merit (FoMs) such as I_{on}/I_{off} ratio, drain induced barrier lowering (DIBL), subthreshold slope (SS) etc. as per requirements of ITRS for logic operation [3].

Ultra-thin-body (UTB) MOSFETs are alluring pretendents for a nanoscale device since they show superior electrostatic integrity (E.I.). SCEs can be more curtailed by the adoption of thin BOX architecture (UTBB) in which the hidden oxide width is shortened for improved gate controllability reported by Burignat et al. [4]. In the nanoscale MOSFET, the double gate (DG) ultra-thin-body (UTB) architecture with undoped channel removes intrinsic parameter variations and underrates impurity scattering. As per the investigation of Hisamoto et al. and Solomon et al., the double gate architecture is suitable for higher current drive potential and superior regulation of SCEs. Non classical silicon MOS structures such as 3D FinFETs, 2D DG-MOSFET are coming in place of the conventional bulk MOSFETs because of their ability to attain higher speeds and reduced short channel effects (SCE′s) with the added advantage to design highly integrated CMOS circuits and better analog/RF applications.

In this study a numerical study is operated by using device simulator considering a nanoscale UTB DG-MOSFET in sub 100 nm gate length. The impact of static electrical FoMs (I_{on}/I_{off} ratio, DIBL) is compared with UTB SG-MOSFET with miniaturization of gate length up to 20 nm. The effects of different high mobility channel materials (GaAs, $In_{0.53}Ga_{0.47}$As) are studied and analyzed by comparing with the Si for DG-MOSFET.

With the continuation of CMOS scaling the conventional planar MOSFET′s leads to increase in SCE′s and leakage current. In order to overcome SCE′s and leakage current, different device Multigate MOSFETs (Mug-FET) structures like the Double gate, Tri gate, FinFET were proposed. Among these devices, FinFETs have acquired attentions because of their low cost process steps and compatibility with CMOS technology. Continuous development and research in the areas of devices and materials have lastly conveyed the III-V FinFETs with an agreement of higher device performances. The FinFET performance depends on the process induced variations categorized under systematic values of gate length L_g, underlap gate length L_{un}, gate oxide thickness t_{ox}, fin height H_{Fin} and fin width W_{Fin}. This work systematically presents various performance metrics of a GaAs based FinFET. We have also analyzed the sensitivity of parameters towards the process variation like H_{Fin} and W_{Fin}.

The main constituent of electronics is the integrated circuit (IC), and that integrates the essential components of circuits - namely resistors, capacitors, inductors, diodes and transistor. The two very crucial factors of automated circuits are transistors and memory chips. From the past two years, the leading device for ICs have been the MOSFETs. Along technology progress and great scalability of the device architecture, silicon based MOSFET VLSI circuits have steadily brought gain performance and cost decline to semiconductor slices for data processing and memory operations. The semiconductor industry showed a magnificent exponential rise in the number of transistors in a chip for profuse decades, as vaticinated by Moore′s law. The regular progress in Si-based CMOS technology has allowed the determined development of electronics, information technology, and communications. This continued advancements have been achieved especially by the dimensional scaling. Si-based technology to improve device density and performance has been achieved by CMOS scaling. Along each technology node, regularly expanding the economic productivity has been achieved by the cut in cost-per-function.

Besides scalability, the other different device features as input resistance, static power dissipation, and easy process means have formed CMOS transistors as the prime constituent of the ongoing integrated circuits (ICs). Now-a-days, CMOS ICs are found in all places and indispensable in our daily life, extending from handy electronics to transportation and telecommunications. Abundance research has done in device design bygone last thirty years, still the development of process hi-tech technologies creates fresh barriers as well as unique opportunities to device engineers. When the device scaling was ongoing in the 21st century, historical growth was tremendous as the circuit density gets doubled and performance also increased by 40% at every technology node, it confirmed that only typical scaling theory cannot continue the Moore′s Law.

When the scaling of CMOS comes in the nanometer region, a lot of genuine puzzles named as short channel effects (SCEs) show up. A few of these issues being as added on leakage currents, difficulty in gain of on-current, large parameter fluctuations, reduced reliability plus yield, gain in assembling cost, etc. In order to sustain the historical improvements, future technology scaling and to mitigate these small geometry effects to a considerable level, several strategies and new device structures have been researched and introduced. A few examples of those are; the continuous scaling of EOT with the use of high-k or metal gate stack gives the better electrostatic control over the channel, similar with use of Multi-

gate MOSFET architecture, silicon-on-insulator (SOI), Strained-Silicon (S-Si), Si nanowire/carbon nanotube FETs, etc. A lot of above discussed devices have given path for new device characteristics.

1.2 Future Technology Node Requirements

The factors or features to be distinguished betwixt various logic technologies are:

1.2.1 High performance (HP)

The high performance conforms to highly complicated ICs which need large values of clock frequencies and at the same time can handle the high power consumption. At the device standard, with an bettering of the intrinsic switching time of a transistor with 17% per year can accomplish the increase in clock frequency from one tech node to the next, at the same time controlling the transistor off-state current within the acceptable limits with respect to power consumption.

$$\mathrm{I} = \frac{\mathrm{Q}}{\mathrm{t}} = \frac{\mathrm{CV}}{\tau} \tag{1.1}$$

$$\tau = \frac{\mathrm{Q}}{\mathrm{I}} = \frac{\mathrm{CV}}{\mathrm{I}} \tag{1.2}$$

where, C stands for gate capacitance, V is the supply voltage, and I is the on-state current of the device. Therefore, the best effective method to achieve enhanced performance is to scale the gate length of the transistor aggressively. Consequently, this will result in reduced gate capacitance and at the same time increasing the on-state current.

1.2.2 Low operating power (LOP)

The low operating power comes at the cost of high performance and it is used for mobile applications, notebook computers, etc. Operating power consumption is also known by the name of dynamic power consumption, is the consumption of the power when the device is in use. The main issue to tackle here is to decrease the dynamic power consumption maintaining the high performance of the device. The dynamic power consumption at the device level is a measure of power-delay product given by

$$\mathrm{P}\tau = \frac{\mathrm{CV}}{\mathrm{I}}\mathrm{P} = \frac{\mathrm{CV}}{\mathrm{I}}\mathrm{VI} \tag{1.3}$$

$$\mathrm{P}\tau = \mathrm{CV}^2 \tag{1.4}$$

Therefore, the best effective method to reduce the dynamic power consumption is to curtail the supply voltage as much as possible i.e.$V \Downarrow \Rightarrow P\tau \Downarrow \Rightarrow$ Dynamic Power Consumption (given by $0.5CV^2f$) decreases.

1.2.3 Low stand-by power dissipation (LSTPD)

The low stand by power dissipation is the measure of the power dissipation when the device is off. This comes at the cost of performance and used in the low cost consumer applications such as in cellular phones. For aforesaid applications, the major concern is to carry on circuit performance while keeping the power consumption as low as feasible when the IC is off. This static power consumption at the transistor level is controlled by the leakage current. Therefore, low stand-by power needs low off state currents as well as really low parasitic currents such as gate leakage current.

1.3 Technology Scaling

The oblique geometric aspects of devices and interconnects are decreased. This shortening in size is called as "scaling" of the geometric aspects of the unified circuits (IC). From the last few decades, the MOSFET has been continuously scaled down in size. There was a time when the channel lengths were in the range of micrometers, however at present MOSFETs in the range of nanometer range are available and used in integrated circuits.

As a consequence of this minimum feature size of ICs, the number of transistors have increased over time. The roadmap of semiconductor industry is provided by the ITRS that gives a report in which it tells about all the parameters of a device in transistor and all other relevant details of the device that should come by the designated year. Mainly, it provides the goal for the researchers. When we reduce the size of MOSFET there comes difficulties which are also related to the semiconductor device fabrication process, the demand to adopt very low volatges and deteriorated electrical characteristics are making it necessary to redesign the circuits and innovations.

1.3.1 Why MOSFET Scaling ?

We want newer generation of scaled down transistors to work faster. As shown in the below table that in the processor 4004, which was introduced in 1971, has 2250 transistors inside it. As we are moving ahead, we can see that the number of transistors are increasing by tremendous number. So to accommodate that much transistors inside a processor, the first task is to scale down the transistor so that it will become handy and can be accommodated in a less area. Approximately 4.2 crores of transistors are used Pentium 4 processor and we can see that chip area is very small and which comes by scaling the transistors used inside it as shown in table 1.1. The small size of MOSFETs is highly attractive for various goals. The essential basis to make transistors smaller and smaller is to integrate more and more number of devices in a designated chip area. This doubling of transistor density was initially seen by Gordon Earle Moore in 1965 and is commonly known to as Moore′s law.

Gordon Earle Moore (born January 3, 1929) is an American businessman, co-founder and Chairman Emeritus of Intel Corporation. It is also a known fact that small sized transistors switch faster. For example, one idea to reduce the size is to scale the MOSFET with all of its dimensions proportionally. The important device dimensions are length and width of channel and thickness of oxide. As

Table 1.1: Evolution

Processor Name	Year of Introduction	Transistors
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	1,20,000
386	1985	2,75,000
486 DX	1989	11,80,000
Pentium	1993	31,00,000
Pentium II	1997	75,00,000
Pentium III	1999	2,40,00,000
Pentium 4	2000	4,20,00,000

the factors discussed above are scaled down proportionally then resistance of the channel does not change but the capacitance of the gate reduces by proportionate factor and hence the delay as calculated by product of these two will scale down by the similar factor.

1.3.2 Moore's Law

Since 1965, the cost of one part of semiconductor memory has come down by 100 million times. Miniaturization is the main engine that boosted the conception of electronics. More number of circuits can be built on a silicon wafer by curtailing the transistor and interconnects sizes and in turn every circuit will become smaller [5]. The development in speed and power consumption in ICs has been possible by Miniaturization. Gordon Moore created an empirical examination in 1965 that the number of devices on a chip doubles every 18 months later it was rectified as 24 months or so as shown in Figure 1.1.

This Moore's law is a succinct explanation of the accelerated and determined trend of miniaturization. A new technology node is defined whenever the minimal line width is shortened. Examples of technology generations are shown in Table 1.2.

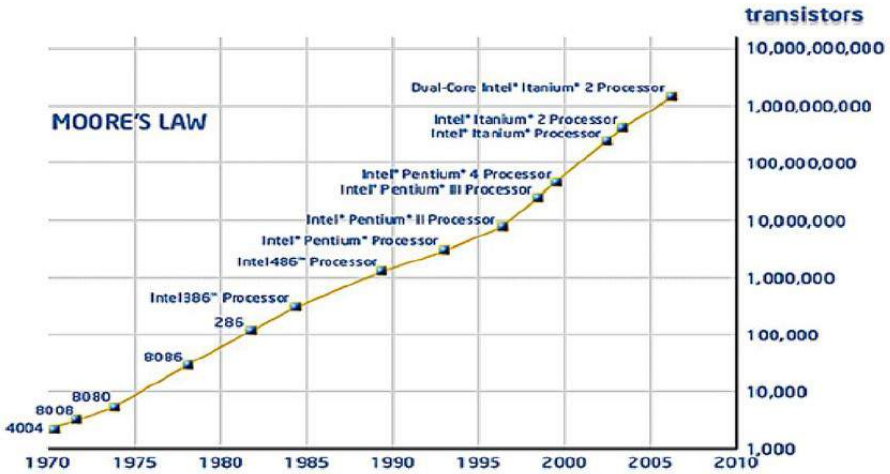


Figure 1.1: Moore's Law

Table 1.2: Improvements in Technology Node over the years

Year	2004	2006	2008	2010	2011	2013	2016	2022
Technology Node	90nm	65nm	45nm	32nm	22nm	16nm	14nm	10nm

The numbers shown in the table refers to the minimal metal line width. Poly-Si lengths may be much small. At each new node, entire characteristics of the circuit layout, like the contact holes, are decreased in size to 70% of the earlier node. After every two or three years, a new technology generation is given. The major award while introducing a new technology generation is the cut of circuit size by halved. (70% of earlier line width measures 50% reduction in area i.e., 0.7∗0.7=0.49).

It is intuitive that Moore′s Law cannot be sustained forever. So, there comes another solution to this is Koomey′s law as addressed by Prof. M. Jagadesh kumar in the recent ICEE conference 2014 in IISc Bangalore which indicates towards the computations per KWh.

1.3.3 Challenges to Miniaturization of MOSFETs

In spite of formidable desputes, however, many researchers and industry envision close variants of conventional microelectronic transistors ongoing miniaturized into the nanometer-scale region. For example, ITRS, circulated by the SIA, envisage that by the year 2010 chips will be built from transistors with channel lengths upto 70 nm. Alone running transistors with 40 nm channel lengths are already illustrated with silicon. And 25 nm channel length transistors are built from S-Si. But while scaling down FETs, we have obey some rules which are given in the table 1.3.

In increasing order of their intractability.

High Electric Fields

As the supply voltage is used in short channels, it causes the avalanche breakdown when hefty numbers of charge carriers comes out of the channel with huge energies thus creating current flood and destruction of the device. This problem may prevail in nano scaled devices which are built of bulk semiconductors.

Heat Dissipation

Due to finite thermo-dynamic efficiency, heat dissipation of devices causes obstacle in the more integration density in circuits and over heating can make the devices to malfunction. This type of issue is an obstacle for any type of heavily crowded circuits.

Subthreshold Current

It is the current flowing through the channel when the supply voltage is under the threshold voltage. Here the transistor should be off but reality is something else that is it is not off. Circuit speed gets better with rising Ion, therefore it would be good to work with small V_{th}.

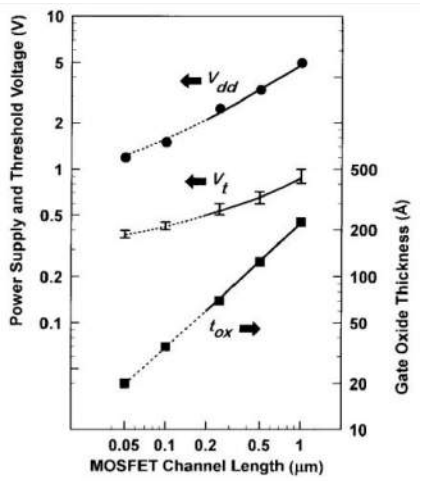


Figure 1.2: Scaling trend of power supply voltage (V_{dd}), threshold voltage (V_{th}), and gate-oxide thickness (T_{ox}) as a function of CMOS channel length

Table 1.3: Technology Scaling Rules for Three Cases

Physical Parameter	Constant Electric Field Scaling Factor	Generalized Scaling Factor	Generalized Selective Scaling Factor
Channel Length, Insulator Thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring Width, Channel Width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric Field in device	1	ε	ε
Voltage	$1/\alpha$	ε/α	ε/α_d
On-Current per device	$1/\alpha$	ε/α	ε/α_w
Doping	α	$\varepsilon\alpha$	$\varepsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate Delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power Dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_w\alpha_d$
Power Density	1	ε^2	$\varepsilon/\alpha_w\alpha_d$

V_{th} roll off

Due to this short channel MOSFETs are hard to turn off. It refers to the decrease in threshold voltage when the channel length decreases below 50 nm as suggested in the literature.

1.4 Motivation

Power consumption is done in two forms that are static and dynamic power consumptions. Dynamic power consumption is somehow advantageous for device but static power consumption is not at all and should be zero ideally. But the reality is that static power holds for 40% of the total power consumption. A desktop computer can tolerate this much but a mobile phone will not be able to sustain and will drain out within few minutes. CPUs are becoming smaller and smaller day by day and this solely depends on the MOSFETs used inside it for switching.

In a normal bulk-silicon, the active elements are situated near the narrow surface layer and are hidden from the silicon body. The formed p-n junction causes the leakage current to flow and rises with rise in temperature and causes various

serious issues. Too much leakage currents and high power dissipation restrict the operation of micro-circuits at large temperatures.

Silicon-on-insulator (SOI) technology utilize a narrow layer of silicon in the range of tens of nanometer which is isolated from the substrate by the wide coating of SiO_2. This technology set apart the constituents in addition with the lateral, diminishes the several parasitic capacitances of the device and in turn it removes the chances of latch-up failures.

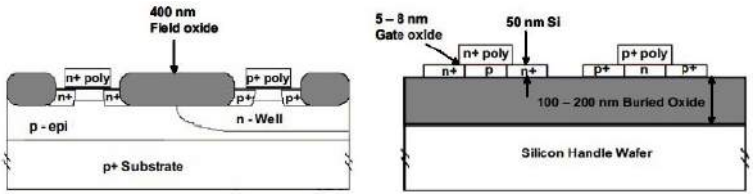


Figure 1.3: Cross-sectional view of the bulk Si (left) and SOI (right) CMOS

Figure 1.3 [6] shows the cross-section of the bulk and SOI MOS devices. As shown in the Figure 1.3 [6], with the addition of buried oxide layer, SOI technology proposes admirable devices with wonderful radiation hardness and high integration density. SOI devices are more appropriate with sharp SS which aids the scaling of the threshold voltage for low-voltage low-power applications. Depending on the thickness of the silicon layer, MOSFETs can be divided into two types of structures; either FD or PD relying upon the thickness of thin silicon layer. When the depletion regime develops over the whole channel of silicon the transistor works in FD otherwise it is in PD. FD is preferred over PD.

Partially depleted SOI has been successfully leveraged for high-performance microprocessors and most other SOI applications for almost a decade. Although OKI has used FD-SOI commercially for a long time, its focus has always been on niche ultra-low power applications. Now, the high-performance world is looking at advanced devices such as ultra-thin body FDSOI MOSFETs and multiple-gate MOSFETs (aka MuGFETs) as potential ways to drastically cut power consumption and leakage while preserving high performance and minimizing short channel effects, probably starting with the 22nm node.

1.5 Research Problem Statement

The salient objectives of the thesis are:

i. To Study of the effects of ultra thin layer of silicon on insulator in single gate and double gate MOSFETs. Introducing the new materials in the channel like GaAs, InGaAs etc. in the aforesaid structures and analyze its effects.

ii. To find the optimum value of underlap length in the DG MOSFET and FinFET so that it can overcome the issues created by short channel effects and made a comparison between the above structures.

iii. To study the role of geometry parameters and Fin aspect ratio of sub 20 nm SOI FinFET in the analog and RF circuit design. Finally the CMOS is made for SG and DG MOSFETs and its VTC characteristics are studied and find out that which one has good NMOS or good PMOS by engineering the work function so that the threshold voltage for both the NMOS and PMOS remains same.

1.6 Thesis Organisation

The dissertation is divided into six chapters and its outline is described as given below:

- Chapter 1: INTRODUCTION

  Crucial ideas connected to technology scaling, Silicon-on-insulator devices and its merits and demerits, research problem of the project and outlines of the thesis.

- Chapter 2: UlTRA THIN Si DIRECTLY ON INSULATOR (SDOI) MOSFETs: SG AND DG

  This chapter explains the buildup of ultra thin silicon directly on insulator (SDOI) single gate (SG) and double gate (DG) MOSFETs and describe the effect of SDOI in diminishing SCEs. NMOS and PMOS models of the aforesaid structures are also made and simulated to analyse which one is better among these and with respect to properties such as I_{on}, I_{off}, SS, V_{th} etc. Then III-V materials are introduced in the NMOS structures of SG and DG to see the effects of these high mobility materials like GaAs, InGaAs etc.

- Chapter 3: OPTIMIZATION OF UNDERLAP LENGTH FOR DG MOSFET AND FINFET

  In this chapter, the role of underlap length is explained in DG MOSFET and FinFET. DG is a 2-D model whereas FinFET is 3-D. The L_{un} is taken symmetric on both sides i.e. on source and drain. Then III-V materials which are high mobility models are introduced in the channel instead of silicon to see the effects on I_{on} etc.

- Chapter 4: ROLE OF FIN ASPECT RATIO IN SILICON-ON-INSULATOR (SOI) FINFET

  This chapter gives the overall emphasis on the role of geometry parameters and aspect ratio of Fin in silicon-on-insulator (SOI) FinFET. Aspect ratio is a very crucial parameter based on which we can divide the structure into three sub-structures as SG, DG and TG MOSFETs. Both DC and AC analysis is done for the aforesaid structures and then an optimum value of width and height of FinFET is found out to make it suitable for RF applications.

- Chapter 5: ANALYSIS OF CMOS DESIGN

  This chapter presents the CMOS design of single gate (SG) and double gate (DG) MOSFETs. The static analysis i.e. voltage transfer characteristics (VTC) is done for both the structures. CMOS is made from the combination of NMOS and PMOS by engineering the work function in order to have same threshold voltage. It analyses which one is having better NMOS or PMOS depending on the VTC characteristics.

- Chapter 6: CONCLUSIONS AND FUTURE SCOPE

Chapter 2

Ultra Thin Si Directly on Insulator (SDOI) MOSFETs: SG and DG

2.1 Introduction

CMOS devices come to nanoscale regime to acquire higher density and low power consumption. The inauspicious effects cause threshold voltage variation with higher leakage current in nano devices known as short channel effects (SCEs). Due to these SCEs the conventional scaling comes to an end, but to maintain the Moore′s law research going towards inventions of novel devices [7–10].

As the natural length of the device is

$$\lambda = \sqrt{\frac{\varepsilon_{\mathrm{si}} \mathrm{t_{si}} \mathrm{t_{ox}}}{\mathrm{n}\varepsilon_{\mathrm{ox}}}} \tag{2.1}$$

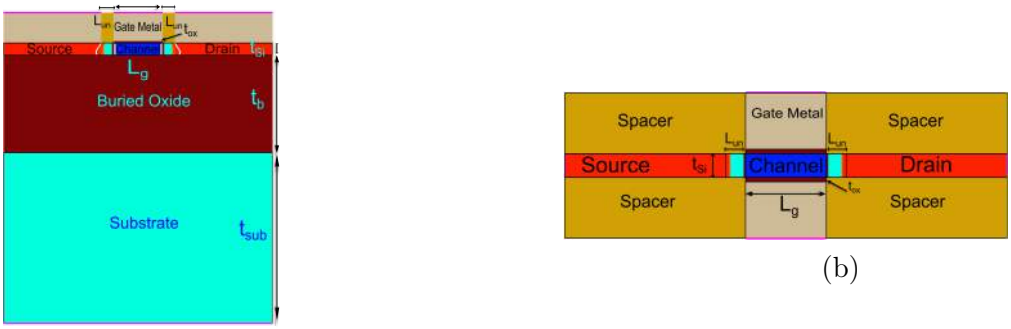
, where n reflects the number of gates, ε_{Si} permittivity of Si, ε_{ox} permittivity of oxide, t_{Si} and t_{ox} thickness of Si body and oxide. 'λ' is the measure of SCEs and it should be as small as possible to minimize the SCEs. So, one of the ways to control the above said SCEs is by using more than two gates and a lean fully depleted (FD) semiconductor body. The predictions of International Technology Roadmap for Semiconductors (ITRS) are followed by the device designers to propose various novel device structures and process parameter variations [3]. Advanced nano MOS schema′s, such as Ultra-Thin Body (UTB), are replacing the conventional bulk MOS devices because of their capability to reduce SCEs and attain higher speed with the added advantage to design highly integrated CMOS circuits [11–15].

Again UTB double gate (DG) MOSFET can be scaled more intrusively than bulk Si schema [5, 16, 17]. A double gate structure fabricated on SOI wafer has been employed in CMOS technology because of its outstanding SCEs immunity, high current drivability (I_{on}) and lower leakage current (I_{off}) as compared to the bulk MOSFETs [18].

This research presents the simulation of short-channel UT-SDOI model for single gate, Double-Gate (DG) MOSFETs and FinFETs. The simulation results from Sentaurus are utilized to verify the obtained model. In continuation with the section I as Introduction, the section II depicts the device structures description and the simulation settings of UT-SDOI MOSFETs. Section III presents the structures and comparison between DG MOSFET and FinFETs for optimization of underlap length. Section IV presents the simulation and role of fin aspect ratio in FinFET. Section V presents the performance related to SCEs for CMOS digital application. At the end a concluding remark provided in section VI about he UTB-MOSFETs.

2.2 Device Structure and Its Parameters

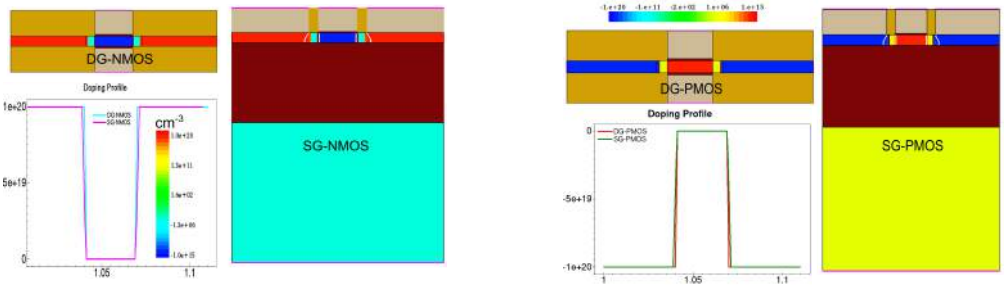
The schematic diagram of the UT-SDOI SG and DG MOSFET structures are used for modeling and simulation as shown in Fig. 2.1. The thickness of buried oxide and gate oxide and of silicon are t_b = 40 nm, t_{ox} = 0.9 nm and t_{Si} = 5 nm, respectively. The gate length L_g= 20 nm, with underlap L_{un}=5 nm considered towards both side of channel. The source drain length fixed at L_{sd}=40 nm. For all structures, the WF of the metal gate is defined between ϕ_M = 4.6 eV to 4.7 eV to achieve a constant leakage current I_{off} =0.15 nA. The structures have evenly doped with N_D value of $1{\times}10^{20}$ cm^{-3} in the source and drain regimes. Si channel is delicately doped with Na value of $1{\times}10^{15}$ cm^{-3} which we can call as undoped



(a) (b)

Figure 2.1: Illustrative Architecture of UT-SDOI (a) SG and (b) DG, SDOI MOSFETs

also. The underlap region kept as intrinsic Si. The underlap regime is left intrinsic which is of silicon material.



(a) (b)

Figure 2.2: Doping profile of the UT-SDOI MOSFET structures (a) Single and Double Gate NMOS (b) Single and Double Gate PMOS.

The doping profile for both nmos and pmos are demonstrated in Fig. 2.2. The simulations are brought out by the TCAD Sentaurus, a device simulator, a 2-D and 3-D numerical simulator which is provided by Synopsys company [19]. The cut line is captured in the middle of silicon channel by using the precision cut in order to analyze the potential in the silicon channel.

2.3 Simulation

In this chapter, TCAD Sentaurus (Synopsys) software is used for device simulation. The electrical output characteristics of the aforesaid device are carried out by this software. Numerical simulations are brought out using TCAD Senaturus provided by Synopsys. The activated model for the charge carriers transport is the drift-diffusion model in Sdevice of Sentaurus. For mobility, basic model is taken, that includes the impact of high-field velocity saturation, dependency of the dopings and of transverse field. For the calculation of intrinsic carrier concentration, Si band gap narrowing model is actuated. An iterative approach is followed to solve the device equations. The iteration continues, till it attains a small enough error limit. This is helpful to determine self-consistent solutions on a discrete mesh. Others incorporated equations are Poisson, continuity, distinct

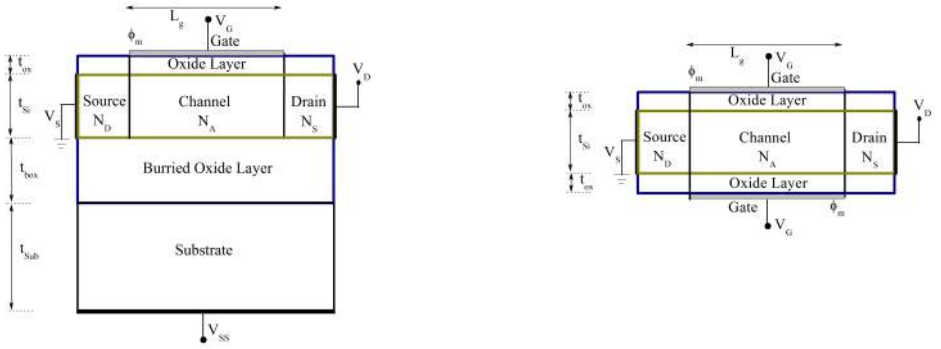
thermal and energy equations. All the structure junctures are assumed abrupt, and the supply requirements are employed at 25 degree celsius during simulation.

2.4 III-V Channel Materials

Channel materials like GaAs, $In_{0.53}Ga_{0.47}As$ etc. formed by the combination of IIIrd and Vth groups of periodic table are introduced in the DG MOSFET instead of silicon and its effects are seen by comparing it with the planar Si-based channel MOSFET. UTB DG-MOSFET has been considered which is planar symmetric one and whose illustrative architecture is presented in Fig. 2.3. Si channel thickness is taken one fourth of the gate length for better control of the transistor [8]. So, t_{Si} is taken as 5 nm. Enlargement of source and drain regimes is 60 nm and metal contacts are established over them. The length of the channel of the device is varied in sub 100 nm. All the structure junctions are abrupt.

Table 2.1: Device Parameters Used in the TCAD Simulation.

Design	HP	LOP	LSTP	This Work	
				UTB SG-MOS	UTB DG-MOS
L_g (nm)	20	20	20	100 nm to 20 nm	
EOT (nm), tox	0.84	0.9	1.2	0.9 nm	
V_{DD} (V)	0.85	0.67	0.87	0.7 V	

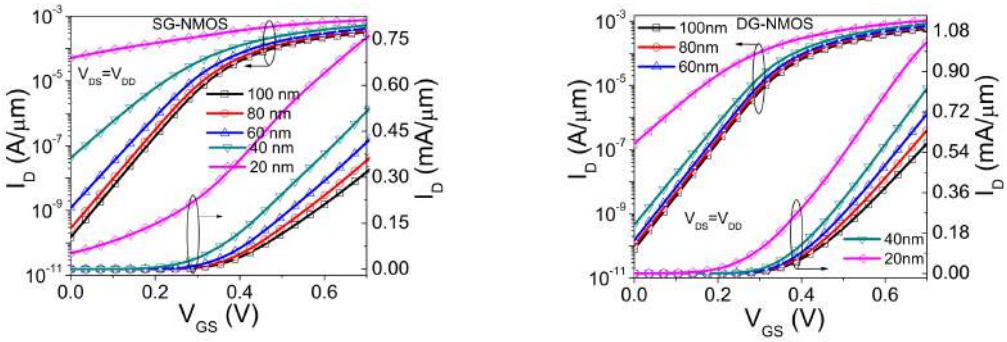


(a) (b)

Figure 2.3: 2-dimensional cross sectional view of the (a) UTB SG (b) UTB DG, MOSFETs.

2.5 Results and Discussion

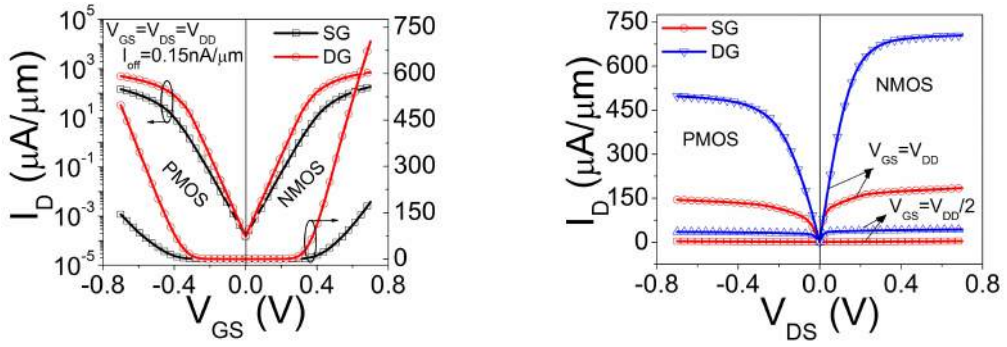
In Fig. 2.4, similar analysis are carried out as previously discussed in Fig. 2.2 at a higher drain bias of V_{DS}=0.7 V to study the effect of V_{DS} on device efficiency. From Fig. 2.4(a) and 2.4(b), the I_{off} is very low in terms of 10^{-7} A/μm in case of DG as compare to SG (I_{off} in terms of 10^{-4} A/μm). So, V_{DS} has a less influence on DG configuration as compare to SG which further decreases the drain induced barrier lowering (DIBL) effect.



(a) (b)

Figure 2.4: Drain current (I_D) of the devices as a part of V_{GS} at V_{DS}= V_{DD} (a) SG, with variation of L_g (b) DG with variation of L_g.

The I_D-V_{GS} characteristics of a CMOS with 5 nm body portliness and 20 nm gate length are shown in Fig. 2.5(a). As shown in the figure, the I_D-V_{GS} have matched I_{off} and V_{th} as centered for both NMOS and PMOS devices, which are achieved by tuning the metal gate work function. Also by observing the Fig. 2.5(b), having constant I_{off}, the UT-SDOI DG shows a higher drive current than it's counterpart UT-SDOI SG. Typical output characteristics of both NMOS and PMOS, UT-SDOI SG and DG devices are demonstrated in Fig. 2.5(b) and report as a fully functional and long channel behavior. Furthermore, one can clearly say that these devices are fully depleted (FD) as there is no kink effect. Because of high electron mobility, the NMOS shows a higher current than PMOS. Again by comparing between UT-SDOI SG and DG devices, the DG configuration depicts a 30% more in drain current than SG configuration.

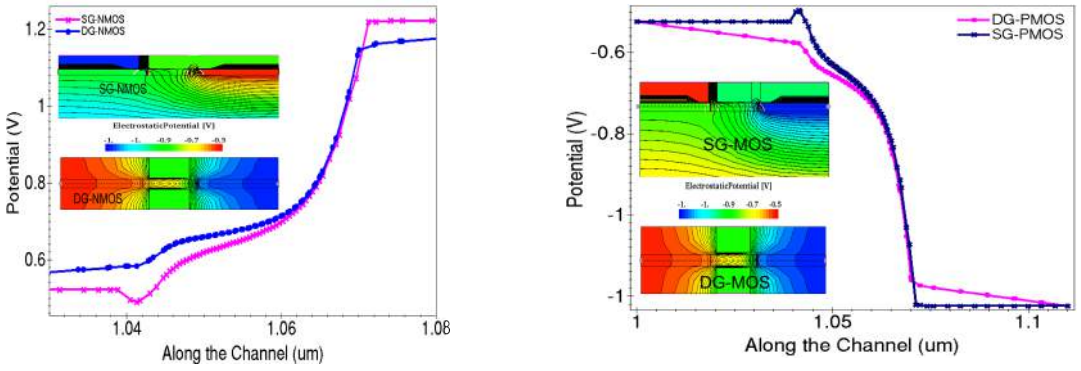


(a) (b)

Figure 2.5: The characteristics of both UT-SDOI SG and DG MOSFETs (n and p type) for V_{GS}=0.7 V, and V_{GS}=0.35 V having same I_{off}=0.15 nA, (a) The transfer curve between I_D and V_{GS} (b) The output curve between I_D and V_{DS}.

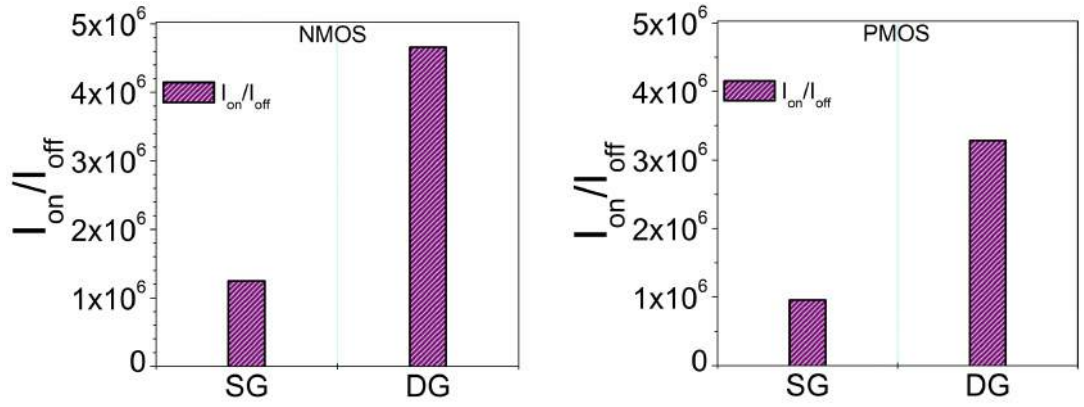
The channel potential distributions for both NMOS and PMOS, UT-SDOI SG and DG devices are demonstrated in Fig. 2.6(a) and 2.6(b) respectively. The inset figures represent field distribution of devices. From the graph, the potential barrier height of DG is little lower than SG which leads to a lower threshold voltage for DG MOSFETs. A lower threshold voltage with acceptable SCEs is very much useful for high performance (HP) applications according to ITRS-2011. So, double gate ultra-thin body i.e. t_{Si}= 5nm MOSFET is a good candidate for

HP applications.



(a) (b)

Figure 2.6: Potential fluctuation over the channel length at V_{GS}=V_{DS}=0.7 V for UT-SDOI SG and DG MOSFET (a) NMOS devices (b) PMOS devices.

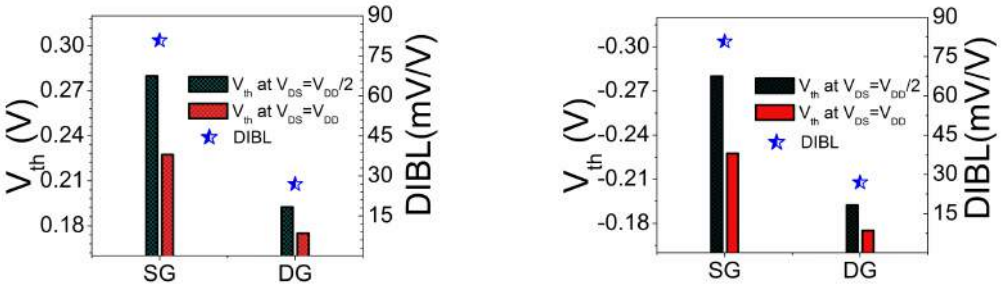


(a) (b)

Figure 2.7: I_{on}/I_{off} ratio of UT-SDOI SG and DG MOSFET (a) NMOS devices (b) PMOS devices.

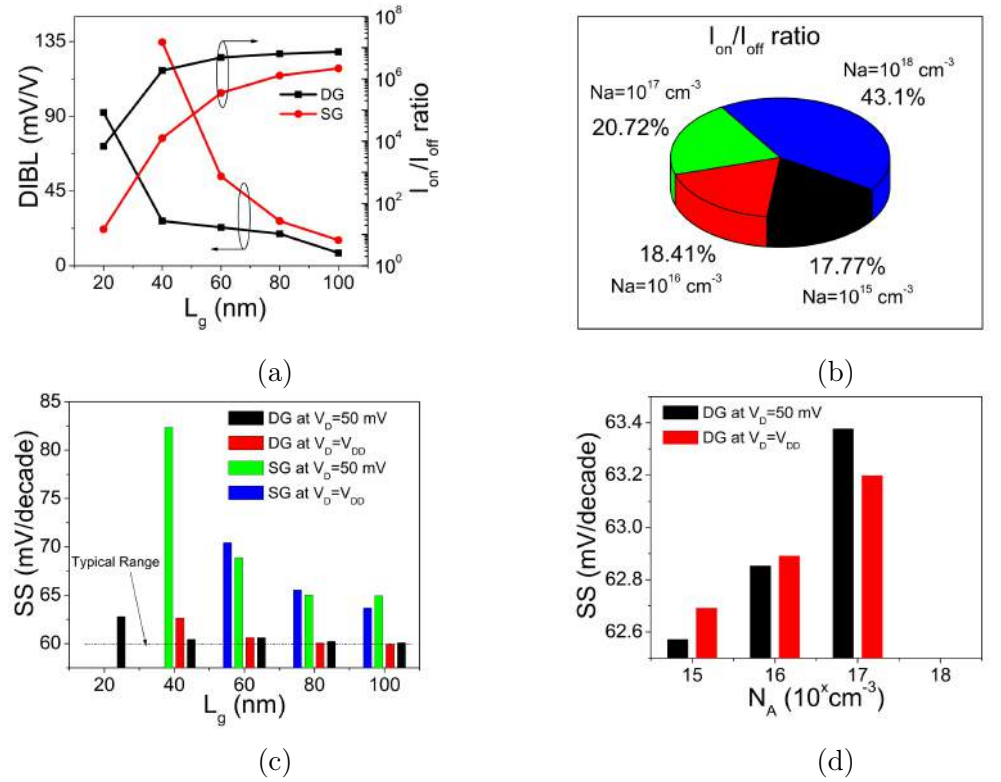
Fig. 2.7 illustrates the on-off ratio for both NMOS and PMOS, UT-SDOI SG and DG devices. SDOI DG devices endow more on current than SG device, emerging in a rapid switching time. It can be measured from the figure that for SDOI DG, on-off ratio increases around a factor of 4 than SDOI SG in case of NMOS and a factor of 3 in case of PMOS. SG devices have several leakage mechanisms like BTBT, GIDL, leakage under threshold, gate leakage, and reverse bias junction [15], [5]. However, DG devices have two crucial leakages as leakage under threshold and leakage of gate [8]. The increase of drain current of SDOI DG is because of the lack in parasitic source-drain resistances.

DIBL and V_{th} are compared between UT-SDOI SG and DG MOSFETs in Fig. 2.8(a) and 2.8(b). As thinner body thickness (t_{Si}), and number of gates are more in case of UT-SDOI DG, owing a low value of natural length (λ) which is desirable to minimize the SCEs. So, the V_{th} is less sensitive to V_{DD} in case of UT-SDOI DG MOSFET than it's SG counterpart, further leads to a less DIBL effect.



(a) (b)

Figure 2.8: Two important SCEs, V_{th} variation and DIBL of UT-SDOI SG and DG MOSFET (a) NMOS devices (b) PMOS devices.



(a) (b)

(c) (d)

Figure 2.9: The performance metrices for both SG and DG MOSFETs at V_{DS}=0.05 V and V_{DD} (a) DIBL and I_{on}/I_{off} ratio for different L_g (b) I_{on}/I_{off} ratio of DG with variation of N_A (c) SS for different L_g (d) SS with variation of N_A.

Fig. 2.9(a) describes the L_g dependence of DIBL and I_{on}/I_{off} ratio for both UTB SG and DG devices. The DIBL increases as the channel length lessens due to the V_{th} roll off effect in shorter L_g. It can also be measured from Fig. 2.8(a), the DIBL is very low in case of DG as compare to SG. This is because of the less influence of V_{DS} on DG configurations as already discussed in Fig. 2.7(b). So, it identifies that the electrostatic control of gate is more in case of DG device. The on-off ratio (I_{on}/I_{off}) is also discussed for both devices with different L_g. DG configuration shows a 13% of higher I_{on}/I_{off} ratio as compare to SG device. Higher I_{on}/I_{off} ratio is by the virtue of lower leakage current and more gate control of the DG device. Fig. 2.9(b) shows the percentage of I_{on}/I_{off} ratio

for UTB-DG MOSFET with different doping profiles. For low stand by power applications (LSTP), this ratio has a significant impact and higher value of this ratio is desirable. From Fig. 2.9(b), I_{on}/I_{off} ratio increases in accordance with the doping concentrations.

This is because higher doping concentration is necessary to control the V_{th} and minimize the SCEs which further decreases the leakage current. So, a maximum 43.1% I_{on}/I_{off} ratio can be achievable in case of doping profile of N_A=10^{18} cm^{-3}. The subthreshold slope (SS) variation with L_g for both the devices at two different drain biases (V_{DS}=50 mV, and 0.7 V) is plotted in Fig. 2.9(c). SS can be calculated as SS= $\Delta V_G/\Delta(\log I_D)$ and the typical value is 60 mV/decade as marked in Fig. 2.9(c). As per the result, for higher L_g (100 nm, 80 nm, and 60 nm) the SS shows approximately ideal value for both device cases. However, as L_g decreases (40 nm, and 20 nm) the SG configuration demonstrates a higher SS value as compare to DG.

This is because SG configuration is more prominent towards SCEs for lower L_g and the gate loses its control over channel. Similarly Fig. 2.9(d) shows the SS values for DG device at different doping profiles. Lower doping profiles give a better SS value for DG configuration and increases with doping concentrations.

Table 2.2: Static Electrical FoMs for SG-MOSFET

SG-MOS	Threshold Voltage V_{th} (V)		DIBL	I_{on}, (A)	I_{off}, (A) V_{GS}=0V	SS (mV/decade)	
L_g (nm)	V_{DS}=0.05 V	V_{DS}=0.7 V		V_{DS}= V_{GS}=0.7V	V_{DS}=0.7V	V_{DS}=0.05V	V_{DS}=0.7V
100	0.19	0.18	15	3.25×10^{-4}	1.49×10^{-10}	64.96	63.67
80	0.19	0.17	27	3.63×10^{-4}	2.83×10^{-10}	65.03	65.54
60	0.17	0.14	54	4.23×10^{-4}	1.19×10^{-9}	68.89	70.42
40	0.12	0.03	135	5.25×10^{-4}	4.20×10^{-8}	82.35	-
20	-	-	-	7.62×10^{-4}	5.15×10^{-5}	-	-

All the above discussed parameters are extracted for both devices and tabulated in Table 2.2, 2.3 and 2.5. By comparing the data from both tables, we can say the UTB-DG configuration shows a better results in terms of SS, DIBL, and I_{off}.

Table 2.3: Static Electrical FoMs for DG-MOSFET

DG-MOS	Threshold Voltage		DIBL	I_{on}, (A)	I_{off}, (A) V_{GS}=0V	SS (mV/decade)	
	V_{th} (V)						
L_g (nm)	V_{DS}=0.05 V	V_{DS}=0.7 V		V_{DS}= V_{GS}=0.7V	V_{DS}=0.7V	V_{DS}=0.05V	V_{DS}=0.7V
100	0.19	0.18	8	5.80×10^{-4}	7.77×10^{-11}	60.08	59.92
80	0.19	0.18	19	6.38×10^{-4}	9.97×10^{-11}	60.23	60.05
60	0.17	0.16	23	7.11×10^{-4}	1.46×10^{-10}	60.61	60.61
40	0.17	0.15	27	8.24×10^{-4}	4.41×10^{-10}	60.42	62.65
20	0.07	0.01	92	1.03×10^{-3}	1.49×10^{-7}	62.78	-

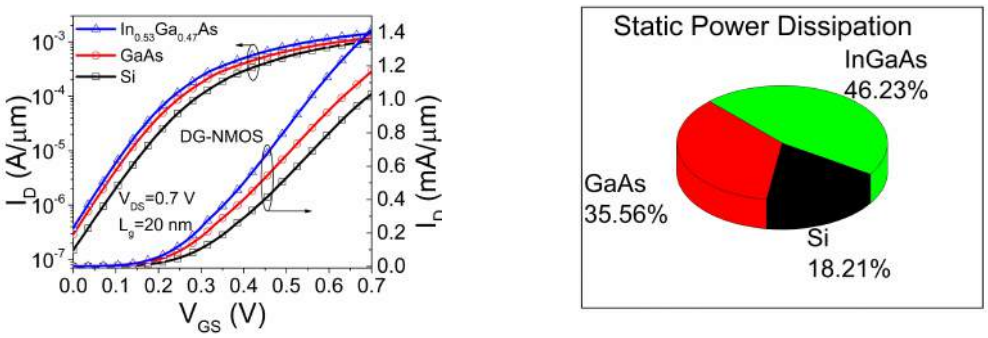
2.5.1 Effects of high mobility channel materials

It is widely anticipated that Stained-Si may be cleaned out and other possible choice channel materials will be needed to instate the goals set decided by ITRS [3].

Although various great challenges must be chasten to carry out III-V N-MOSFETs inclusion in forthcoming C-MOSFETs. High mobility (low-bandgap) materials like GaAs, $In_{0.53}Ga_{0.47}As$ which are the combination of elements of III and V columns of periodic table show a significant amount of augmentation in on current but endure from the BTBT leakage current i.e. off current. These materials are the alternatives to reach to the predicted performance of the CMOS technology.

Table 2.4: Material Parameters Used in DG-MOSFET for the Simulation

Material Parameters	Si	GaAs	$In_{0.53}Ga_{0.47}As$
E_G (eV)	1.12	1.424	0.751
ε_r	11.7	12.9	13.9
μ $(cm^2V^{-1}s^{-1})$	200	500	1300
n_i (cm^{-3})	1.15×10^{10}	2.15×10^{6}	6.37×10^{11}



(a) (b)

Figure 2.10: Effects of high mobility channel materials for DG MOSFET at V_{DS}=0.05 and V_{DD} using different materials (a) Drain current variation for saturation region (b) Static power dissipation pie chart.

Table 2.5: Performance Comparison of DG-MOSFET by Considering Different Channel Materials

DG-MOS at L_g=20nm	Threshold Voltage, V_{th} (V)		DIBL	I_{on}, (A)	I_{off}, (A) V_{GS}=0V	SS (mV/decade)	
	V_{DS}=0.05 V	V_{DS}=0.7 V		V_{DS}= V_{GS}=0.7V	V_{DS}=0.7V	V_{DS}=0.05V	V_{DS}=0.7V
Si	0.07	0.01	92	1.03×10^{-3}	1.49×10^{-7}	62.78	-
GaAs	0.285	0.25	53.84	1.16×10^{-3}	2.91×10^{-7}	79.18	79.042
$In_{0.53}Ga_{0.47}As$	0.281	0.251	46.15	1.41×10^{-3}	3.79×10^{-7}	78.98	78.84

Fig. 2.10(a) shows that drain current is maximum for the InGaAs due to its high mobility at V_{DS}=0.7 V. But the static power dissipation is more in high mobility materials due to the high leakage currents as shown in Fig. 2.10(b) which can be compensated with the high drain current particularly for the switching applications.

2.6 Summary

The sensitivity and trend of V_{th}, I_{on}/I_{off} ratio and potential of UT-SDOI SG and DG MOSFET for both P-type and N-type cases are established through proper simulation setup. The device dimensions are considered in the work are according to ITRS-2011 roadmap. The designs are valid for all three types of applications like HP, low operating power, and LSTP. From the results, the UT-SDOI DG shows a higher drive current and lower DIBL than it's counterpart UT-SDOI SG even maintaining a constant I_{off}. The on-off current ratio for SDOI DG increases around a factor of 4 than SDOI SG in case of NMOS and a factor of 3 in case of PMOS case. From all analysis UT-SDOI DG MOSFET has potential to meet the ITRS roadmap for 22nm technology generation and below this node with considerable amount of design adaptability for HP and LOP devices are achievable. However, LSTP design specification may be feasible by considering a scaled version of oxide thickness.

With the use of GaAs, $In_{0.53}Ga_{0.47}$As in DG MOSFET, we have found that a decline of DIBL in GaAs and $In_{0.53}Ga_{0.47}$As. Our result shows that $In_{0.53}Ga_{0.47}$As based DG MOSFETs have the lower DIBL, but greatly affected by quantum confinement trappings. So by comparing these parameters, DG MOSFET with high mobility materials exhibits high drive current which is more suitable for better switching application.

Chapter 3

Optimization of Underlap Length for DG MOSFET and FinFET

3.1 Introduction

Scaling of planar transistors has sustained to determine efficiency, potential, and integration density of circuit progress up to the 22 nm process generation. Despite the fact, deedful pioneering on FinFET devices have continuing from the last ten years, A production fabrication laboratory has freshly adopted the use of these.

As scaling into sub-micron region, Short Channel effects inhibit further scaling like DIBL, threshold voltage roll off etc. occurs in single gate MOSFET. FinFET is the prime candidate which have excellent control over channel in sub-micron region and making transistors still scalable. In order to overcome SCEs and leakage current, different device Multigate MOSFETs (Mug-FET) structures like Double gate, Tri gate, FinFET were proposed [20] [21].

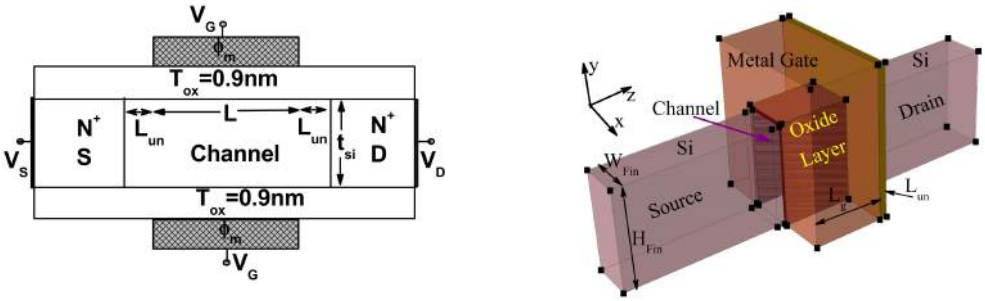
The transistor channel width of one FinFET is outlined by the fin width W_{Fin} and fin height H_{Fin}. In many cases, especially when H_{Fin} is at least twice W_{Fin}, the FinFET can be considered a DG transistor where the channel width can be considered H_{Fin}+$W_{Fin}/2$, and for this reason, the rise of FinFET models is related to the evolution of DG models. The fabrication process of these bulk FinFETs is reported to be compatible with standard CMOS technology [20].

The advantages of Mug-FETs are increased current of drain and switching speed, dynamic power is also reduced to half with static leakage current of 90% less. DG MOSFET manufactured on Silicon-on-insulator wafers is one of the best encouraging contender due to its attractive features of high current drivability, transconductance, reduced SCEs [8]. Similarly, FinFETs also acquired attentions because of their low cost process steps and compatibility with CMOS technology [22] [11]. The transistor performance depends on the process induced variations categorized under systematic values of gate length L_g, underlap gate length L_{un}, gate oxide thickness t_{ox}, etc. [23].

The main purpose of this work is to study the sensitivity of L_{un} on various performance metrics of both DG MOSFET and FinFET for further scalability of the device. A systematic analysis is carried out among DG and FinFET.

3.2 Device Structure

The DG MOSFET and 3-D SOI-FinFET designs simulated in the indicated task are shown in Fig. 3.1(a) and 3.1(b) respectively. An n-channel MOSFET having SiO_2 as interfacial oxide with high-k material (Si_3N_4) as spacer in the underlap regions is modeled. The spacer is used to reduce the R_s and R_d. The channel length (L_g) is considered as 20 nm for both devices. The Source/Drain length (L_S/L_D) are taken to be 40 nm, and doping, N_D is homogeneous with a value of 5×10^{19} cm^{-3}. EOT is 0.9 nm [24] and V_{DD} is 0.7 V. The work function for the metal gate electrode is tuned between 4.5 eV to 4.7 eV to achieve a constant threshold voltage for both device cases. The channel is lightly doped (10^{15} cm^{-3}) i.e. undoped channel which boosts the mobility of the carriers and thus the I_{on} density from the source. The underlap length, L_{un} is varied from 0 nm to 15 nm to analyze the parameter dependency. Supply voltages and parameters employed in the simulations are with respect to ITRS for under 50 nm gate length devices.



(a) (b)

Figure 3.1: Cross sectional view of (a) DG; (b) FinFET

3.3 Simulation

The effectiveness of the simulator has been checked by examining its outcomes with past literature data [25]. The activated model for the charge carriers transport is the drift-diffusion model in Sdevice of Sentaurus. The mobility model with definition of band gap is included [26]. The inversion layer mobility models CVT (Lombardi), along with SRH and Auger recombination models are reckoned.

3.4 III-V Channel Materials In FinFET

The 3-D GaAs on insulator FinFET design simulated in the indicated task is displayed in Fig. 3.2. An n-channel MOSFET having interfacial oxide as SiO_2 with

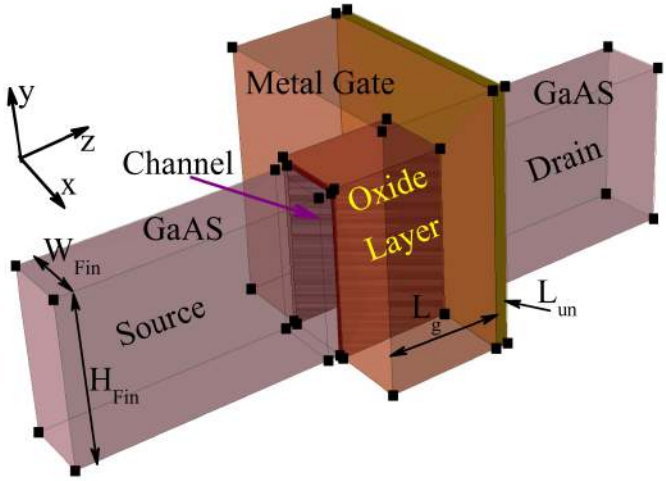


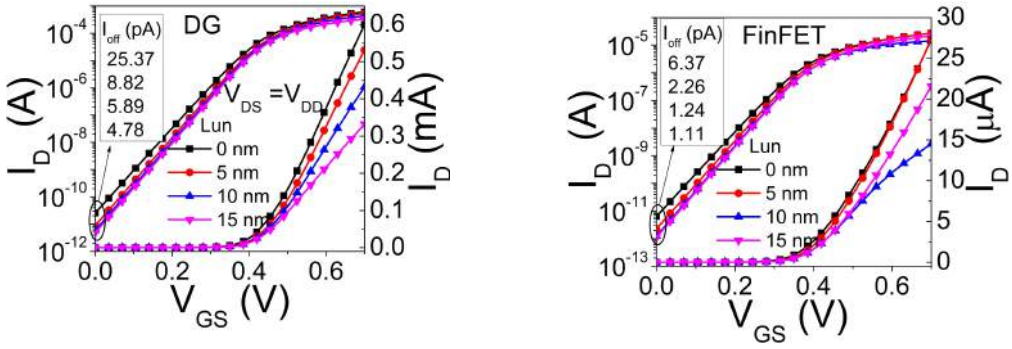
Figure 3.2: Cross sectional view of GaAs FinFET

Si_3N_4 as spacer in the underlap regimes is modeled. The channel length (L_g) is considered as 20 nm. The L_S/L_D as 40 nm, and doping, N_d, is homogeneous with a value of 5×10^{19} cm^{-3}. EOT is 0.9 nm and V_{DD} is 0.7 V. The work function for the metal gate is fixed as 4.5 eV. The channel is undoped which boosts the mobility of the carriers and thus the I_{on} density from the source. The channel to source

and channel to drain underlap region L_{un} is 5 nm. The H_{Fin} and W_{Fin} are varied from 5 nm to 26 nm and 5 nm to 20 nm respectively to investigate the parameter dependency. Supply voltages and parameters employed in the simulations are with respect to ITRS [11] for under 50 nm gate length devices.

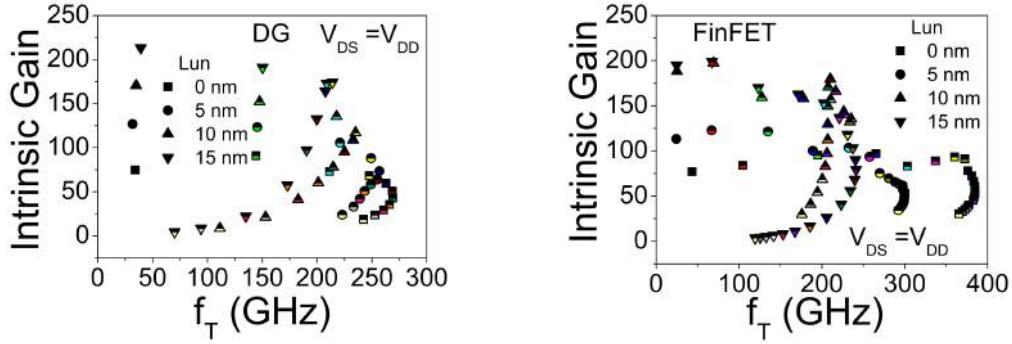
3.5 Results And Discussion

In this work, we have considered a symmetrical underlap region, L_{un} for both DG MOSFET and FinFET. With an increase in L_{un}, the source to drain coupling significantly reduces, which further reduces the subthreshold leakage current. The I_D-V_{GS} characteristic with different L_{un} for DG and FinFET are plotted in Fig. 3.3(a) and 3.3(b) respectively. The I_{off} is significantly reduced with increase in L_{un}, which can be observed from the inset values of Fig. 3.3. If we make a comparison between Fig. 3.3(a) and 3.3(b) i.e. among DG and FinFET, then the first one shows a high drive current while the later predicts very low leakage.



(a) (b)

Figure 3.3: I_D as a part of V_{GS} for V_{DS}=V_{DD} with variation of L_{un} (a) DG; (b) FinFET.

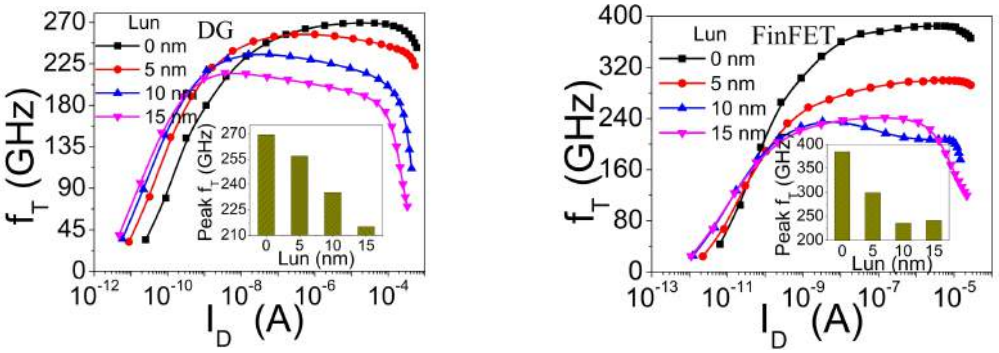


(a) (b)

Figure 3.4: Dependency of Intrinsic Gain (A_V) on cutoff frequency (f_T) for V_{DS}=V_{DD} with variation of L_{un} (a) DG; (b) FinFET

Fig. 3.4 describes the dependency of intrinsic gain (A_V) on cutoff frequency (f_T) with a variation of L_{un} for DG and FinFET. From the figure it can be observed that A_V increases with the increase in L_{un}. The f_T dependency on I_D with variation of L_{un} ranging from 0 to 15 nm for DG and FinFET is given in Fig. 3.5. We can observe that f_T (f_T=$g_m/2\pi C_{gg}$) increases rapidly with increase in I_D

because higher I_D generates a larger transconductance, g_m. From the inset of Fig. 3.5, FinFET predicts a higher f_T value as compared to DG. Fig. 3.6 discussed various important performance metrics like energy delay product (EDP=CV^2*CV/I), I_{on}/I_{off}, subthreshold swing (SS) and energy (E=CV^2) for different L_{un} of DG and FinFET devices. The I_{on}/I_{off} and SS are improved sufficiently with increase in L_{un}. This is due to the reduction in source drain coupling as L_{un} increases which in results decrease the off state current and SS. However, there is a degradation which is observed in case of EDP and E with the increase in L_{un}. So, it is very important to choose L_{un} to fit the energy requirements.



(a) (b)

Figure 3.5: Dependency of cut-off frequency (f_T) on drain current for V_{DS}=V_{DD} with variation of L_{un} (a) DG; (b) FinFET.

From the same analysis, DG MOSFET gives a higher I_{on}/I_{off} ratio and lower SS, while FinFET demonstrates an improvement in EDP and E. Similarly, Fig. 3.8 describes about intrinsic source drain inductance (L_{SD}), power dissipation (PD=$V_{DD}I_{off}$) and intrinsic delay ($(C_{gg}\times V_{DD})/I_{eff}$) with a variation of L_{un} ranging from 0 to 15 nm. An improvement in P.D. but degradation in intrinsic delay can be observed for higher L_{un}. Thus, it is needed to be careful while choosing L_{un} for both device cases. FinFET demonstrates better results in case of L_{SD}, P.D. and intrinsic delay over DG MOSFET. This is because FinFET design has an optimum control on the channel which shows better immunization capability towards short channel effects (SCEs). The extracted values for all above said parameters are tabulated and compared for different L_{un} values for DG and FinFET in Table 3.1. There is an improvement in I_{on}/I_{off}, SS, L_{SD} and P.D. can be observed with increase in L_{un}. However, degradation occurred in case of intrinsic delay, EDP, Q-factor and g_m for higher L_{un}. Among DG and FinFET, the prior one gives higher current drivability, while the later one shows an improvement in EDP and delay.

Here a unique attempt has been made to present deep analysis of process variability dependency on various performance metrics of the GaAs-FinFET. According to the literature, access resistance problem is more serious in FinFETs. However, some solutions are available like increasing the H_{Fin} out of the gate region [11]. The parasitic resistance problem can be avoided by using higher H_{Fin}/L_g ratio which further increases the drain current. The I_D-V_{GS} characteristics with different H_{Fin} and W_{Fin} for GaAs-FinFET are plotted in Fig. 3.8(a) and 3.8(b) respectively.

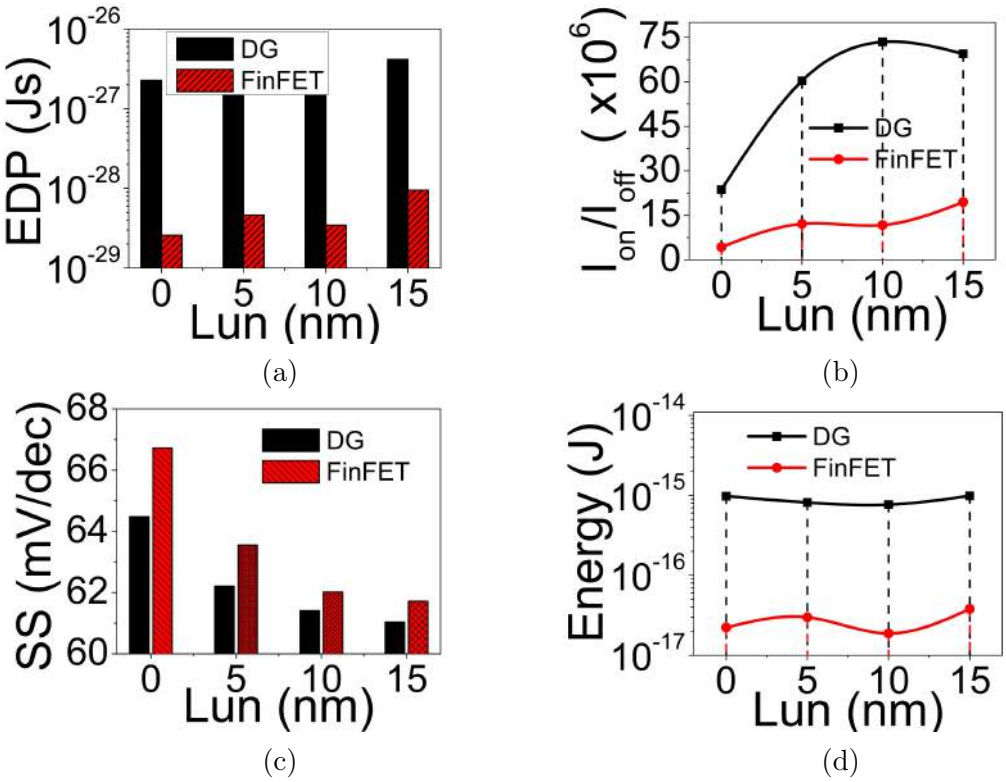


Figure 3.6: Dependency of various performance parameters on under lap length (L_{un}) of DG MOSFET and FinFET at V_{DS}=V_{DD} (a) Energy Delay Product (EDP); (b) on-off ratio (I_{on}/I_{off}); (c) subthreshold swing (SS); (d) Energy.

Table 3.1: Various Performance Comparison between DG and FinFET

	L_{un}	Delay (CV/I), (ps)	Energy (CV^2) (J), $\times10^{-16}$	EDP (Js), $\times10^{-27}$	Inductance, L_{sd} (H) (Delay/g_{ds}), $\times10^{-8}$	I_{on}/I_{off} $\times10^7$	PD (I_{off}*V_{DD}), (pW)	SS (mV/decade)	V_{th} (V)	$g_{m,max}$ (mS)	Q-factor ($g_{m,max}$/SS)
DG	0	2.32	9.75	2.26	1.422	2.364	17.76	64.48	0.43	3.099	48.07
	5		8.13	1.77	2.245	6.034	6.17	62.21	0.44	2.387	38.38
	10	2.52	7.64	1.93	1.979	7.342	4.12	61.41	0.43	1.695	27.6
	15	4.24	9.86	4.18	2.124	6.943	3.34	61.03	0.42	1.224	20.05
FinFET	0	1.16	0.22	0.025	33.99	0.428	4.455	66.73	0.43	0	1
	5	1.55	0.29	0.046	47.89	1.212	1.583	63.55	0.44	0.114	1
	10	1.84	1.87	0	129.6	1	0.865	62.02	0	0.053	0.869
	15	2.51	3.79	0.095	160.8	1.947	0.776	61.72	0.43	0.081	1.325

The I_{off} is significantly reduced with decrease in H_{Fin} and W_{Fin}, which can be observed from the inset values of Fig. 3.8. This is because narrow fins cause the decrease of electric field in the silicon region which minimizes the leakage current. Fig. 3.9(a) and 3.9(b) describe the variation of subthreshold slope (SS) and V_{th} with H_{Fin} and W_{Fin}. This analysis allows to figure out the trade off among I_{off} with an optimized V_{th}.

It is more decisive to fix the value of H_{Fin} for proper operation with a better immunity towards short channel effects (SCEs). From Fig. 3.9(a), V_{th} decreases as H_{Fin}/L_g ratio increase leads to higher V_{th} roll-off and subthreshold slope for high H_{Fin} values. The V_{th} is extracted from I_D-V_{GS} curve and plotted in Fig. 3.9(b) by varying W_{Fin}/L_g ratio ranging from 0.2 to 1.0. V_{th} value decreases with increase

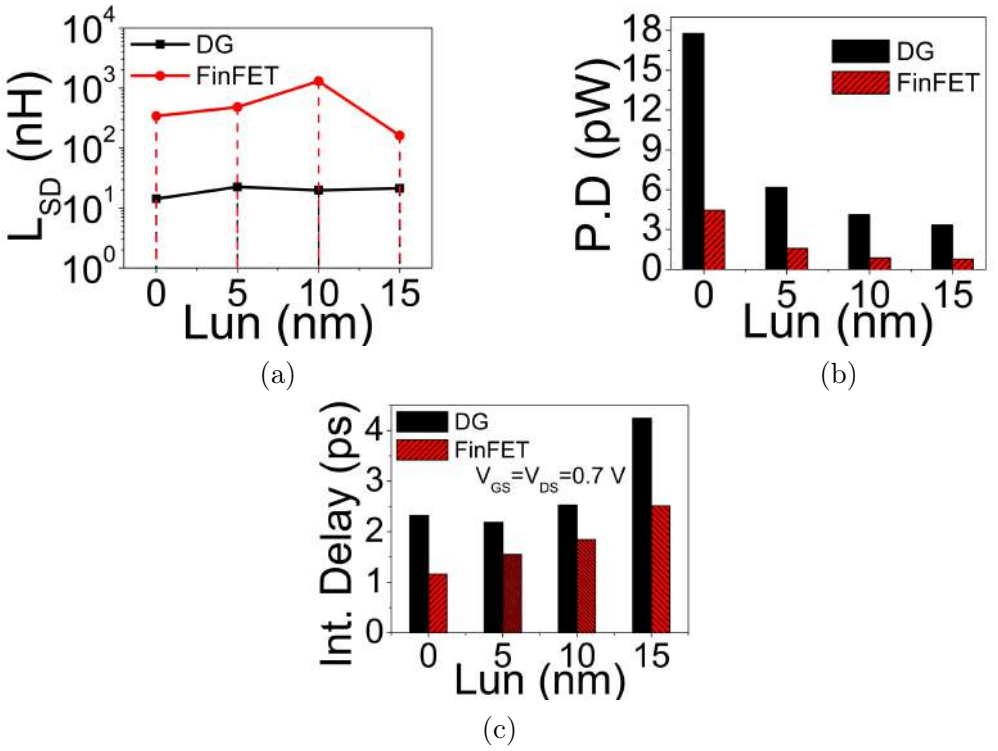


Figure 3.7: Dependency of various performance parameters on under lap length (L_{un}) of DG MOSFET and FinFET at V_{DS}=V_{DD} (a) Intrinsic source drain inductance (L_{SD}); (b) Power Dissipation (P.D.); (c) Intrinsic Delay.

in W_{Fin}/L_g ratio which will further degrades the device performance because of the SCEs like DIBL, V_{th} roll-off and CLM. The dependency of intrinsic gain (A_V) on cutoff frequency (f_T) with a variation H_{Fin} and W_{Fin} for GaAs-FinFET is discussed in Fig. 3.10(a) and 3.10(b). From the figure, a decrement in H_{Fin} and W_{Fin} will depict a higher A_V. Fig. 3.10(b) shows the intrinsic gain (A_V) of the device against V_{GS} with a variation of W_{Fin}/L_g ranging from 0.25 to 1.0 at $V_{DD}/2$. A higher gain can be observed for the FinFETs having lower fin widths is because of the fully depletion of fins, which reduces the output conductance.

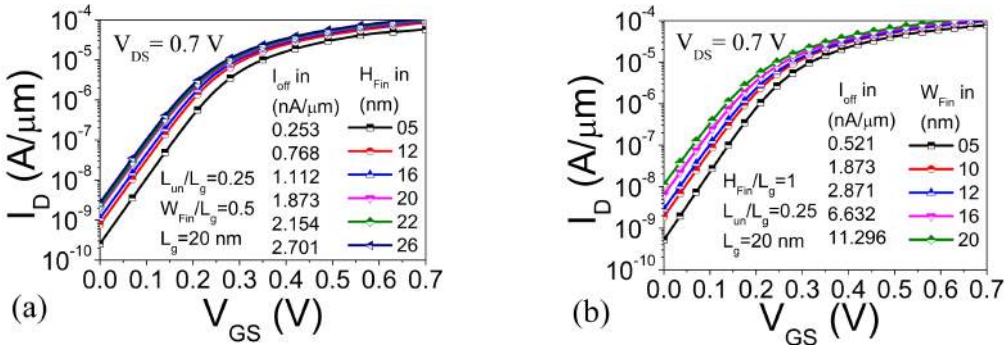


Figure 3.8: I_D-V_{GS} with variation of (a) H_{Fin}; (b) W_{Fin}.

Fig. 3.11(a) and 3.11(b) describe about important performance metrics like energy delay product (EDP=CV^2*CV/I) and intrinsic delay ($(C_{gg}*V_{DD})/I_{eff}$) with a variation of H_{Fin} and W_{Fin}. There is an improvement can be observed in case of intrinsic delay with the increase in H_{Fin}. The trade-off between I_{off} and

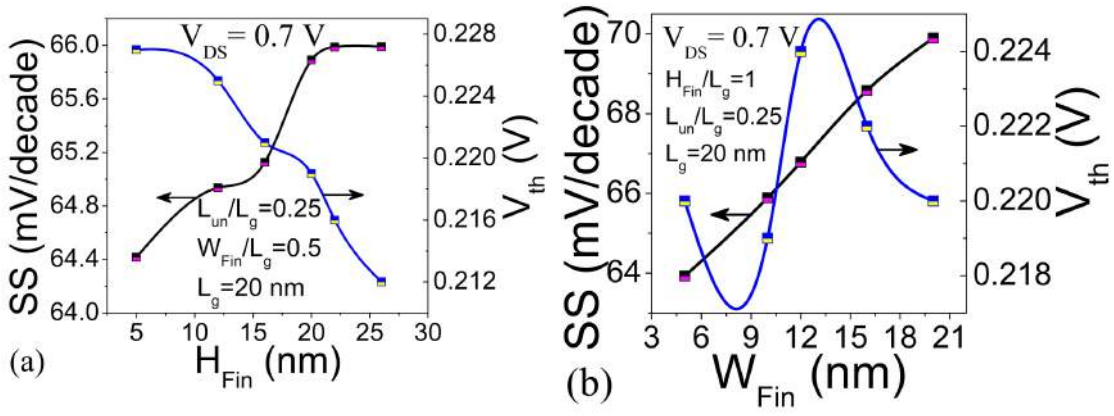


Figure 3.9: Dependency of SS and V_{th} on (a) H_{Fin} (b) W_{Fin}

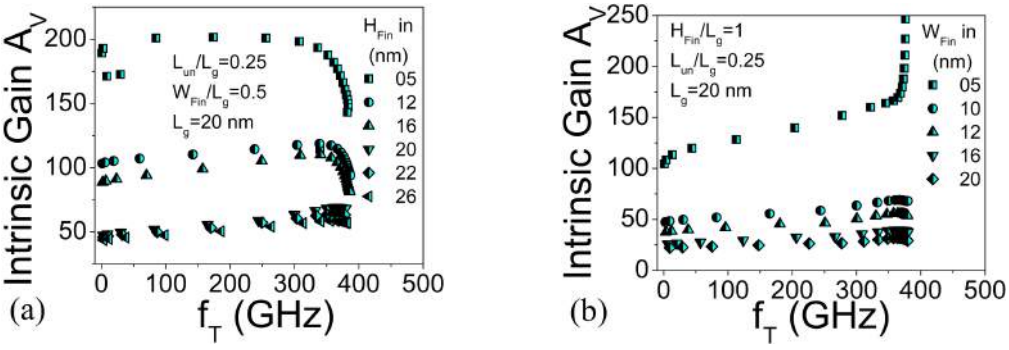


Figure 3.10: Dependency of A_V on f_T with variation of (a) H_{Fin} (b) W_{Fin}

I_{on} is discussed in Fig. 3.12 for different H_{Fin} and W_{Fin} values. Both I_{off} and I_{on} are increasing with increase in H_{Fin} and W_{Fin}. So, for optimum design in case of HP and LOP, the H_{Fin} and W_{Fin} can be chosen in between $0.6\times L_g$ and $0.8\times L_g$. So, it is very important to choose H_{Fin} and W_{Fin} to fit the delay requirements. Power Dissipation (PD) as a function of I_{off} with variation of H_{Fin} and W_{Fin} is examined in Fig. 3.13. From the Fig. 3.13, PD increases with increase in both values of H_{Fin} and W_{Fin}. This is due to the high I_{off} for higher values of H_{Fin} and W_{Fin}. The extracted values for all above said parameters are tabulated and compared for different H_{Fin} and W_{Fin} values in Table 3.1. From the table, there is a significant improvement in I_{on}/I_{off} can be observed for higher values of H_{Fin} as well as lower W_{Fin} values. Similar effects for other parameters with the variation of H_{Fin} and W_{Fin} can also be examined from the Table 3.1. From these results, one can carefully chose the critical device parameters.

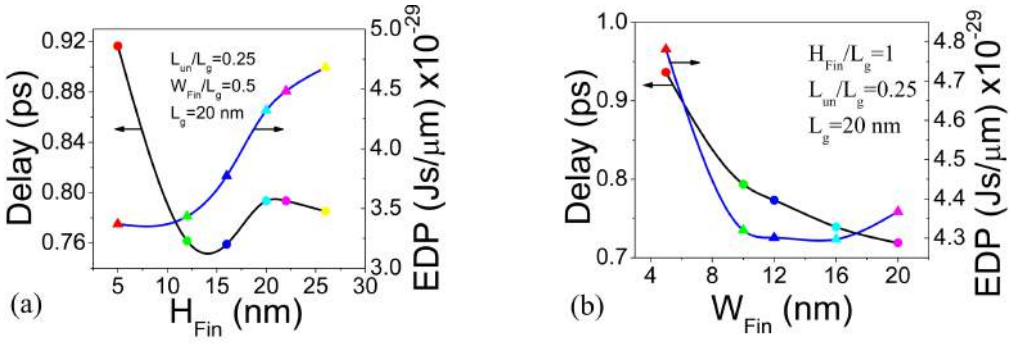


Figure 3.11: Dependency of cut-off frequency (f_T) on drain current for V_{DS}=V_{DD} with variation of L_{un} (a) DG; (b) FinFET.

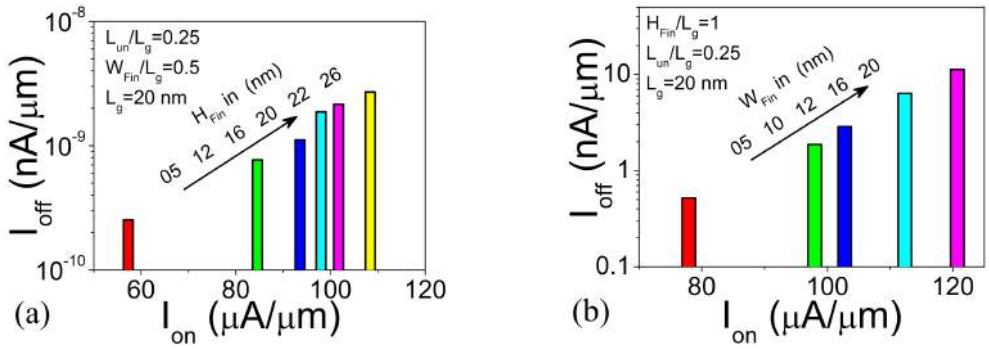


Figure 3.12: Trade-off between I_{off} on I_{on} for different (a) H_{Fin} (b) W_{Fin}

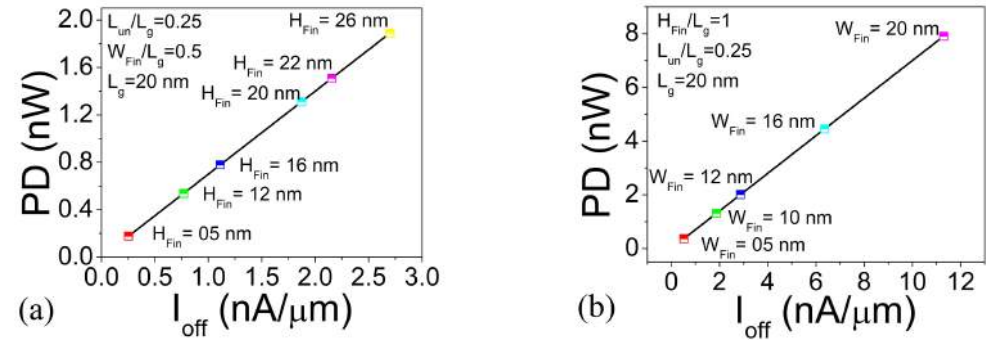


Figure 3.13: Dependency of Delay on I_{off} with variation of (a) H_{Fin} (b) W_{Fin}

3.6 Summary

Various performances of DG MOSFET and FinFET are systemically examined and compared using extensively 3-D device simulator Sentaurus^{TM} . We have optimized the gate underlap length (L_{un}) of both DG and FinFET, to demonstrate that L_{un} can be suitably chosen for HP or LOP applications. Analog/RF accomplishment of nanoscale DG MOSFET and FinFET is collated by means of 3-D numerical TCAD simulations. When underlap length increases, an improvement in P.D. occurs but with the compensation of high delay. Thus, it is needed to be careful while choosing L_{un}. There is an improvement in I_{on}/I_{off}, SS, L_{SD} and P.D. can be observed with increase in L_{un}. FinFET demonstrates better results in case of L_{SD}, P.D. and intrinsic delay over DG MOSFET. This is because Fin-

FET design has a bonzer control on the channel which shows better immunization capability towards short channel effects (SCEs). Among DG and FinFET, the former one gives higher current drivability, while the successive one shows the betterment in EDP and delay. This work assesses the performance analysis of a GaAs based FinFET for designing sub 20 nm technology node. From the results, we have obtained that taller fins are required for higher current drivability and narrower fins are required for higher immunization to SCEs. In case of H_{Fin} variation, H_{Fin} =0.6 $\times L_g$ case shows the optimum device performances in terms of gain and maximum frequency of operation. By thinning the W_{Fin}, we can able to make the FinFET free from substrate related effects which further improves the energy consumption, power dissipation, and SS of the device.

Table 3.2: Various performance comparison of III-V FinFET

	cases	Delay, (CV/I), (ps)	Energy (CV^2), (J), $\times 10^{-17}$	EDP, (Js), $\times 10^{-29}$	Inductance, L_{sd} (H), (Delay/g_{ds}), $\times 10^{-7}$	I_{on}/I_{off}, $\times 10^{-4}$	PD, ($I_{off} * V_{DD}$), (nW)
H_{Fin}/L_g	0.25	0.917	3.676	3.37	7.402	22.61	0.177
	0.6	0.762	4.508	3.434	3.205	11	0.538
	0.8	0.759	4.97	3.773	2.511	8.412	0.778
	1	0.794	5.44	4.32	2.044	5.232	1.311
	1.1	0.793	5.649	4.482	1.837	4.719	1.508
	1.3	0.785	5.958	4.679	1.534	4.013	1.891
W_{Fin}/L_g	0.25	0.936	5.107	4.781	7.434	14.95	0.364
	0.5	0.794	5.44	4.32	2.044	5.232	1.311
	0.6	0.773	5.562	4.301	1.535	3.578	2.01
	0.8	0.739	5.813	4.297	0.975	1.765	4.454
	1	0.719	6.074	4.367	0.708	1.068	7.907

Chapter 4

Role of Fin Height, Width and Aspect Ratio In SOI FinFET

4.1 Introduction

As observed from market demand, the need of people is tending towards electronic portable devices based on semiconductor. The density of transistors and other passive components in a chip, as well as the performance in terms of speed need to increase in order to maintain acceptable power consumption. That can be achieved through System-on-Chip (SoC) technology. SoC integrates most elements of a system as a stand-alone system on a single semiconductor chip. Its contents are programmable core processor(s), memory, input/output interfaces elements, along with software and analog/mixed signal functions [3], [27]. The most important component of ICs is the MOSFET which needs to be modeled and analyzed for better Short Channel Effects (SCEs) immunity and Electrostatic Integrity (EI) at nanoscale regime.

The continuation of CMOS scaling the conventional planar MOSFETs leads to increase in SCEs and leakage current [20], [21]. In order to overcome SCEs and leakage current different device structures like Double gate, Tri gate, FinFET and Silicon Nano Wire Transistors (SNWT) were proposed [2, 10, 28–30]. The transistor performance depends on the process- induced variations categorized under systematic values of gate length L_g, fin height (H_{Fin}), fin width (W_{Fin}), gate oxide thickness t_{ox}, channel doping etc. [10]âĂŞ[12]. The development of non-classical Multigate MOSFETs (Mug-FETs) brought about a chief progress at nano scale dimensions as reported by Colinge [8].

The advantages of Mug-FET technology are higher drain current and switching speed along with less than half the dynamic power requirement having 90% less static leakage current [31], [32]. The most important geometric parameter of FinFET technology is aspect ratio (AR=W_{Fin} /H_{Fin}) [33]. The structural classification of the device is FinFET (AR<1), Trigate (AR=1) and Planar (AR>1) [24]. Taller fins in the device show higher on current (I_{on}) and narrow fins establish SCEs immunity. A trade-off is required in between device performances with its aspect ratio [34], [35].

The FinFET design is evolving into further extensive as characteristics size within ICs decrease and also because there is a developing requirement to give much more elevated amounts of incorporation with less power utilization inside ICs. FinFETs are not accessible as discrete devices. So, it is essential to simulate for studying performance variation in view of analog and RF circuit application. In continuation with our previous reported article on DG-MOSFET [36], [37], a unique attempt has been made to present deep analysis of process variability dependency on various performance metrics of 3D FinFET.

While II part shows the device architecture of SOI-FinFET, section III describes simulation methodology with validation of models in the device simulator Sentaurus^{TM} [26]. Section IV investigates the performance measure of the device for analog and RF circuit applications with different Fin aspect ratio, the final conclusions are drawn in section V.

4.2 Device Structure

The 3-D SOI-FinFET simulated in the indicated task is displayed in Fig. 4.1. Table 4.1 that typifies the design considerations of the device. An n-channel

MOSFET having interfacial oxide as SiO_2 with Si_3N_4 as spacer in the underlap regimes are modeled. The L_S/L_D as 40 nm, and uniform doping, N_D, at a value of 10^{20} cm^{-3} is considered. EOT is 0.9 nm [25] [24] [38] while the supply voltage V_{DD} is 0.7 V. The work function for the metal gate is supposed to be 4.5 eV. The channel is undoped which boosts the mobility of the carriers and thus the I_{on} density from the source [39].

Table 4.1: Device Parameters As Per ITRS 2013

Design	HP	LOP	LSTP	This Work
				FinFET/Trigate
Gate length, L_g (nm)	20	20	20	20
EOT (nm), t_{ox}	0.84	0.9	1.2	0.9
Supply Voltage, V_{DD} (V)	0.85	0.67	0.87	0.7

Table 4.2: Typical Cases of 3-D SOI-FinFET for Simulation

Device Design[3][26][17]	H_{Fin}/L_g	W_{Fin}/L_g
	0.25, 0.6, 0.8, 1.0, 1.1, 1.3	0.25, 0.5, 0.6, 0.8

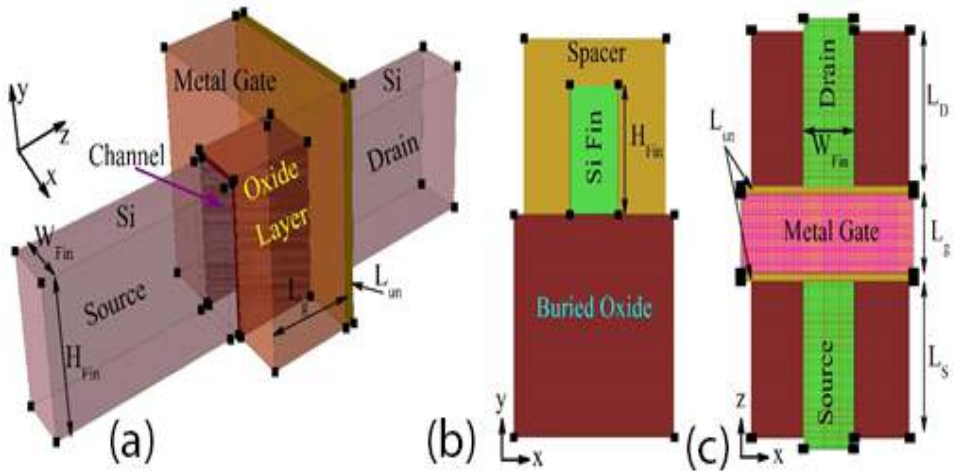


Figure 4.1: Perspective view of SOI FinFET (a) 3-D view (b) 2-D view in x-y (c) 2-D view in x-z . The metal and spacer regions are made transparent in (a).

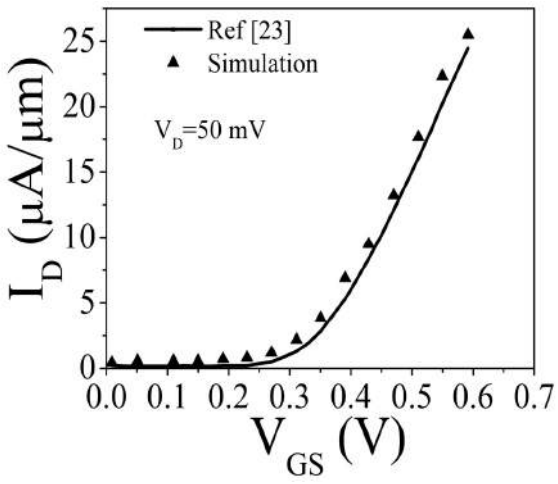


Figure 4.2: Matched I_D-V_{GS} characteristics of FinFET and simulation result

The effectiveness of the simulator has been checked by examining its outcomes with past literature data. From Fig. 4.2, it can be noticed that our simulation outcomes are in accord with Andrade et al. [25]. Table 4.2 symbolizes the typical cases that are reckoned for device simulation.

4.3 Simulation

Working Principle for Sentaurus TCAD

Modeling and simulation bridge the need for development and fabrication engineers by improving semiconductor process control in manufacturing. Sentaurus TCAD is a strong GUI-driven simulation environment for controlling simulation tasks and analyzing outcomes. Sentaurus TCAD simulations afford crucial insights on the nature of semiconductor devices, which can lead to new concepts. However, it needs to be properly calibrated for simulation.

Advantages of Sentaurus TCAD

- Reduces technology development time and cost.
- Provides full flow 3-D process and device simulation with advanced structure generation, meshing, and numeric.
- Supports insight into advanced physical phenomena, improving device design, yield, and reliability.
- Provides fast prototyping, development and optimization of semiconductor technologies.

Fig. 4.3 demonstrates the complete flow chart of working principle of Sentaurus TCAD i.e., creation of the device structure (including the doping profiles), and definition of the electrical contact are done through Sentaurus Structure Editor.

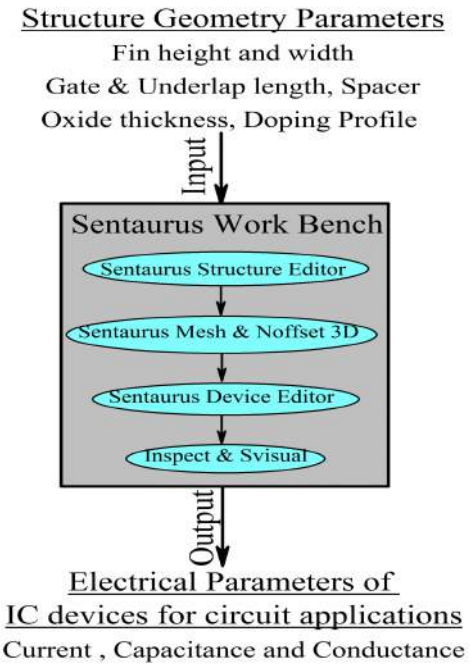


Figure 4.3: Simulation procedure in Sentaurus TCAD

Sentaurus Mesh and N-offset-3D generates the meshing for solving diffusion and transport equations through validation of various physical models (like bandgap narrowing, Fermi-Dirac, Band-to-Band tunneling, Drift-Diffusion, carrier mobility and velocity saturation). Sentaurus Device solves multiple, coupled physical equations based on the meshing, to properly estimate the device performance. Sentaurus Inspect and Svisual used to extract critical device performance parameters.

4.4 Results and Discussion

Various performance metrics like I_{on}, I_{off}, g_m, TGF, g_d, V_{EA}, C_{gg}, f_T, R_o, and Gain (A_V) are evaluated and the sensitivity of above said parameters with W_{Fin}, and H_{Fin} are systematically presented. Finally, depending upon the aspect ratio (W_{Fin}/H_{Fin}) of the device, the 3-D device is distinguished as FinFET or Trigate or planar MOSFET. The intrinsic delay and power dissipation are also discussed for all the three cases of the device.

4.4.1 Effect of H_{Fin}

In this section, the sensitivity of H_{Fin} with various key device parameters are studied. From the characteristic curve i.e., I_D-V_{GS}, some important technological parameters like I_{on}, I_{off}, and V_{th} are extracted for the device.

Fig. 4.4(a) and 4.4(b) presents the plot of g_m for 20 nm FinFETs at high ($V_{DD}/2$) and low (50 mV) drain biases for different H_{Fin}/L_g ratios.

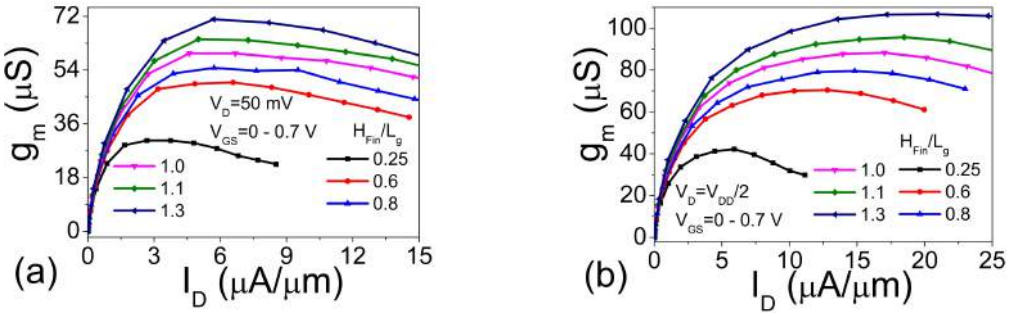


Figure 4.4: Transconductance (g_m) as a part of drain current (I_D) of the device (a) for V_{DS}=0.05 V (b) for V_{DS}=0.35 V. Main Device Parameters are L_g=20 nm, W_{Fin}=10 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, T=300 K.

To analyze the immense improvement in g_m ($\Delta I_D/\Delta V_{GS}$) with an increase in H_{Fin}/L_g ratio, we have evaluated and studied the I_D-g_m curve. According to the literature, access resistance problem is more serious in FinFETs. However, some solutions are available like increasing the H_{Fin} out of the gate region [11]. The parasitic resistance problem can be avoided by using higher H_{Fin}/L_g ratio which further increases the drain current. This is also validated from Fig. 4.4(a) and 4.4(b), both the parameters i.e., I_D, and g_m are increasing with the increase in H_{Fin}/L_g ratio. Higher I_D, and g_m values are obtained for H_{Fin}=1.1×L_g i.e., 22 nm and H_{Fin}=1.3×L_g i.e., 26 nm cases.

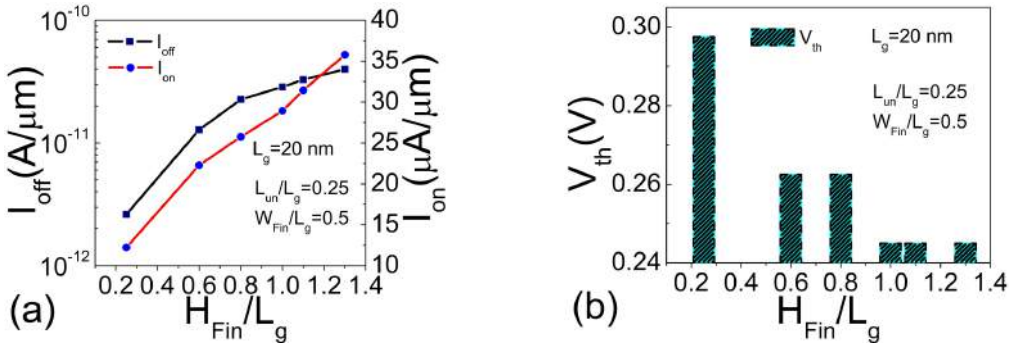


Figure 4.5: (a) Drain on current (I_{on}), Drain leakage current (I_{off}) and (b) V_{th} of the device as a part of normalized Fin height H_{Fin} with respect to physical gate length L_g.

Fig. 4.5(a) and 4.5(b) presents the extraction of parameters from the characteristic curves like I_{on} (I_{on} = I_D at V_{GS} = V_{DD}), (I_{off} = I_D at V_{GS} = 0 V) and threshold voltage (V_{th} =V_{GS} where I_D = 100 nA). There is always an agreement betwixt I_{on}, and I_{off} from device design point of view. So, the device engineers can pick the optimum device dimensions as per their requirements. After analyzing Fig. 4.5(a), both I_{on}, and I_{off} are increasing with the increase in the ratio of H_{Fin}/L_g. Hence this is to highlight that for higher current drivability, taller fins are required and for better SCE immunity, narrow fins are preferred. This is because narrow fins cause the decrease of electric field in the silicon region which minimizes the leakage current. By correlating the I_{on} and I_{off} for all H_{Fin}/L_g conditions, we can claim that H_{Fin} = 0.6×L_g or 0.8×L_g are the optimum cases as they predict moderate values for both I_{on} and I_{off}. The sensitivity of V_{th} towards H_{Fin}/L_g ratio is presented in Fig. 4.5(b). Threshold voltage for FinFET is usually

determined and controlled by the metal gate work function. However, it is very difficult to control V_{th} by tuning the gate work function in FinFETs because of inseparable gate as shown in Fig. 4.1 [40]. So, here we have discussed about V_{th} control by adjusting the fin height. As earlier stated in [41] that FinFETs have two limitations based on the fin height. If $H_{Fin} \ll W_{Fin}$, then FinFET will act like a FD-SOI MOSFET else in the reverse case ($H_{Fin} \gg W_{Fin}$), it behaves like a double gate (DG) MOSFET. So, it is more critical to fix the value of H_{Fin} for proper device operation with a better immunity towards SCEs. From Fig. 4.5(b) V_{th} decreases as H_{Fin}/L_g ratio increase leads to higher V_{th} roll-off and subthreshold slope for high H_{Fin} values which is verified from the data given in [41].

Fig. 4.6(a) and 4.6(b) show the variation of output conductance (g_d) with V_{DS} at high (0.35 V) and low (50 mV) gate biases for different H_{Fin}/L_g ratio. Because of the wrapping of gate from three sides of the channel and narrow Fin width, FinFETs have more electrostatic control over the channel and it is fully depleted. For this reason drain bias dependency (depletion width at drain side) is less, so is the channel length modulation (CLM) which further minimizes the change in I_D, and hence the g_d ($\Delta I_D/\Delta V_{DS}$) is low. Again from the Fig. 4.6(a) and 4.6(b), g_d increases with the increase in H_{Fin}/L_g ratio which can hamper the gain (g_m/g_d) of the device.

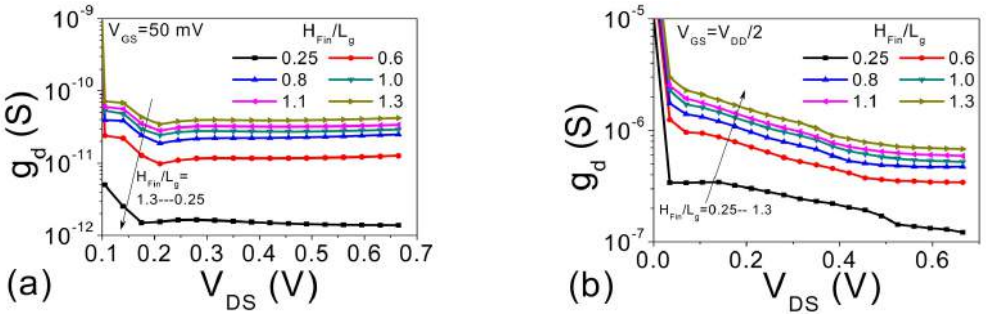


Figure 4.6: Drain conductance (g_d) of the device as a part of drain to source voltage (V_{DS}) (a) for V_{GS}=0.05 V (b) for V_{GS}=0.35 V. Main Device Parameters are L_g=20 nm, W_{Fin}=10 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}=5 nm, V_{DS} varied from 0 V-to-0.7 V, T=300 K.

CMOS Analog circuits require transistors with low g_d in order to achieve high gain. High g_d means low output resistance which resulting an increase in I_D with V_{DS} in the saturation regime. The components are associated with this increase, namely CLM and DIBL.

Fig. 4.7(a) and 4.7(b) demonstrate the intrinsic gain (A_V) for different region of operations of the FinFET with the variation of H_{Fin}/L_g ratio. From the figure, a decrement in H_{Fin}/L_g ratio will depict a higher A_V.

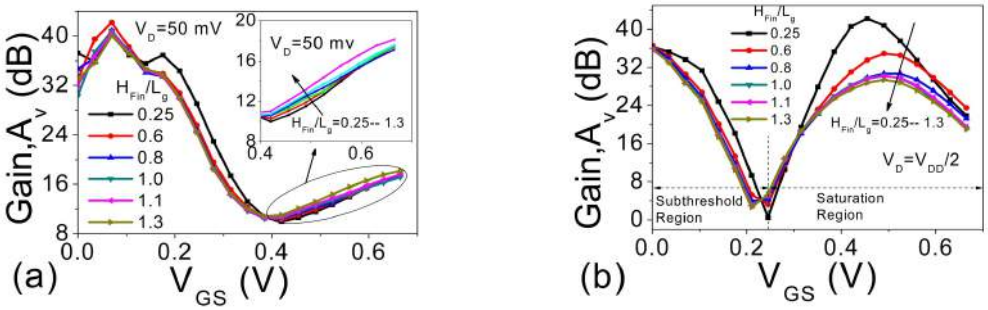


Figure 4.7: Intrinsic gain (A_V=g_m/g_d) as a part of gate to source voltage (V_{GS}) (a) for V_{DS}=0.05 V (b) for V_{DS}=0.35 V. Main Device Parameters are L_g=20 nm, W_{Fin}=10 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}=5 nm, V_{GS} varied from 0 V-to-0.7 V, T=300 K.

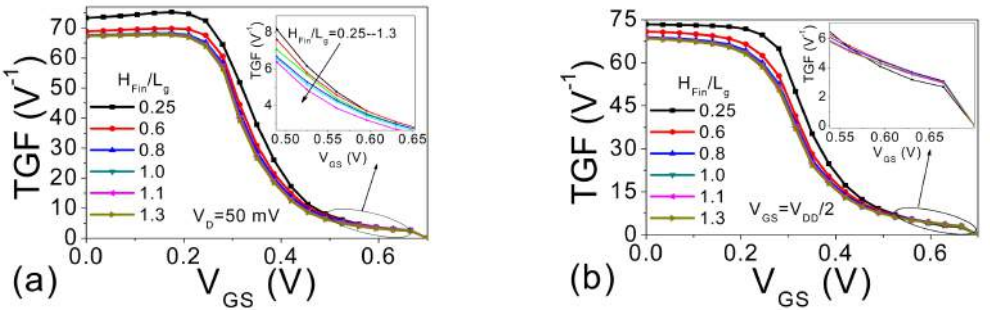


Figure 4.8: Transconductance generation factor (TGF=g_m/I_D) as a part of gate to source voltage (V_{GS}) (a) for V_{DS}=0.05 V (b) for V_{DS}=0.35 V. Main Device Parameters are L_g=20 nm, W_{Fin}=10 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}=5 nm, V_{GS} varied from 0 V-to-0.7 V, T=300 K.

This is due to the large reduction in g_d values for lower H_{Fin}/L_g ratios which is already discussed in Fig. 4.6. Transconductance generation factor (TGF=g_m/I_D) is plotted against V_{GS} with a variation of H_{Fin}/L_g ratio at two different V_{DS} is plotted in Fig. 4.8(a) and 4.8(b). TGF demonstrates the effective use of the current to accomplish a desired value of g_m. The high value of TGF is advantageous to realize analog circuits which are operating at low supply voltages. From the figure, the variation of TGF occurs at subthreshold region (at low V_{GS} and low V_{DS}) of operation and almost same TGF is achieved in strong inversion. This g_m/I_D ratio is inversely proportional to the level of channel inversion i.e., to the higher I_D value. From Fig. 4.8(a) and 4.8(b), lower H_{Fin}/L_g ratios depict high TGF values and it gradually decreases as H_{Fin}/L_g ratio increases in the subthreshold region of operation. This is due to the higher I_D values for larger H_{Fin}/L_g ratios as given in Fig. 4.4.

Also, a low g_d propagates a higher drain current to output conductance ratio, which is nothing but the early voltage (V_{EA} = I_D/g_d) of the device. Fig. 4.9(a) and 4.9(b) show the variation of V_{EA} as a function of V_{GS} for different H_{Fin}/L_g ratios at two regions of operation. From the Fig. 4.9(a) and 4.9(b), the devices with small H_{Fin}/L_g ratios have a good control over CLM and DIBL owing to low g_d value which further improves the V_{EA}. For better analog performance, the V_{EA} and A_V should be as high as possible. The V_{EA} is increasing with a decrease in H_{Fin}/L_g ratio in the subthreshold region (V_{DD}= 50 mV), however, there is no such variations in the super-threshold region (V_{DD}= 0.35 V).

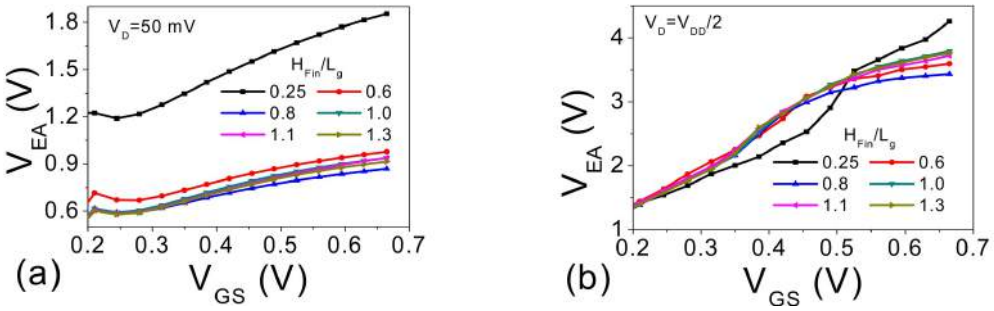


Figure 4.9: Early Voltage (V_{EA}=I_D/g_d) as a part of drain to source voltage (V_{DS}) (a) for V_{GS}=0.05 V (b) for V_{GS}=0.35 V. Main Device Parameters are L_g=20 nm, W_{Fin}=10 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{GS} varied from 0 V-to-0.7 V, T=300 K.

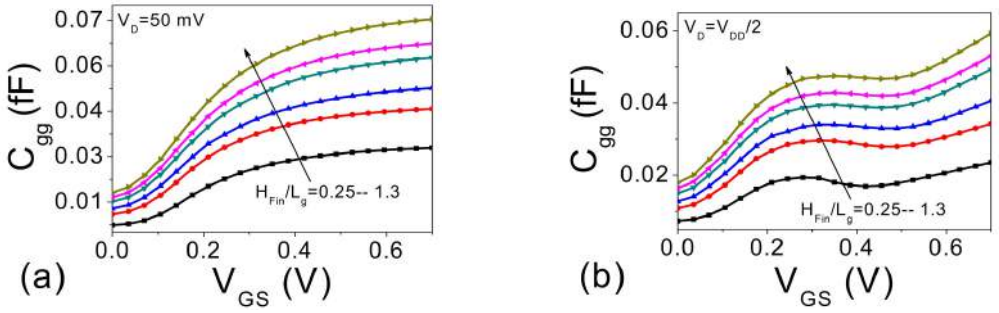


Figure 4.10: Total gate capacitance (C_{gg}) as a part of gate to source voltage (V_{GS}) (a) for V_{DS}=0.05 V (b) for V_{DS}=0.35 V. Main Device Parameters are L_g=20 nm, W_{Fin}=10 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{GS} varied from 0 V-to-0.7 V, T=300 K.

From Fig. 4.10, the C_{gg} value of the device increases with an increase in H_{Fin}/L_g ratio. This is caused by the increased fringing field density with H_{Fin}/L_g ratio. Sun et al. [22] have reported that H_{Fin} = 0.6×L_g or 0.8×L_g are good for better SCE immunity. So, we have varied H_{Fin} from 0.25×L_g to 1.3×L_g. As FinFET has a taller stripe than the height of gate electrode along the channel side walls, which increases the fringing field, so as the total capacitance. Cut-off frequency, f_T, is a standout amongst the most imperative parameters for assessing the RF execution of the device. Generally, f_T is the frequency at which the current gain is unity. From Fig. 4.11(a) and 4.11(b), the variations of f_T can be observed with respect to V_{GS} for different H_{Fin}/L_g ratios. As we know f_T = $g_m/2\pi C_{gg}$, so both g_m and C_{gg} values will have equal and opposite influence on f_T. The reduction in capacitance in case of lower H_{Fin}/L_g ratios (refer Fig. 4.10) is further counterbalanced by the reduction of g_m with reduction in H_{Fin}/L_g ratio (refer Fig. 4.4). It is very much significant that the forecast improvement in f_T with traditional scaling of a FinFET can be only achievable by choosing the optimal value of H_{Fin} and W_{Fin}. The difference in f_T is mainly due to the difference in g_m, and partially due to the higher value of total capacitance (C_{gg}). The crest point of f_T compares to the point between the base entryway channel/source capacitance and top of transconductance. It is also clear from Fig. 4.11 that f_T is highest for the device having H_{Fin} = 0.6×L_g, reflecting predominant gate controllability and thus higher transconductance and lower parasitic gate capacitances when contrasted with different devices taken in our analysis.

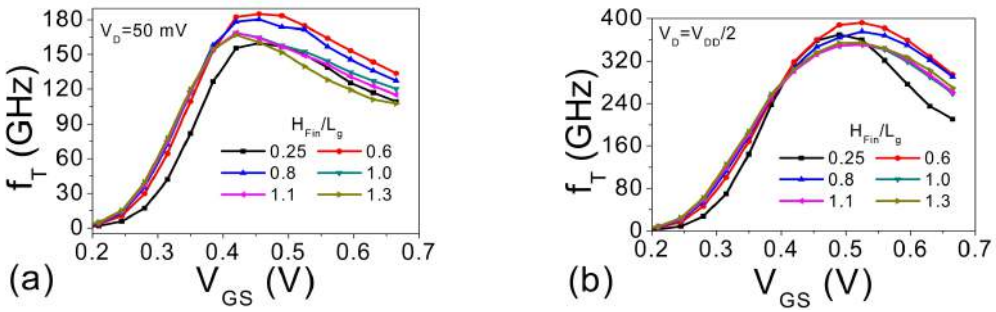


Figure 4.11: Cut-off frequency (f_T) as a part of gate to source voltage (V_{GS}) (a) for V_{DS}=0.05 V (b) for V_{DS}=0.35 V. Main Device Parameters are L_g=20 nm, W_{Fin}=10 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{GS} varied from 0 V-to-0.7 V, T=300 K.

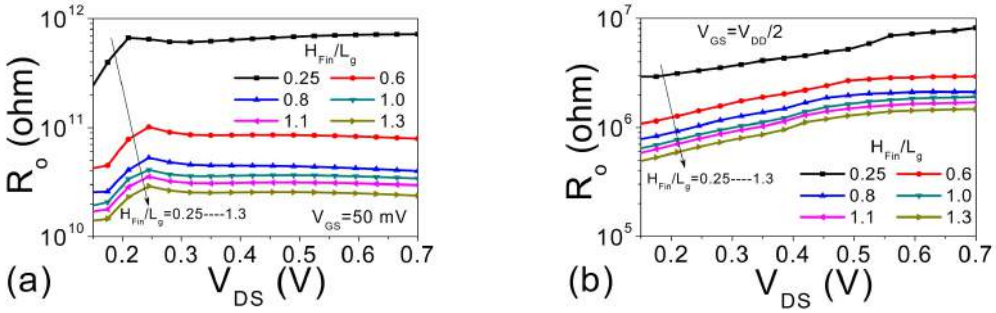


Figure 4.12: Output resistance (R_o) of the device as a part of drain to source voltage (V_{DS}) (a) for V_{GS}=0.05 V (b) for V_{GS}=0.35 V.

Fig. 4.12 (a) and 4.12 (b) show the output resistance (R_0) for different H_{Fin}/L_g ratios at low and high V_{DS}. R_0 also have an impact on the intrinsic gain ($g_m R_0$). According to the figure, the lower H_{Fin} devices predict larger R_0. This is due to the improvement in SCEs and lower values of g_d (as $R_0 = 1/g_d$) for low H_{Fin}/L_g ratios (refer Fig. 4.6).

4.4.2 Effect of W_{Fin}

Similar type of analysis as in the previous section are systematically investigated and discussed with a variation of W_{Fin}/L_g ratio. By choosing a smaller W_{Fin}, we can be able to minimize the longitudinal electric field at the source side because of closeness of multiple gates [27]. However, as scaling approaches the fundamental dimension such as atomic size range and the sensitivity of the device, parameters have a greater effect on the device performance. Particularly in case of analog/RF performance, the deviation of results are much larger with a small change in device design parameters [27]. So, in this work we have systematically explored the impact of W_{Fin}/L_g ratio on the analog/RF performance of the FinFET.

Fig. 4.13 (a) and 4.13 (b) show the g_m- I_D plot with a variation of W_{Fin}/L_g ratio at V_{DS}=0.05 V and V_{DS}=0.35 V respectively. Here W_{Fin} is varied from $0.25\times L_g$ to $1.0\times L_g$ because for this aforesaid technology node, Sun et al. [22] have reported that W_{Fin}=$0.6\times L_g$ for FinFET and W_{Fin}=$1.0\times L_g$ for Trigate is required to minimize SCEs. Both I_D and g_m are increasing with the increase in W_{Fin}/L_g ratio as predicted and obtained maximum values at W_{Fin}=$0.25\times L_g$. The effect of series resistance is clearly visible from Fig. 4.13 (a) (low drain bias/linear

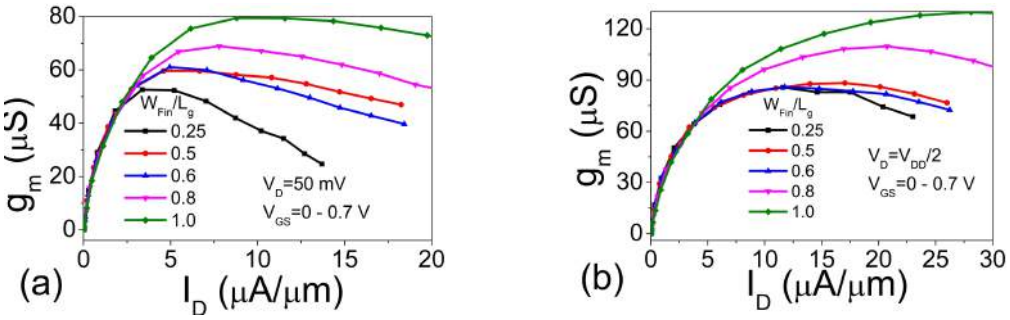


Figure 4.13: Transconductance (g_m) as a part of Drain current (I_D) of the device (a) for V_{DS}=0.05 V (b) for V_{DS}=0.35 V. Main Device Parameters are L_g=20 nm, W_{Fin}=10 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{GS} varied from 0 V-to-0.7 V, T=300 K.

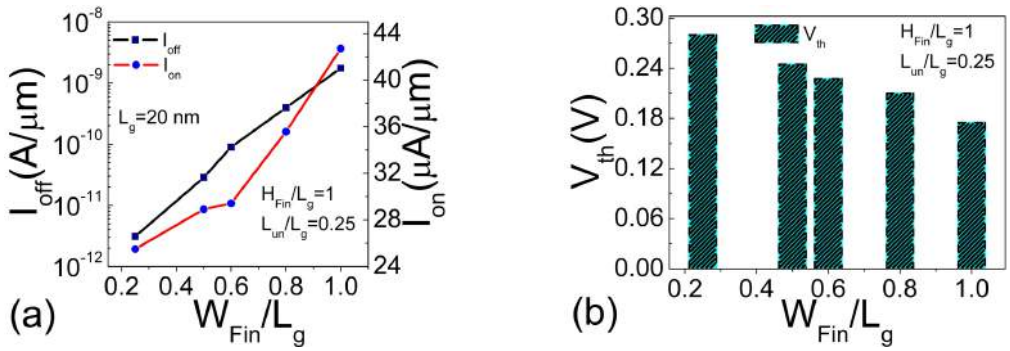


Figure 4.14: (a) Drain on current (I_{on}), Drain leakage current (I_{off}) and (b) threshold voltage (V_{th}) of the device as a part of normalized Fin width W_{Fin} with respect to physical gate length L_g.

region) by not following the linear dependency nature for low W_{Fin} cases. From this analysis, we can say that the R_S is much higher for low Fin width devices.

The extraction values of I_{on}, I_{off} and V_{th} are plotted against W_{Fin}/L_g ratios in Fig. 4.14 (a) and 4.14 (b) respectively. As W_{Fin} increased, both I_{on} and I_{off} increases and reaches their maximum values for W_{Fin}=1.0×L_g. Here H_{Fin}/L_g ratio is fixed at 1.0 and W_{Fin}/L_g is varied ranging from 0.2 to 1.0. For W_{Fin}=0.6xL_g, case we are getting desirable values for both I_{on} and I_{off} i.e., I_{on}=30μA and I_{off} of 10^{-11} A. The V_{th} is extracted from I_D-V_{GS} curve and plotted by varying W_{Fin}/L_g ratio ranging from 0.2 to 1.0. V_{th} value decreases with an increase in W_{Fin}/L_g ratio which further degrades the device performance because of the SCEs like DIBL, V_{th} roll-off and CLM. This is also verified from the experimental data presented in [42]. As W_{Fin}/L_g decreases, the coupling between front and back interface is reduced which enhances V_{th} value. From this analogy, it may be predicted that by considering thicker H_{Fin} and thinner W_{Fin} we can enhance the FinFET performance.

Fig. 4.15 (a) and 4.15 (b) demonstrate g_d-V_{DS} curve for different W_{Fin}/L_g ratios at two regions of operation. The output conductance is related to the important device dimensions as (g_d = 2H_{Fin}+W_{Fin}) [43]. So, g_d is directly proportional to W_{Fin} i.e., narrower W_{Fin} predicts lower g_d value which is our requirement. It can be observed that, the g_d variation is more for higher applied voltage (V_{GS}=V_{DD}/2) case. This because of the device is heating at higher biasing voltage. Moreover, thinning the W_{Fin} and reducing the supply voltage are worthy enough to reduce

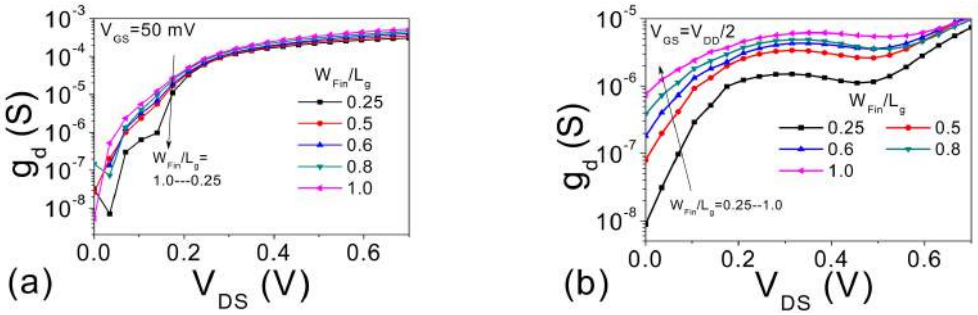


Figure 4.15: Drain conductance (g_d) of the device as a part of drain to source voltage (V_{DS}) (a) for V_{GS}=0.05 V (b) for V_{GS}=0.35 V. Main Device Parameters are L_g=20 nm, H_{Fin}=20 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{DS} varied from 0 V-to-0.7 V, T=300 K.

the body heating problem, hence, the SCEs. So, the FinFETs with thinner fin width are well known for suppression of SCEs because they are free from substrate associated degradation in the g_d.

Fig. 4.16(a) and 4.16(b) show the intrinsic gain (A_V) of the device against V_{GS} with a variation of W_{Fin}/L_g ranging from 0.25 to 1.0 at V_{DS}=50 mV and $V_{DD}/2$. A higher gain can be observed for the FinFETs having lower fin widths is due to the much lower g_d (refer Fig. 4.15), which is because of the full depletion of fins.

A plot of TGF (g_m/I_D) as a part of V_{GS} for both linear and saturation regions of operation is given in Fig. 4.17 (a) and 4.17(b). g_m/I_D is more sensitive to W_{Fin}/L_g ratio at linear region (low V_{GS}), however in saturation region (high V_{GS}), the variation seems to be much smaller (refer the inset figure).

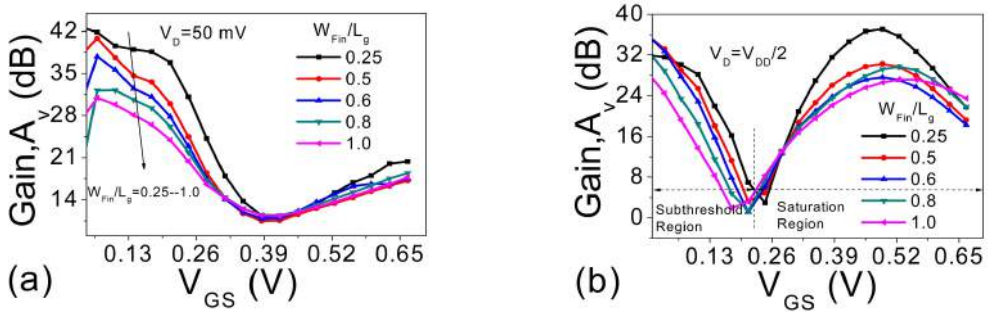


Figure 4.16: Intrinsic gain (A_V=g_m/g_d) as a part of gate to source voltage (V_{GS}) (a) for V_{DS}=0.05 V (b) for V_{DS}=0.35 V. Main Device Parameters are L_g=20 nm, H_{Fin}=20 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{GS} varied from 0 V-to-0.7 V, T=300 K.

As per Subramanian et al., [42] g_m/I_D has a strong dependency on series resistance (R_S) than any other parameter. So, I_D,sat is a strong function of R_S and the ratio (g_m/I_D)sat is a weak function of Rs hence less sensitive in the saturation region.

Basically, the decrement in g_d for low fin widths can also be explained in terms of higher early voltage (V_{EA}=I_D/g_d) as observed from Fig. 4.18 (a) and 4.18 (b). V_{EA} is generally used to explain the I_D-V_{DS} curve for BJT, however in case of MOSFET, it is the hypothesized intercept of saturation output characteristics on the V_{DS} axis. However, we can say that lower W_{Fin}/L_g ratios predict better

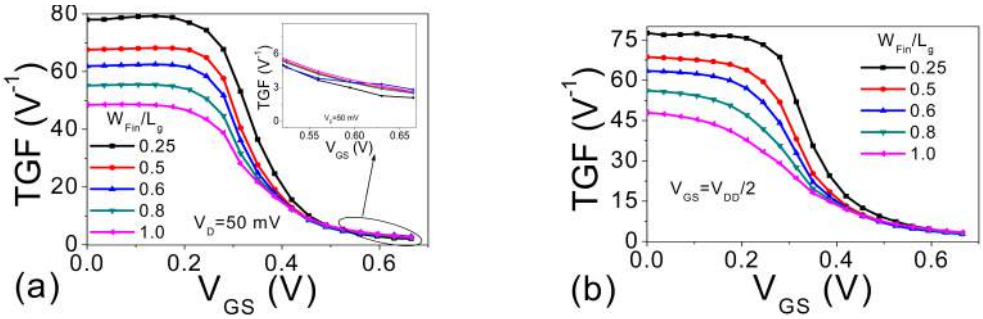


Figure 4.17: Transconductance generation factor (TGF=g_m/I_D) as a part of gate to source voltage (V_{GS}) (a) for V_{DS}=0.05 V (b) for V_{DS}=0.35 V. Main Device Parameters are L_g=20 nm, H_{Fin}=20 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{GS} varied from 0 V-to-0.7 V, T=300 K.

V_{EA} due to the reduction of substrate effect, body heating problem, and better immunity towards SCEs as discussed under Fig. 4.15.

The C_{gg}-V_{GS} data for different fin width at V_{DS}= 0.05 V and 0.35 V are presented in Fig. 4.19 (a) and 4.19 (b) respectively. It can be measured that the C_{gg} values are much lower for FinFETs with low W_{Fin}/L_g ratios. There is a 25.37% of reduction in C_{gg} from W_{Fin}/L_g=1 to W_{Fin}/L_g=0.25. However, from Fig. 13, we know that higher W_{Fin}/L_g ratios also predict high transconductance values. So, increase in g_m contributes to abolish the increment of C_{gg}, which results in a little variation in cutoff frequency for all cases of W_{Fin}/L_g as shown in Fig. 4.20.

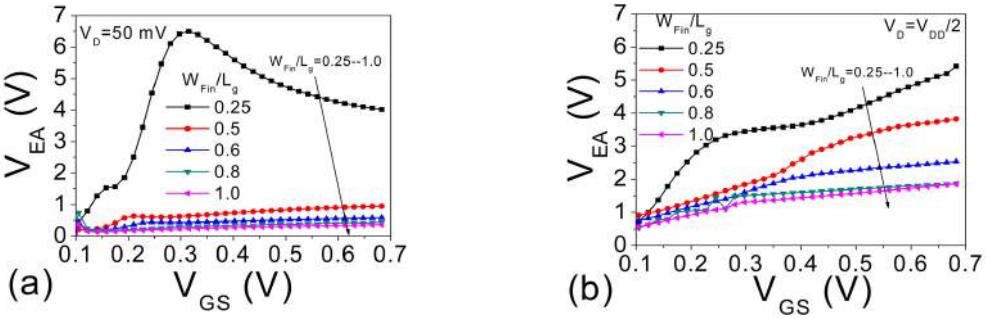


Figure 4.18: Early Voltage (V_{EA}=I_D/g_d) as a part of drain to source voltage (V_{DS}) (a) for V_{GS}=0.05 V (b) for V_{GS}=0.35 V. Main Device Parameters are L_g=20 nm, H_{Fin}=20 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{GS} varied from 0 V-to-0.7 V, T=300 K.

The high frequency (f_T=$g_m/2\pi C_{gg}$) of operation for different W_{Fin}/L_g ratios can be observed from Fig. 4.20 (a) and 4.20 (b). f_T is extracted at which the current gain is unity. A little improvement of f_T can be observed with an increase in fin width. This difference in f_T is mainly due to the difference in g_m, as observed in Fig.4.13, and due to the higher value of total capacitance (C_{gg}), as observed in Fig. 4.19. The crest point of f_T relates to the point betwixt the gate channel/source capacitance and top of transconductance.

Fig. 4.21 (a) and 4.21 (b) compare the output resistance (R_0) with a variation of W_{Fin} ranging from 5 nm to 20 nm at low V_{GS} (50 mV) as well as high V_{GS} (0.35 V). There is no such variation in R_0 with respect to W_{Fin}/L_g ratio observed for lower V_{GS} case. However, there is a significant variation in case of higher V_{GS} with W_{Fin}/L_g ratio. This is because of the dependency of R_0 on electric field and

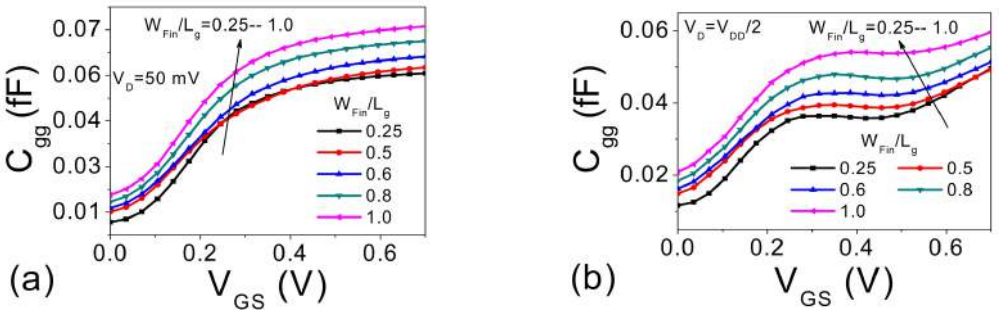


Figure 4.19: Total gate capacitance (C_{gg}) as a part of gate to source voltage (V_{GS}) (a) for V_{DS}=0.05 V (b) for V_{DS}=0.35 V. Main Device Parameters are L_g=20 nm, H_{Fin}=20 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{GS} varied from 0 V-to-0.7 V, T=300 K.

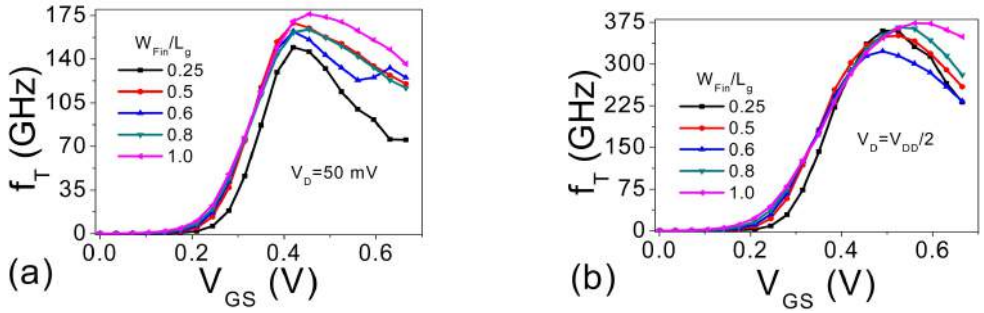


Figure 4.20: Cut-off frequency (f_T) as a part of gate to source voltage (V_{GS}) (a) for V_{DS}=0.05 V (b) for V_{DS}=0.35 V.

possibly due to the bias voltage. From Fig. 4.21 (b), a low value of R_0 is observed for thicker W_{Fin} values where current crowding or electron pile-up effects are more serious. This results in an improvement in drive current and transconductance as discussed under Fig. 4.13. So, FinFETs with high W_{Fin}/L_g ratio give higher g_m, but they have a poor gate control results severe SCEs (low device gain) and FinFETs with low W_{Fin}/L_g ratio predict high series resistance which limits the achievable g_m, but better immunity towards SCEs as it shows higher gain.

Aspect Ratio (AR)

Up to this, we have systematically investigated the parameter variation (W_{Fin} and H_{Fin}) effects on several device performances including DC as well as Analog/RF. From the above study, taller fins are needed for higher current drivability and also shows a little improvement in high frequency of operation whereas shorter fins are required for better SCEs. From this point of view, aspect ratio (AR=W_{Fin}/H_{Fin}) of the device is a very interesting and important parameter from FinFET design consideration point of view. However, some fabrication limitations are major concerns to achieve such taller fin heights and narrower fin widths.

In this section, according to the AR we have distinguished the device as FinFET, Trigate, and Planar MOSFET. The device having $H_{Fin} > W_{Fin}$ (i.e., AR<1) is known as FinFET, and the reverse i.e., $H_{Fin} < W_{Fin}$ (AR>1) is considered as Planar MOSFET, and where $H_{Fin} = W_{Fin}$ (AR=1) is called Trigate [33].

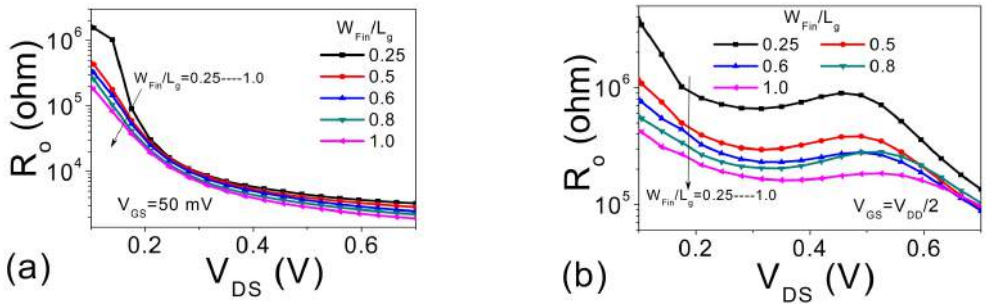


Figure 4.21: Output resistance (R_o) of the device as a part of drain to source voltage (V_{DS}) (a) for V_{GS}=0.05 V (b) for V_{GS}=0.35 V. Main Device Parameters are L_g=20 nm, H_{Fin}=20 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{DS} varied from 0 V-to-0.7 V, T=300 K.

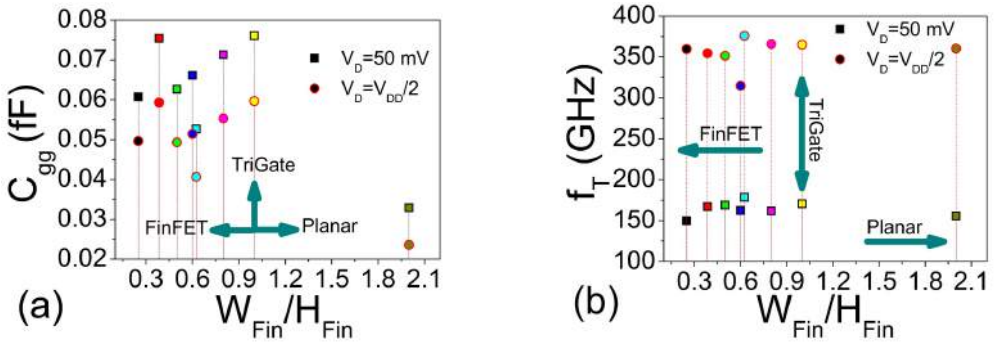


Figure 4.22: (a) Total gate capacitance (C_{gg}) (b) Cutoff frequency (f_T) as a part of Fin aspect ratio (AR=W_{Fin}/H_{Fin}). Main Device Parameters are L_g=20 nm, t_{ox}=0.9 nm, t_{box}=40 nm, t_{sub}=70 nm, L_{un}= 5 nm, V_{GS} = V_{DS} = V_{DD} = 0.7 V, T=300 K, AR varied as (0.250, 0.385, 0.5, 0.6, 0.625, 0.8, 1.0, 2.0).

The total gate capacitance (C_{gg}) and cutoff frequency (f_T) with a variation of AR are given in Fig. 4.22 (a) and 4.22 (b) respectively. In case of Planar MOSFET i.e., for AR>1, the obtained C_{gg} is reasonably low which further enhances the f_T. By comparing all different AR cases, AR=0.6 gives better values for both C_{gg} and f_T. From the circuit level design requirements, the intrinsic delay is the more important measure to be analyzed. So to minimize the intrinsic delay ($(C_{gg}*V_{DD})/I_{eff}$), the optimization of delay is included with respect to aspect ratio. Where I_{eff} is the average of I_D at V_{GS}=V_{DD} and V_{DS}=$V_{DD}/2$ and I_D for V_{GS}=$V_{DD}/2$ and V_{DS}=V_{DD} [44]. The I_{off}, intrinsic delay, and static power dissipation (V_{DD}*I_{off}) with variation of AR ranging from 0.3 to 2 are plotted in Fig. 4.23 (a), 4.23 (b) and 4.23 (c) respectively. For FinFET design with AR=0.3 and Planar design with AR=2, the I_{off} is diminished by a larger factor as contrasted to other designs including the Trigate design (AR=1). Similarly, intrinsic delay and power dissipation can be observed and compared for different designs (FinFET, Trigate and Planar). The Trigate design (AR=1) shows minimum delay but again maximum power dissipation as compare to its counterparts. This is due to the high I_{eff} in case of AR=1. However, the FinFET design with AR=0.3 and Planar with AR=2 show optimum values of power dissipation.

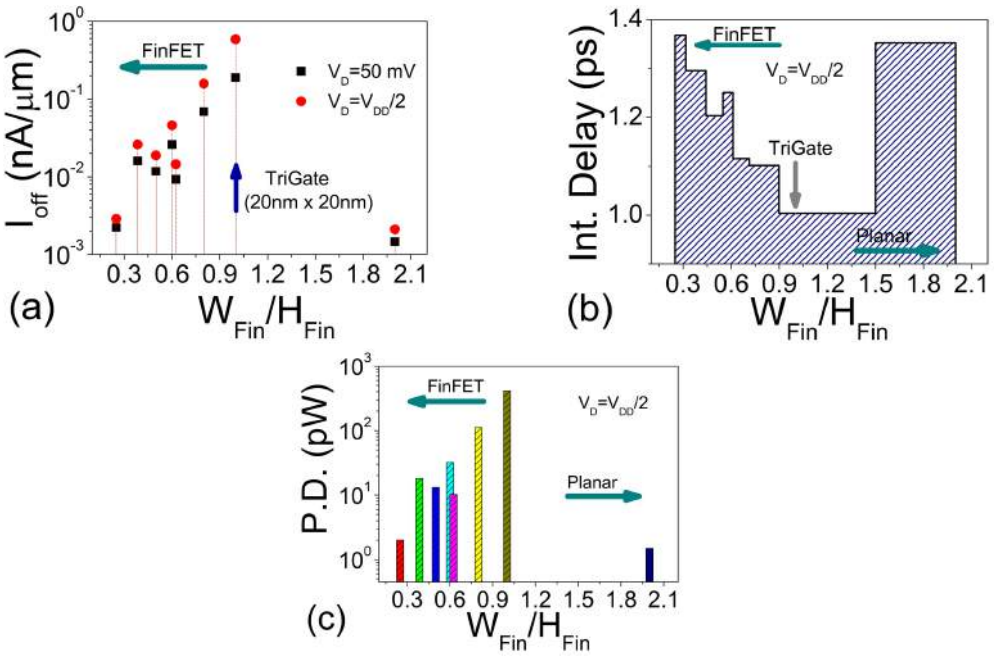


Figure 4.23: (a) Drain leakage current (I_{off}) (b) Intrinsic Delay ($(C_{gg}{*}V_{DD})/I_{eff}$) (c) Static power dissipation ($V_{DD}{*}I_{off}$) as a function of Fin aspect ratio (AR=W_{Fin}/H_{Fin}).

4.5 Summary

The process parameters like H_{Fin}, W_{Fin}, and Aspect Ratio (AR=W_{Fin}/H_{Fin}) are most important for designing FinFETs. This report provides an extensive analysis of process variability parameters in device design perspective point of view. From the results, it is deduced that taller fins are required for higher current drivability and narrower fins are required for higher immunization to SCEs. In case of H_{Fin} variation, H_{Fin}=$0.6\times L_g$ case shows the optimum device performances in terms of gain and maximum frequency of operation. By thinning the W_{Fin}, FinFET can be freed from substrate related effects which further improves the A_V, V_{EA}, and R_0 of the device. The Trigate (AR=1) shows a tremendous improvement in delay of the device because of higher I_{eff}. However, FinFETs (AR<1) and Planar MOSFETs (AR>1) predict desirable improvements in power dissipation and f_T. Thus, this work provides valuable results to design a FinFET or Trigate or Planar MOSFET according to the requirement for HP or LSTP applications.

Chapter 5
Analysis of CMOS Design

5.1 Introduction

Scale-down of device dimensions in conventional bulk-silicon CMOS technology has been a prime driving force of the semiconductor industry development from the last thirty years. The better performance with the smaller size of the devices has been the basis of this development. However, for conventional bulk-Si and PD SOI CMOS, carried on scaling much after a L_g of = 50nm [45] is doubtful. This is because of severe short-channel effects (SCEs), high off-state leakage currents, and unacceptably low I_{on}/I_{off} ratios. Indeed, controlling the body doping within very small dimensions, which is required for SCE control, has been the most difficult technological challenge to overcome for further scaling. Thus, there is a developing enthusiasm for non-classical completely drained (FD) SG and DG MOSFETs with ultra-thin bodies (UTBs), which have inborn concealment of SCEs. Their little characteristic gate capacitance in powerless/moderate reversal regions and, particularly for DG devices, the high $I_{on}/\ I_{off}$ proportion originating from the about perfect subthreshold gate swing infer significant CMOS speed predominance over the traditional SG partners [46]. In any case, DG innovation is complex; the DG FinFET [47, 48] is least demanding to create, however its demonstrated utility is years away.

Conflictingly, FD/SOI SG innovation is less confused; SOI UTBs and metal gates are the principle obstructions in its improvement [49]. On account of the technological complexities and challenges connected with DG CMOS, inquiries have been postured about the execution advantage, in respect to SG CMOS, that it can possibly give. Case in point, if the DG MOSFET gives double the current, however with double the gate capacitance, then unnecessary device parasitics suggested by the unpredictable innovation may render substandard execution. In addition, it has been contended that SCEs in the bulk Si SG MOSFET could be adequately stifled by super-halo channel doping such that bulk Si CMOS could really be downsized to 25 nm channel lengths [50]. Nonetheless, this contention is recreation based, and there is instability about the physical displaying accepted and whether the expected device structure could even be manufactured [Tau98]. Regardless, given such a "speculative" nanoscale bulk Si CMOS innovation, more itemized experiences on the relative execution possibilities of non-classical UTB CMOS would be valuable in choosing how and in the event that they ought to be forcefully sought after.

5.2 Device Structure

The symbol of a basic inverter is shown in Fig. 5.1, which tells about the basic operation of a CMOS inverter as it simply inverts the inputs.

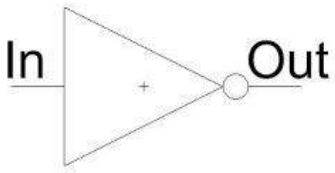
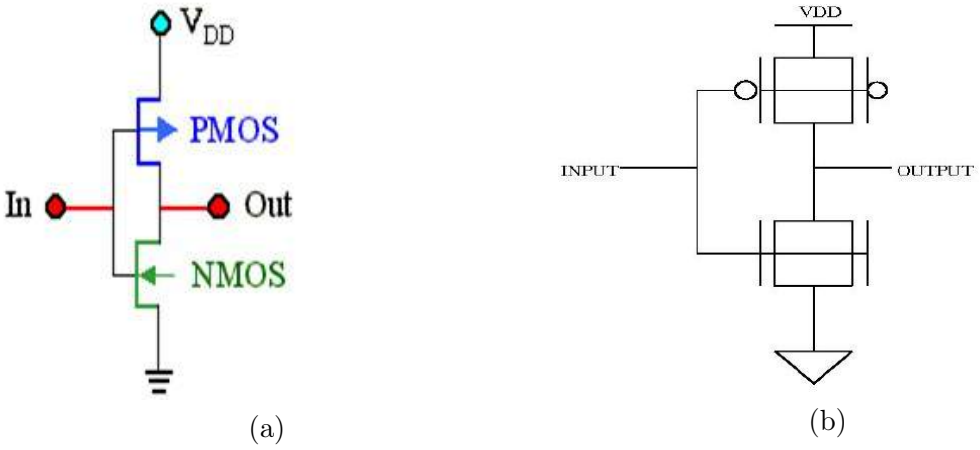


Figure 5.1: Symbol of a basic Inverter



(a) (b)

Figure 5.2: Circuit diagram of (a) SG CMOS and (b) DG CMOS

Figure 5.2 shows the circuit diagram of a static CMOS inverter of SG and DG. Its procedure is easily understood with the benefit of the simple switch model of the MOS transistor. The transistor is simply like a switch with an enormous off resistance (for $|V_{GS}| < |V_T|$), and a definate on-resistance (for $|V_{GS}| > |V_T|$). This leads to the further analysis of the inverter. When V_{in} is high and equal to V_{DD}, the NMOS transistor is on, while the PMOS is off. A direct path exists between V_{out} and the ground node, resulting in a steady-state value of 0V. Furthermore, when the input voltage is low (0 V), NMOS and PMOS transistors are off and on, respectively. It describes that a path exists between V_{DD} and V_{out}, results in high output voltage. The gate clearly functions as an inverter.

From switch level view, number of other desired properties of static CMOS can be derived as follows:

- The high and low output levels equal V_{DD} and GND, respectively; in other words, the supply voltage is equal to the voltage swing and results in high noise margins.
- There always exists a path with fixed resistance between the output and either V_{DD} or GND in steady state. A well-designed CMOS inverter, therefore, has a low output impedance, which makes it less responsive to noise and disruption. Expected values are in kW range for output resistance.
- The input resistance of the CMOS inverter is intensely large, as the gate of an MOS transistor is essentially ideal insulator and takes no dc input current. Since the transistor gates connects to only input node of the inverter, the steady-state input current is approximately zero. A single inverter can

apparently lift an enormous number of gates (or have an infinite fan-out) and still be practically operative; nonetheless, increase in the fan-out also increases the propagation delay. So, although fan-out does not have any effect on the steady-state nature, it reduces the momentary response.

- No direct path exists between the supply and ground rails under steady-state operating conditions (this is, when the input and outputs remain same). The absence of current flow (ignoring leakage currents) means that the gate does not dissipates any static power.

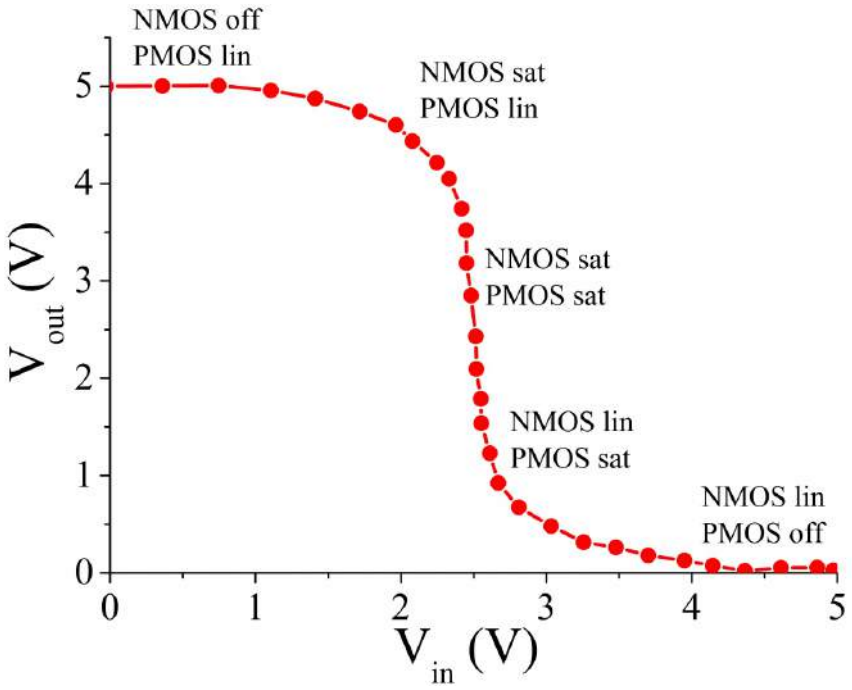


Figure 5.3: CMOS Inverter Voltage Transfer Characteristics

For valid dc operating points, the currents through the NMOS and PMOS devices must be same. Distinctly, this explains that the dc points must exists at the interface of respective load lines. As observed, all operating points exists at extremes output levels. The VTC of the inverter hence shows a very limited evolution zone. This results from the high gain during the switching transient, when both NMOS and PMOS are on at the same time, and are in saturation. In that operation region, a small change in the input voltage results in a large output change. All these findings results into the VTC of Figure 5.3.

5.3 Simulation

Supply voltages and parameters employed in the simulations are with respect to ITRS [3] for under 50 nm gate length devices. The V_{DD} is 0.7 V. The work functions of the gate electrodes are fixed at 4.5 eV to attain wanted V_{th} value. The simulated model for the charge carriers transport is the drift-diffusion model in Sdevice of Sentaurus. For mobility, basic model is taken, that includes the impact of high-field velocity simulation, dependency of the doping and of transverse field. The silicon band gap narrowing model that concludes the intrinsic carrier

concentration is actuated. The arrangement of the device equations are done self-reliably on the discrete mesh in an iterative manner. The Poisson mathematical statement, continuity, and the distinctive thermal and energy equations are built-in the simulation [26].

5.4 Results and Discussion

The overall shape of the voltage-transfer characteristic of the static CMOS inverter was derived, as were the values of V_{OH} and V_{OL} (V_{DD} and GND, respectively). It remains to determine the precise values of V_M, V_{IH}, and V_{IL} as well as the noise margins.

For the time we design a gate for normal operative condition and typical device parameters, we should always know that the initial operating temperature can be in a very large range, and that the device parameters after construction might deviate from the nominal values we used in our design optimization process. Fortunately, the dc characteristics of the static CMOS inverter turn out to be rather insensitive to these variations, and the gate remains functional over a wide range of operating conditions. To further confirm the assumed robustness of the gate, we have re-simulated the voltage transfer characteristic by replacing the nominal devices by their worst- or best-case incarnations. Two corner-cases are plotted in Figure 5.4: a better-than-expected NMOS combined with an inferior PMOS in case of DG CMOS, and the opposite scenario in SG CMOS. Comparing the resulting curves with the nominal response shows that the variations mostly cause a shift in the switching threshold, but that the operation of the

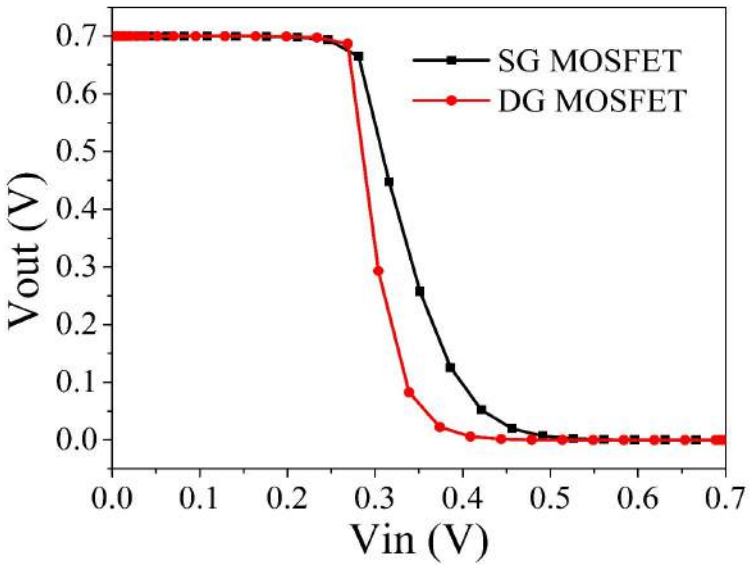


Figure 5.4: Voltage Transfer Characteristics of SG and DG CMOS

gate is by no means affected. This robust behavior that ensures functionality of the gate over a wide range of conditions has contributed in a big way to the popularity of the static CMOS gate.

5.5 Summary

The static CMOS inverter associate a pull-up PMOS section with a pull-down NMOS device. The PMOS is normally made wider than the NMOS due to its inferior current-driving capabilities. The gate has an almost ideal voltage-transfer characteristic. The logic swing is not a function of the transistor sizes but is equal to the supply voltage. The noise margins of a symmetrical inverter (where PMOS and NMOS transistor have equal current driving strength) approach $V_{DD}/2$. Fanout does not affect the steady-state response.

It is noted that the DG CMOS has better NMOS along with inferior PMOS whereas SG CMOS has better PMOS and inferior NMOS as noticed from the static behavior of the CMOS. Keeping the load capacitance small is the most effective means of implementing high-performance circuits. Transistor sizing may help to improve performance as long as the delay is dominated by the extrinsic (or load) capacitance of fanout and wiring. The dynamic power consumed in charging power dominates the dissipation and discharging the load capacitor. The dissipation is proportional to the action in the network. Scaling the technology is an effective means of reducing the area, propagation delay and power consumption of a gate. The impact is even more striking if the supply voltage is scaled simultaneously.

Chapter 6

Conclusions And Future Work

6.1 Conclusions

This research focuses on the ongoing SOI MOSFETs which are currently used in I-series microprocessors of INTEL. A comparison is also made between various models to analyze which one is suitable for HP or LSTP applications.

The UT-SDOI DG shows a higher drive current and lower DIBL than it's counterpart UT-SDOI SG even maintaining a constant I_{off}. The on-off current ratio for SDOI DG increases around a factor of 4 than SDOI SG in case of NMOS and a factor of 3 in case of PMOS case. From all analysis UT-SDOI DG MOSFET has potential to meet the ITRS roadmap for 22 nm technology generation and below this node with considerable amount of design adaptability for HP and LOP devices are achievable.

We have optimized the gate underlap length (L_{un}) of both DG and FinFET, to demonstrate that L_{un} can be suitably chosen for HP or LOP applications. When underlap length increases, an improvement in P.D. occurs but with the compensation of high delay. Thus, it is needed to be careful while choosing L_{un}. There is an improvement in I_{on}/I_{off}, SS, L_{SD} and P.D. can be observed with increase in L_{un}. FinFET demonstrates better results in case of L_{SD}, P.D. and intrinsic delay over DG MOSFET. Among DG and FinFET, the former one gives higher current drivability, while the successive one shows the betterment in EDP and delay.

In case when we have introduced the III-V materials in the channel then from the results, we have obtained that taller fins are required for higher current drivability and narrower fins are required for higher immunization to SCEs. By thinning the W_{Fin}, we can able to make the FinFET free from substrate related effects which further improves the energy consumption, power dissipation, and SS of the device.

In case of H_{Fin} variation, H_{Fin}=0.6×L_g case shows the optimum device performances in terms of gain and maximum frequency of operation. By thinning the WFin, FinFET can be freed from substrate related effects which further improves the A_V, V_{EA}, and R_0 of the device. The Trigate (AR=1) shows a tremendous improvement in delay of the device because of higher I_{eff}. However, FinFETs (AR<1) and Planar MOSFETs (AR>1) predict desirable improvements in power dissipation and f_T.

The PMOS is normally made wider than the NMOS due to its inferior current-driving capabilities. It is noted that the DG CMOS has better NMOS along with inferior PMOS whereas SG CMOS has better PMOS and inferior NMOS as noticed from the static behaviour of the CMOS. Scaling the technology is an effective means of reducing the area, propagation delay and power consumption of a gate.

6.2 Future Scope

- New materials like BeO_2, Tm_2O_3 etc. can be used in place of existing insulator SiO_2 which provide better insulation by taking care of the EOT.
- Temperature effects can be studied on the various structures discussed in this research in order to find the value of a particular operating point at

which the characteristics of the device are not affected by the variation of temperature known as temperature compensation point.

- Heavy ion effects can be studied in the aforesaid structures like alpha, beta and gamma particles due to which logic of the operation can go wrong.
- Dopingless concept can be applied in the above mentioned structures so that the fabrication process can be made easy.
- Static and dynamic characteristics of CMOS are discussed but the transient response analysis is done at a supply voltage of 1.5 V whereas the static analysis is done at 0.7 V. So, further investigation can be done on the various parameters of CMOS inverter in order to operate it fully on 0.7 V as given by ITRS report. Once a CMOS is ready fully then a lot of structures like NAND gate, multipliers, adders and microprocessors etc. can be implemented.

6.3 Publications

6.3.1 Journal

1. S. K. Mohapatra, K. P. Pradhan, **D. Singh**, and P. K. Sahu, "The Role of Geometry Parameters and Fin Aspect Ratio of sub-20nm SOI-FinFET: An Analysis towards Analog and RF Circuit Design," Nanotechnology, IEEE Transactions on, vol. 14, no. 03, pp. 1-9, May 2015.

6.3.2 Conferences

1. S. Panda, P. K. Sahu, **D. Singh**, K. P. Pradhan, and S. K. Mohapatra, "Performance comparison between ultrathin body (UTB) single and double gate MOSFETs," in International Conference on Microelectronics, Communication and Computation, San Diego, USA. (**Best Paper Award**), Feb 2015, pp. 1-4.

2. **D Singh**, K P Pradhan, S K Mohapatra, P K Sahu, "Optimization of Underlap Length for DGMOSFET and FinFET", International Conference, ICRTC, March 12-13, 2015.

3. K P Pradhan, **D Singh**, S K Mohapatra, P K Sahu, "Assessment of III-V FinFETs at 20 nm node: A Process variation analysis", International Conference, ICRTC, March 12-13, 2015.

4. S. K. Mohapatra, K. P. Pradhan, P. K. Sahu, **D. Singh**, and S. Panda, "Ultra-Thin Si Directly on Insulator (SDOI) MOSFETs at 20 nm gate length," in Proceedings of IEEE International Conference on High Performance Computing and Applications (ICHPCA), Bhubaneswar, Odisha, India, Dec 2014, pp. 1-4.

5. **D. Singh**, S. Panda, S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Static performance analysis on UTB-SG and DG MOSFETs with Si and III-V channel materials," in Proceedings of IEEE International Conference on

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6. **D. Singh**, S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Variation study of process parameters in Trigate SOI-FinFET," in India Conference (INDICON), 2014 Annual IEEE, Dec 2014, pp. 1-4.

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