# ANALYSIS AND DESIGN OF A SINGLE ENDED RESONANT RESET FORWARD CONVERTER

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# ANALYSIS AND DESIGN OF A SINGLE ENDED RESONANT RESET FORWARD CONVERTER

*Dissertation submitted to the*

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*in partial fulfillment of the requirements of*

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*in*

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*by*

***Abhirup Pal***

(Roll Number: 214EE5263) *under*

*the supervision of*

***Dr. Susovon Samanta***


May, 2016

Department of Electrical Engineering

**National Institute of Technology**

**R o u r k e l a**

Electrical Engineering Department
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# CERTIFICATE OF EXAMINATION

May 18, 2016

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Title of Dissertation: Analysis and Design of a single-ended Resonant Reset Forward Converter

We the below signed, after checking the dissertation mentioned above and the official record book (s) of the student, hereby state our approval of the dissertation submitted in partial fulfillment of the requirements of the degree of Doctor of Philosophy in Computer Science and Engineering at National Institute of Technology Rourkela. We are satisfied with the volume, quality, correctness, and originality of the work.

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May 18, 2016

# Supervisor's Certificate

This is to certify that the work presented in this dissertation entitled *"Analysis and Design of a single ended Resonant Reset Forward converter"* by "*Abhirup Pal*", Roll Number *214EE5263*, is a record of original research carried out by him/her under my supervision and guidance in partial fulfillment of the requirements of the degree of *Master of Technology* in *Electrical Engineering*. Neither this dissertation nor any part of it has been submitted for any degree or diploma to any institute or university in India or abroad.

Susovon Samanta

# Dedicated to

My ever caring and lovely Father, Tapan Kumar Pal
My ever worried and beautiful mother, Soma Pal
My forever best pals Nilayan Chattopadhyay, Saptarshi Mitra, Soumik Biswas, Suvradeep Mukherjee and Prithul Saha

# Declaration of Originality

I, Abhirup Pal, Roll Number 214EE5263 hereby declare that this dissertation entitled "*Analysis and Design of a single ended Resonant Reset Forward converter"* represents my original work carried out as a postgraduate student of NIT Rourkela and, to the best of my knowledge, it contains no material previously published or written by another person, nor any material presented for the award of any other degree or diploma of NIT Rourkela or any other institution. Any contribution made to this research by others, with whom I have worked at NIT Rourkela or elsewhere, is explicitly acknowledged in the dissertation. Works of other authors cited in this dissertation have been duly acknowledged under the section "Bibliography". I have also submitted my original research records to the scrutiny committee for evaluation of my dissertation.

I am fully aware that in case of any non-compliance detected in future, the Senate of NIT Rourkela may withdraw the degree awarded to me on the basis of the present dissertation.

May 17, 2015
NIT Rourkela

*Abhirup Pal*

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And last but not the least, my heartfelt gratitude to GOD who has made me what I am today.

# Abstract

A resonant reset forward converter was developed as one of the topologies of the forward converter because it offered the simplest technique of transformer core resetting. The resonant reset topology does not require any external passive components or any tertiary winding to facilitate the core reset but it utilizes the magnetizing inductance of the transformer and the parasitic capacitances of the devices to bring down the core flux to its initial position and hence avoids core saturation of the transformer, which is the principle working device in the converter from the point of view of electrical isolation and reproduction of good quality dc voltage at the output (or the load). The saturation of the transformer would have otherwise led to heavy inrush current resulting in huge losses and degradation in efficiency of the converter.

Thus in a low power dc-dc converter this resonant reset topology of the forward converter offers significant advantages. The small signal model of the converter which was proposed using the switch averaging method was validated using the software PSPICE and it gave perfect ripple free dc waveform at the output. The closed loop stage involved the development of a type IIIB controller to generate a sufficient phase margin and hence improve stability. The Optocoupler was also used in the feedback for the purpose of maintaining the electrical isolation and the pole which it generated (due to Miller's capacitance) was compensated by manually placing a combination of a parallel resistor and capacitor at the output of the collector terminals of the transistor of the Optocoupler. Finally the hardware developments were done for the voltage mode controlled feedback loop using IC UC 3525A which gave satisfactory results for various load tests and desired input voltage fluctuations.

***Keywords: Resonant reset, magnetizing inductance, parasitic capacitance, small signal analysis, switch averaging, voltage mode controller, Optocoupler***

# CONTENTS

# CHAPTER 1
# INTRODUCTION

The Forward converter is one of the most important industry workhorses now-a-days owing to its robust design. It is basically a modification of the buck converter with galvanic isolation, which is being provided by the transformer in the forward path. Since any stable and robust design requires an inherent feedback, the feedback path must also be isolated to maintain the continuity of galvanic isolation otherwise the entire concept of isolation will be lost and a fault in a primary side of the converter would invariably result in a huge current in the secondary as well i.e. the load side will be overloaded and may burn out. This may lead to fatal injuries for any working personnel at the load side of the converter. Thus a well-designed forward converter finds widespread applications in space and military where payloads may be a camera, infra-red devices or sensors.

## 1.1 MOTIVATION OF THE PROJECT

The forward converter, owing to its extensive developments, has numerous topologies with each of them having its own advantages and disadvantages. The most intriguing problem of the forward converter is the core flux reset mechanism of the transformer, the failure of which may result in saturation and eventual burning out of the transformer. The idea was hence to select a particular topology which would satisfactorily reset the core and also minimize the losses in the various external components used to reset the transformer, since in a low wattage converter the losses incurred in the external passive components may account for a large part of the converter output hence degrading the efficiency. The selected topology must also

reduce the voltage stresses across the devices of the converter which will further enable us to reduce the rating of the switches and hence achieve cost reduction.

## 1.2 OBJECTIVE OF THE PROJECT

The objective of the project was to analyse in detail the working mode of the resonant converter, considering the effect of the parasitic capacitances (both distributed and lumped) on the resonant stage of the converter and finally arrive at a reset criteria for the converter. The small signal analysis also had to be carried out to remove any switching harmonics and simulations were to be performed on various platforms as MATLAB and PSPICE to validate the theoretical results.

## 1.3 PROBLEM STATEMENT

Problems were aplenty in designing the power stage of the converter. The first of them being the effect of the parasitic capacitances which led to huge voltage stresses across the devices and sometimes also inaccurate core-reset of the transformer. To understand their effects vividly the capacitances across the various devices were lumped into one, only across the switch. These gave considerably better results with reduction in the number of the modes. The next challenge lied in the design of the transformer since it was the principle most component in our converter and played a vital role in the reproduction of output voltages at the load side. The next difficulty was the addition of an extra pole in the transfer function of the converter which led to reduction in the phase margin and hence stability. Suitable measures thus had to be taken to compensate all those and form practical guidelines for the successful development of an end-to-end converter.

# CHAPTER 2

# TIME DOMAIN ANALYSIS

## 2.1 THE CONTEMPORARY FORWARD CONVERTER

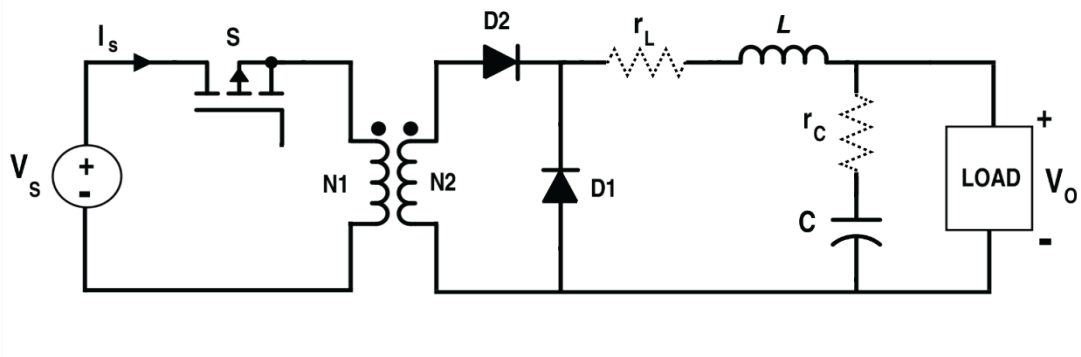



**Fig: A standard ideal Forward Converter**

The above forward converter is one of the simplest designs and does not take into account any of the non-linearity present in the switching devices used in the circuit.

When the switch S is closed by the application of a gate pulse the transformer stores energy and by transformer action the energy is being transferred to the secondary side or the load side.

During the off mode i.e. when the switch is not conducting the energy in the transformer dies down instantaneously as the transformer is considered ideal. The diode $D_1$ instantaneously switches off and the diode $D_2$ swings into conduction which now maintains the load current through it.

# PART A

## 2.2 ANALYSIS USING DISTRIBUTED CAPACITANCE

The practical world differs a lot from the theoretical sense. This is when parasitic capacitances are considered across the main switch (Mosfet) and the two diodes. Also it is a well-known fact that the semiconductor devices available in the market are never ideal i.e. there is a certain finite delay associated with turning ON and OFF of the devices which in turn enhances the complexity in understanding the dynamics of the converter model.

### 2.2.1 MODELOF THE WORKING CIRCUIT

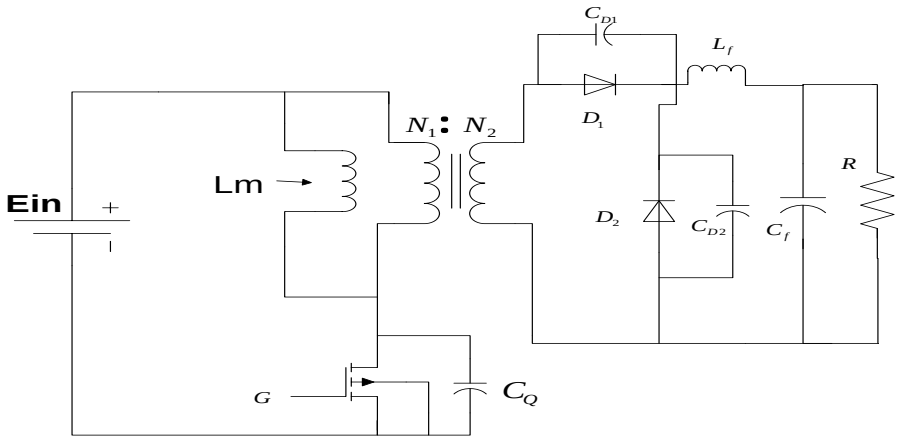



**Fig: Modified Circuit after introduction of parasitic capacitances**

### 2.2.2 ANALYSIS OF MODE 1 (0<t<$T_1$)

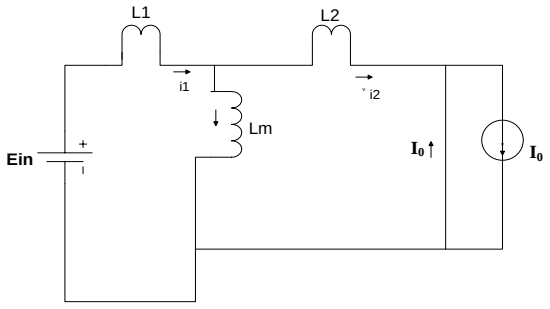



**Fig: Equivalent circuit of Mode 1**

**Description of the mode:**

In this mode both the diodes are conducting and the mode ends when the diode $D_2$ stops conducting and the parasitic capacitance forms across it.

**Mathematical Equations:**

$$i_m(t) = L_{l2} / L_l L_m Ein\ t + i_m(0)$$

$$T_1 = (I_0 - i_2(0)) L_l / Ein$$

## 2.2.3 ANALYSIS OF MODE 2 ($T_1$<t<$T_2$)

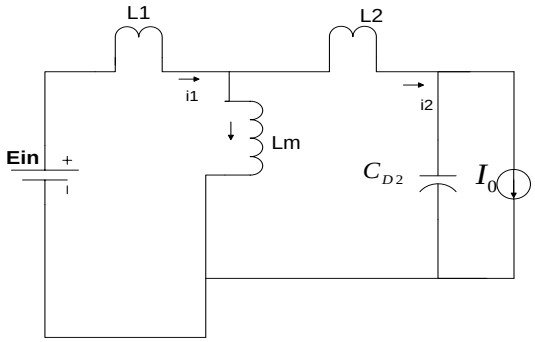



**Fig: Equivalent circuit of mode 2**

**Description of the mode:**

This is the main operating mode of our circuit and it continues till we switch off the gate pulse.

**Mathematical Equations:**

$$i_m(t) = Ein\sqrt{C_{D2} / L_l} / L_m\ t\ \sin\ w_B(t - t_1) + Ein\ / L_m(t - T_1) + i_m(0)$$

## 2.2.4 ANALYSIS OF MODE 3 ($T_2<t<T_3$)

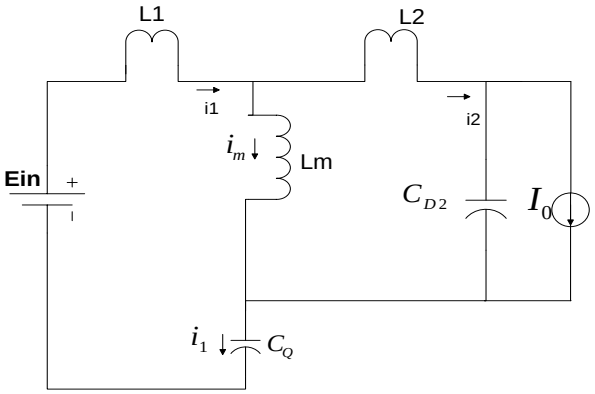



**Fig: Equivalent circuit of Mode 3**

**Description of the mode:**

This mode begins when the gate pulse is not present and ends at the time when the reverse bias across the diode $D_2$ is removed i.e. it starts conducting again.

**Mathematical Equations:**

$$i_m = EinC_Q / \sqrt{L_m(C_{D2}+C_Q)}\ \sin\ t / \sqrt{L_m C'}) \ - I_0$$

$$T_3 = T_2 + \pi / 2w$$

## 2.2.5 ANALYSIS OF MODE 4 ($T_3<t<T_4$)

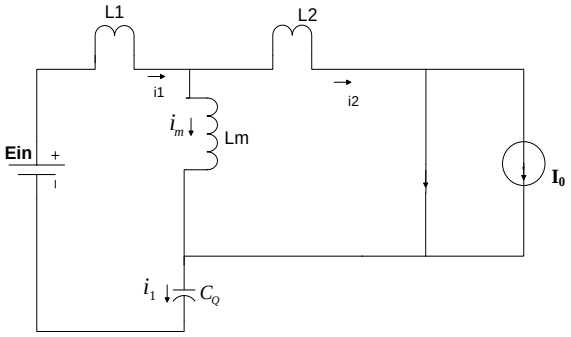



**Fig: Equivalent circuit of Mode 4**

**Description of the mode:**

Here both the secondary diodes conduct and finally it ends when the diode $D_1$ is reverse biased by the dropping resonating current formed by the L and C components of the circuit.

**Mathematical Equations:**

$$\boxed{i_2(\mathrm{t}) = X_E \cos[w_E(t-T_3)+Y_E] + \mathrm{i}_2(T_3) - i_1(T_3)}$$

## 2.2.6 ANALYSIS OF MODE 5 ($T_4<t<T_5$)

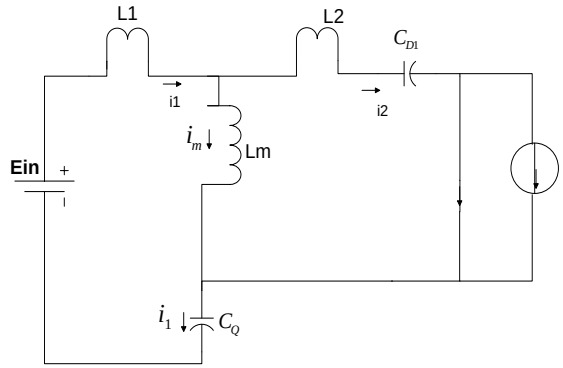



**Fig: Equivalent circuit of Mode 5**

**Description of the mode:**

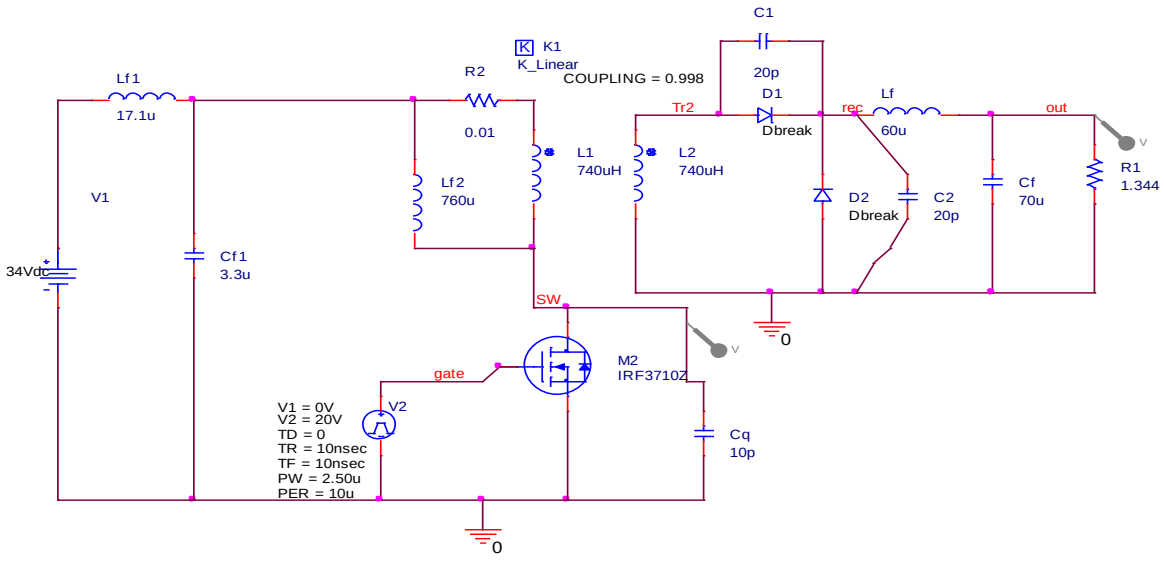
This mode is basically the principle OFF mode of our switching cycle and it continues till the reverse bias across the diode $D_1$ is removed.

**Mathematical Equations:**

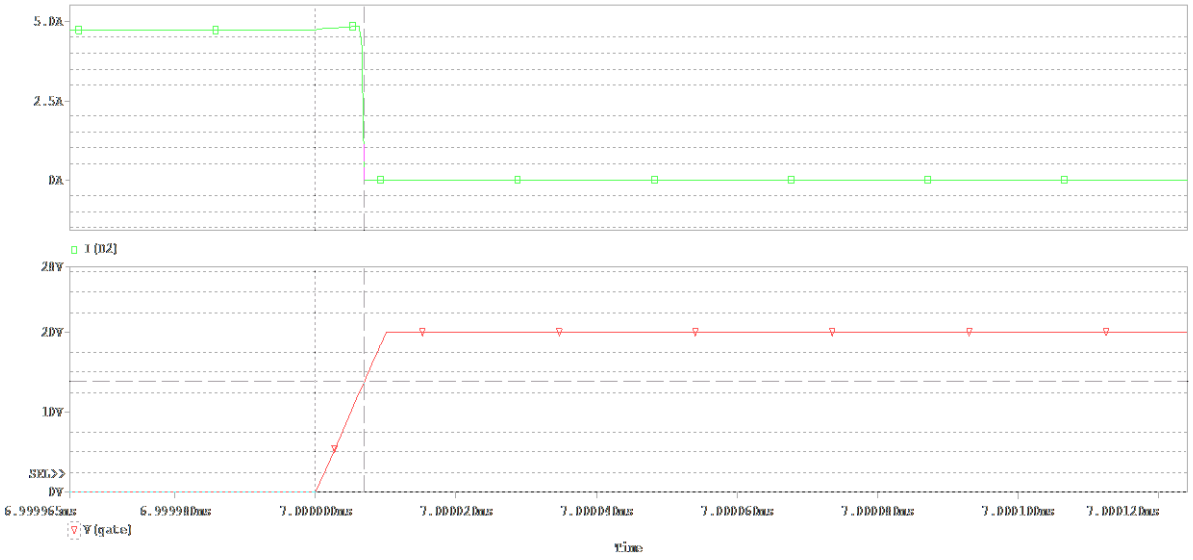
$$i_m(t) = i_m(T_4)\cos w_G(t) + [E_{in} - V_Q(T_4)]\sqrt{\frac{C'}{L_m}}\sin w_G(t)$$

# 2.2.7 PSPICE SIMULATION AND RESULTS

## 2.2.7.1 PSPICE SCHEMATIC



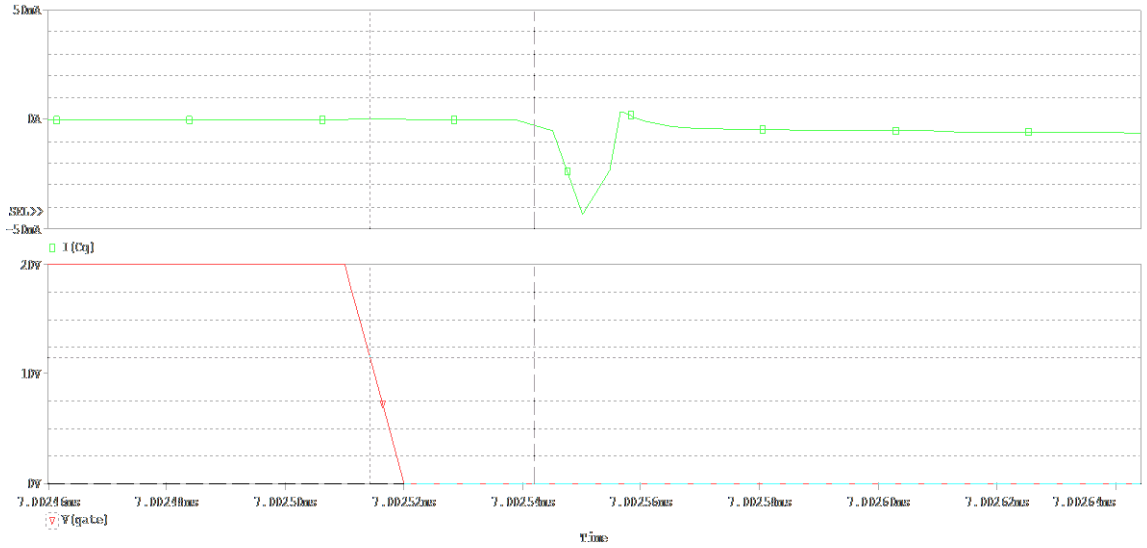
## 2.2.8.2 SIMULATION RESULT OF MODE 1




Mode duration (Practical): 8 nsecs

Mode duration (Theoretical): 10nsecs

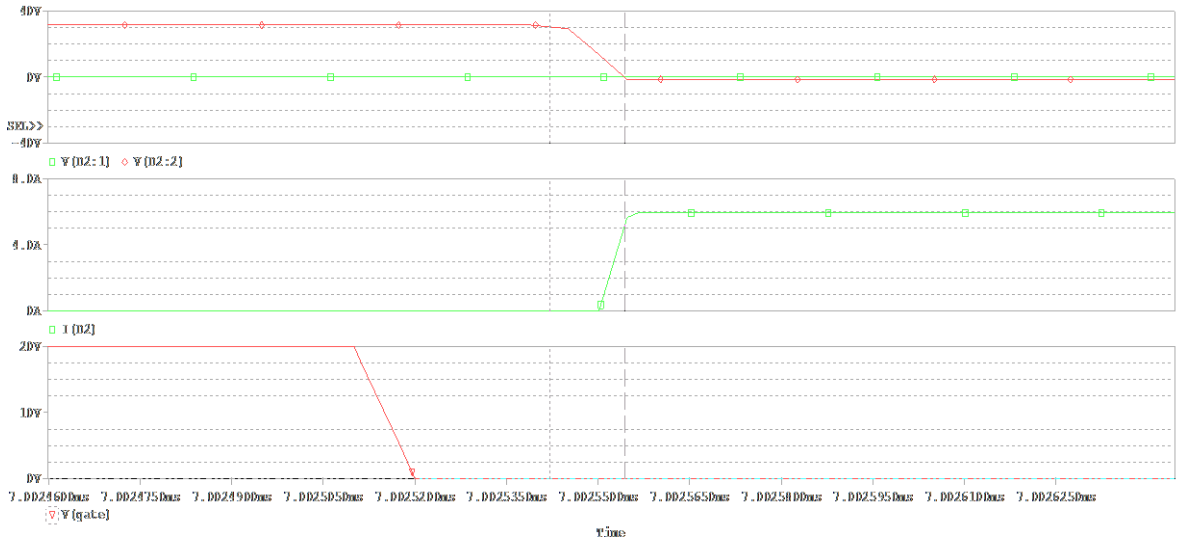
## 2.2.8.3 SIMULATION RESULT OF MODE 2




Mode duration (Practical): 2.835 micro secs

Mode duration (Theoretical): 2.6 micro secs

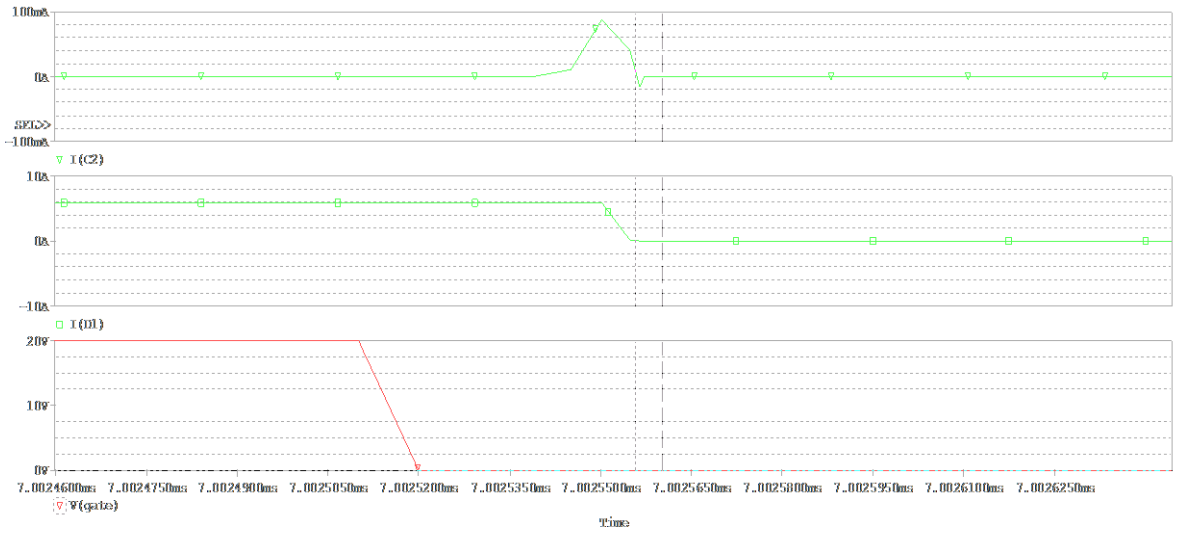
## 2.2.8.4 SIMULATION RESULT OF MODE 3



Mode duration (Practical): 16 nano secs

Mode duration (Theoretical): 15 nano secs

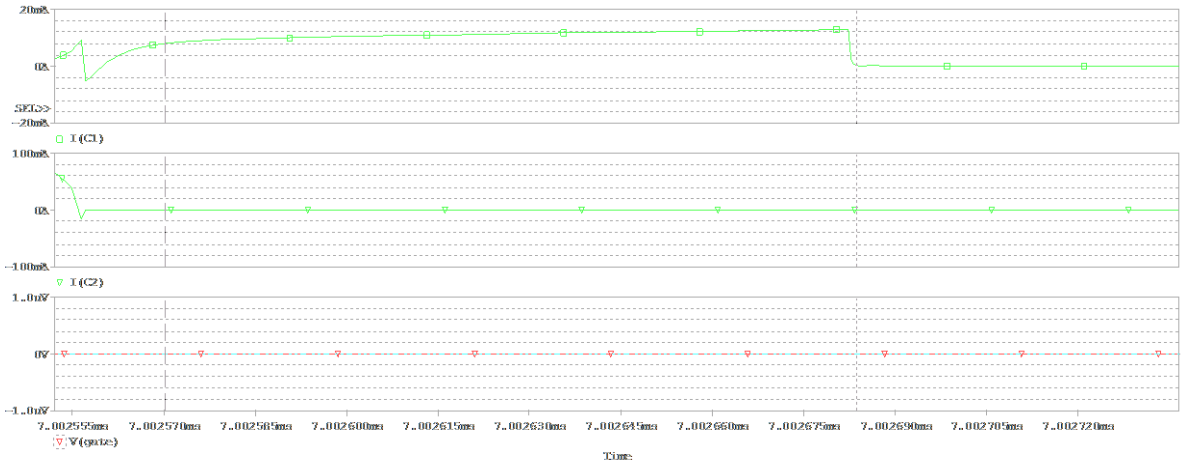
## 2.2.8.5 SIMULATION RESULT OF MODE 4



Mode duration (Practical): 3.5 nano secs

Mode duration (Theoretical): 4.21 nano secs

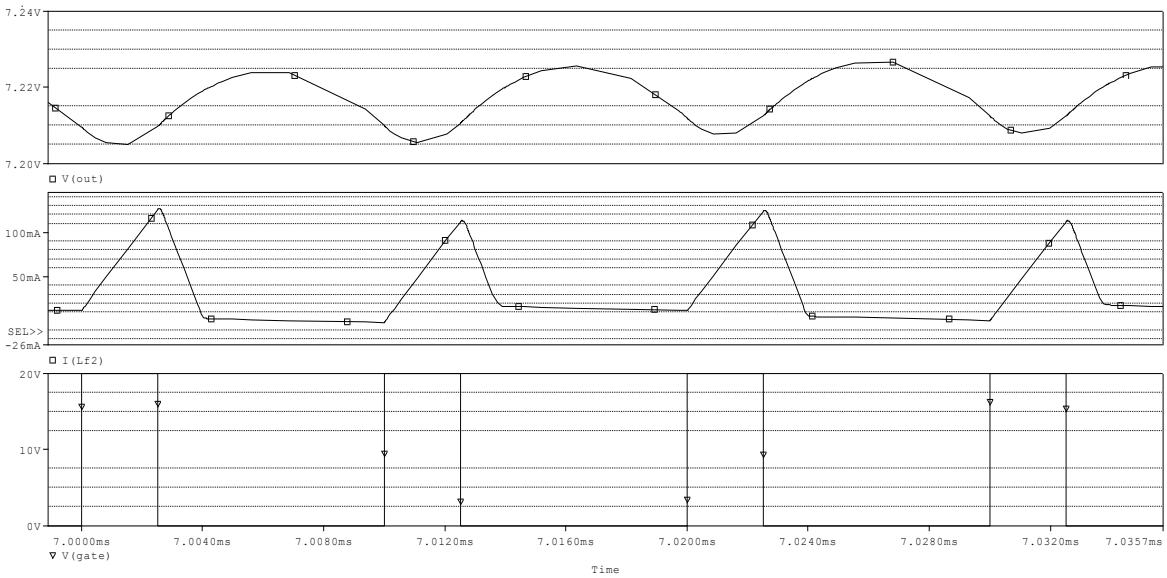
## 2.2.8.6 SIMULATION RESULT OF MODE 5




Mode duration (Practical): 1.31 micro secs

Mode duration (Theoretical): 1.5 micro secs

## 2.2.8.7 SIMULATION RESULT OF OUTPUT VOLTAGE AND MAGNETIZING CURRENT




**a) Output Voltage; b) Magnetising Current of the Transformer; c) Gate Pulse**

# CHAPTER 3

# DYNAMICS AND CONTROL

To understand the dynamics of the converter in a much deeper and intricate manner the small signal analysis is required to be carried out though it is true that the time domain analysis gives much more accurate results.

There are various methods by which the small signal analysis can be carried out of which the basic averaging method is the most convenient and relatively easy to analyse.

## 3.1 AC EQUIVALENT CIRCUIT MODELLING USING BASIC AVERAGING METHOD

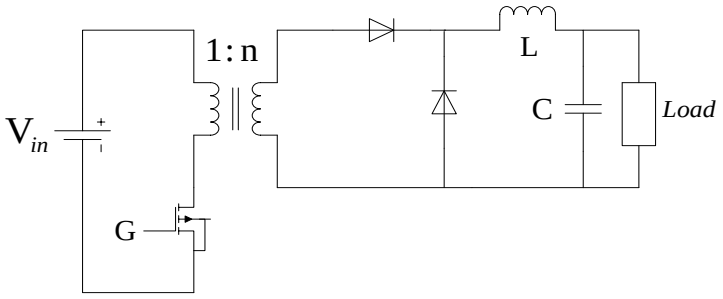



**Fig: A standard ideal Forward Converter**

When the Switch is ON:

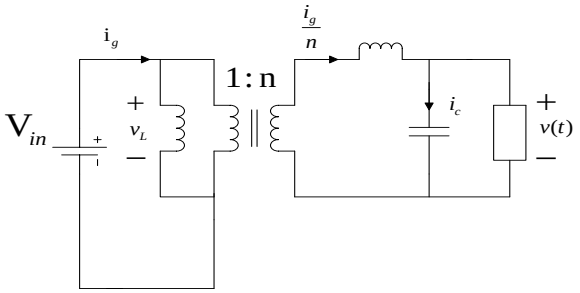



**Fig: Equivalent circuit when the switch is in forward conduction**

$$v_L(t) = V_g$$

$$i_c(t) = \frac{i_g}{n} - \frac{v(t)}{R} = \frac{i(t)}{n} - \frac{v(t)}{R}$$

$$i_g(t) = i(t)$$

When the Switch is OFF:

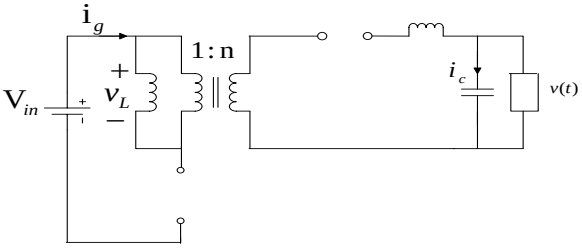



**Fig: Equivalent circuit when the switch is reverse blocking mode**

$$v_L(t) = -V_g$$

$$i_c(t) = \frac{i(t)}{n} - \frac{v(t)}{R}$$

$$i_g(t) = 0$$

Performing Averaging over one switching period for the above equations gives us:

For the voltage across magnetising branch of the transformer:

$$< v_L(\mathrm{t}) >_{T_s} = d(\mathrm{t})\,\mathrm{V}_g + d'(\mathrm{t})(-\mathrm{V}_g)$$

$$\boxed{< v_L(\mathrm{t}) >_{T_s} = \mathrm{V}_g[d(\mathrm{t}) - d'(\mathrm{t})] = \mathrm{V}_g[2d(\mathrm{t}) - 1]}$$

Averaging the capacitor waveforms:

$$< i_c(\mathrm{t}) >_{T_s} = (d + d')[\frac{i(\mathrm{t})}{n} - \frac{v(\mathrm{t})}{R}]$$

$$\boxed{< i_c(\mathrm{t}) >_{T_s} = [\frac{i(\mathrm{t})}{n} - \frac{v(\mathrm{t})}{R}]}$$

Averaging the input current waveform:

$$\boxed{i_g(\mathrm{t}) = d(\mathrm{t})i(\mathrm{t}) + 0 = d(\mathrm{t})i(\mathrm{t})}$$

Writing down all the above equations:

$$L\frac{d < i(\mathrm{t}) >_{T_s}}{dt} = 2v_g < d(\mathrm{t}) >_{T_s} - v_g \ldots\ldots\ldots (1)$$

$$C\frac{d < v(\mathrm{t}) >_{T_s}}{dt} = \frac{< i(\mathrm{t}) >_{T_s}}{n} - \frac{< v(\mathrm{t}) >_{T_s}}{R} \ldots\ldots\ldots (2)$$

$$< i_g(\mathrm{t}) >_{T_s} = d(\mathrm{t}) < i(\mathrm{t}) >_{T_s} \ldots\ldots\ldots\ldots (3)$$

Perturbing around a steady state operating point we have:

$$v_g = V_g + v_g \quad ; \quad i_g(\mathrm{t}) = \mathrm{I}_g + i_g$$

$$d(\mathrm{t}) = \mathrm{D} + d \quad ; \quad d'(\mathrm{t}) = \mathrm{D}' - d'$$

$$i(\mathrm{t}) = \mathrm{I} + \hat{i} \quad ; \quad v(\mathrm{t}) = \mathrm{V} + \hat{v}$$

From equation (1) we have:

$$L\frac{d}{dt}[I + \hat{i}] = 2[V_g + v_g][D + d] - [V_g + v_g]$$

$$L\left(\frac{dI}{dt}+\frac{d\hat{i}}{dt}\right)=2[V_g D]-[V_g]+(2V_g\, d+2Dv_g)-v_g$$

Taking the small signal terms only we have: $\boxed{L\frac{d\hat{i}}{dt}=2V_g d+2Dv_g-v_g}$ $\{\because L\frac{dI}{dt}=0\}$

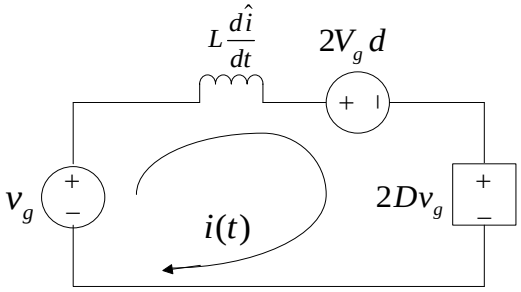



**Fig: Equivalent small signal circuit after averaging the inductor voltage waveform**

Again from equation (2) we have:

$$C\frac{d}{dt}[V+\hat{v}]=\left(\frac{I+\hat{i}}{n}\right)-\left(\frac{V+\hat{v}}{R}\right)$$

$$C\left[\frac{dV}{dt}+\frac{d\hat{v}}{dt}\right]=\left(\frac{I}{n}-\frac{V}{R}\right)+\left(\frac{\hat{i}}{n}-\frac{\hat{v}}{R}\right)$$

Taking the small signal terms only we have: $\boxed{C\frac{d\hat{v}}{dt}=\frac{\hat{i}}{n}-\frac{\hat{v}}{R}}$

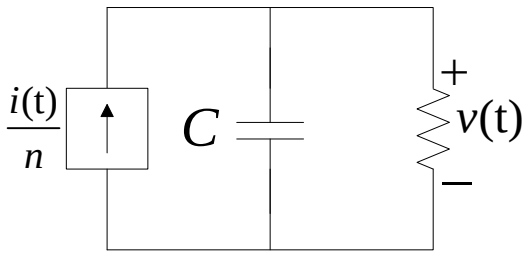



**Fig: Equivalent small signal circuit after averaging the capacitor waveform**

From equation (3) we have:

$$I_g+i_g=(D+d)(I+\hat{i})$$

Taking the small signal terms only we have: $\boxed{i_g = Id + D\hat{i}}$

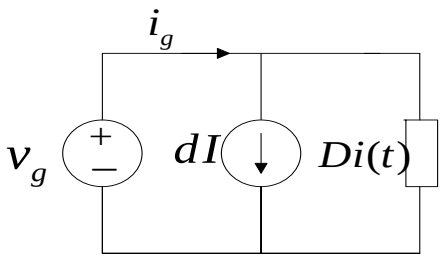



**Fig: Equivalent small signal circuit after averaging the input current**

Combining all the models we have the required small signal ac model as shown:

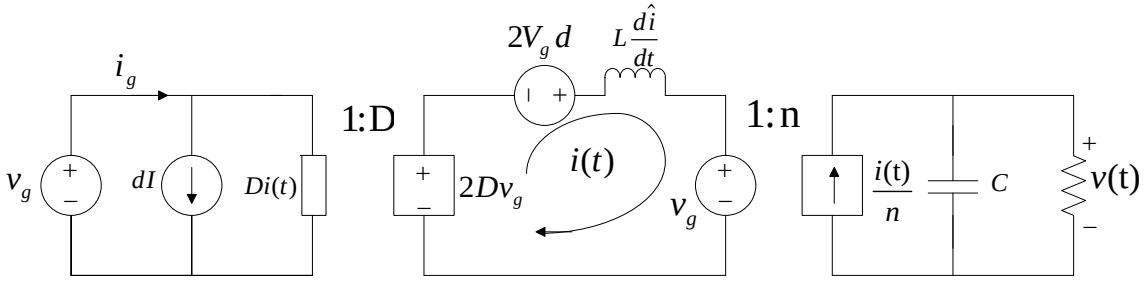



**Fig: Resulting Small signal equivalent model after combining all the above individual models**

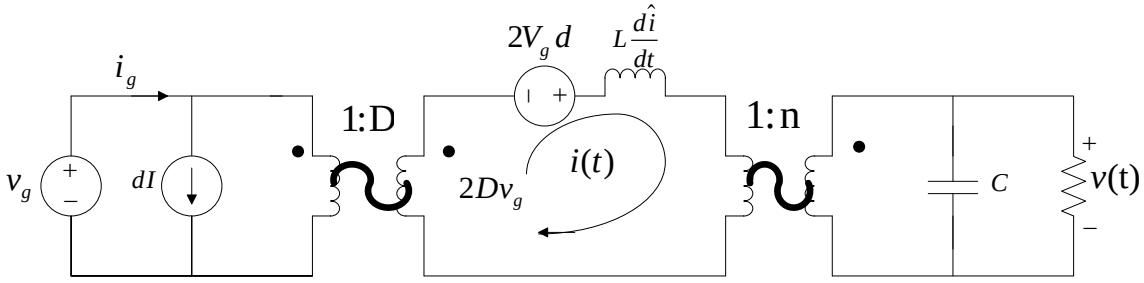



**Fig: Combination of dependent sources into effective ideal transformer leading into the final small signal ac model**

The resultant transfer function of the above model can be obtained by setting the input voltage source to zero and then applying superposition theorem, which is given as below:

$$G_{vd} = \frac{V}{nd}\left(\frac{1}{1 + s\frac{L}{R} + s^2 LC}\right)$$

# 3.3 PSPICE SIMULATION AND RESULTS

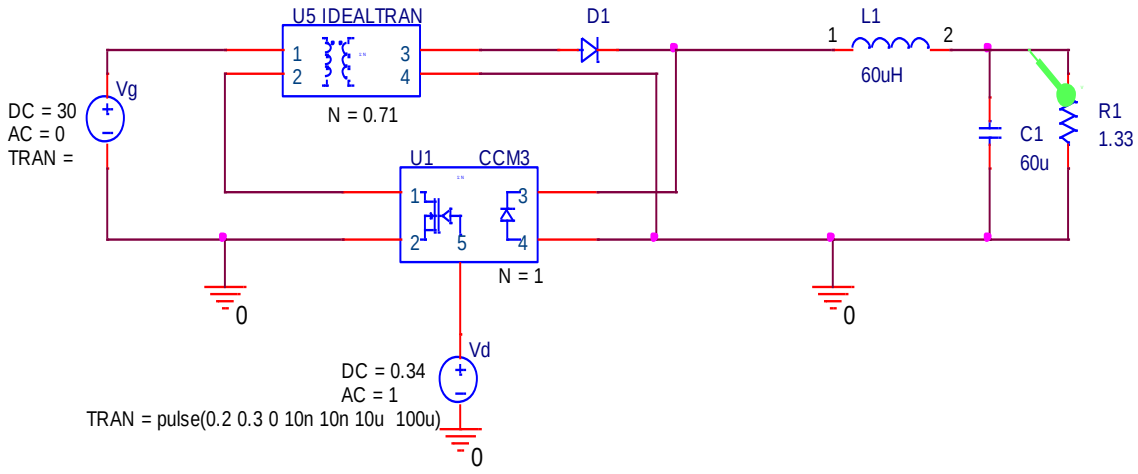



**Fig: Pspice schematic using small signal method**

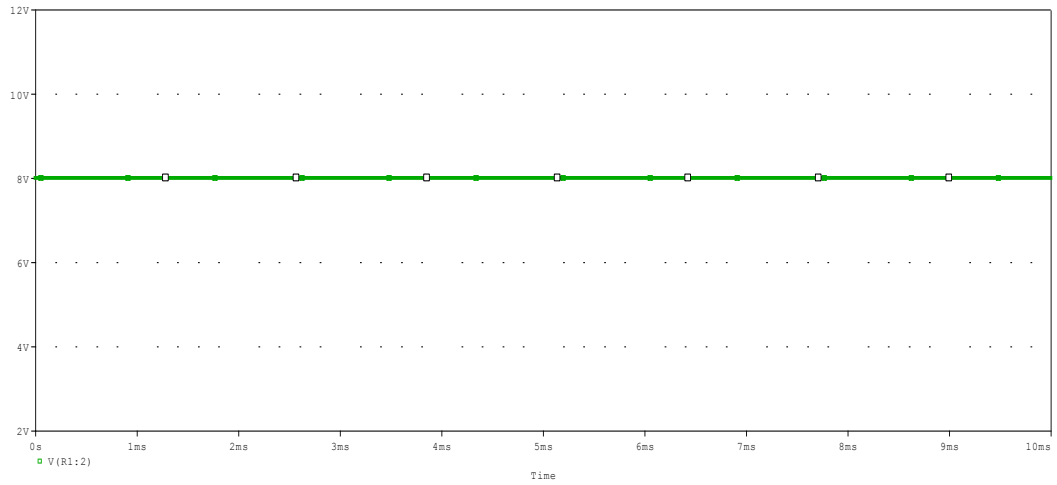



**Fig: Output voltage with switching harmonics eliminated**

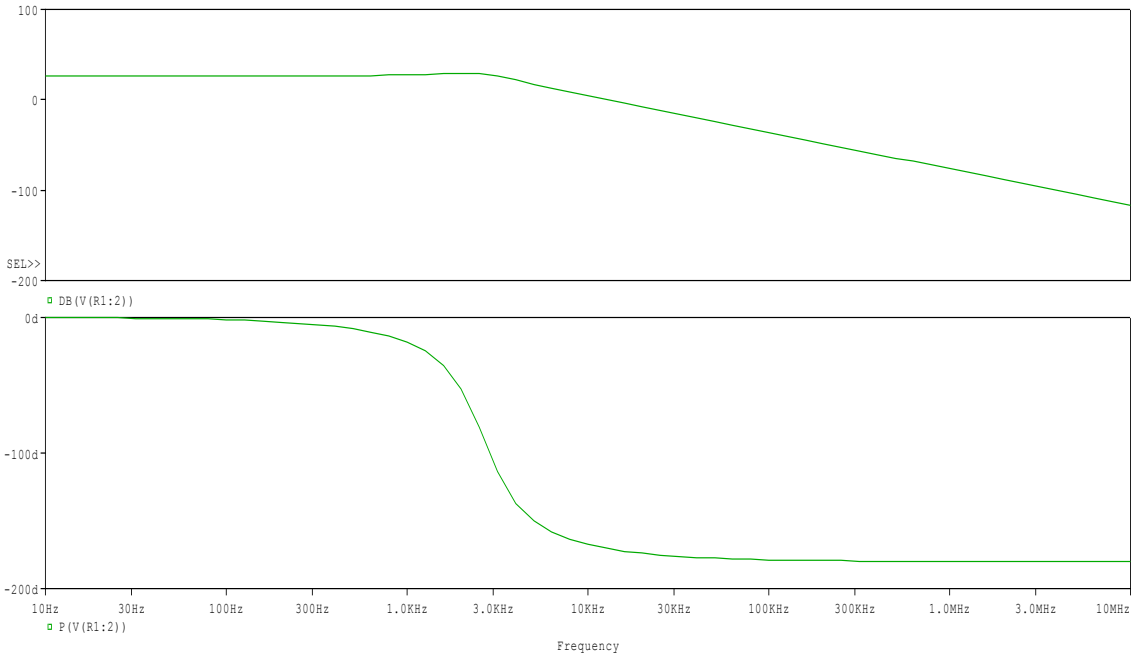



**Fig: Bode Plot of open loop Plant**

# CHAPTER 4
# CONTROLLER DESIGN AND FEEDBACK ISOLATION

## 4.1 DESIGN OF CONTROLLER

The open loop frequency analysis of the forward converter gave a Phase Margin of 12.9 degrees only at a gain cross-over frequency of 26.91 kHz. To design a stable closed loop robust system we need to improve the phase margin to at least 45 degrees, if not more. Thus is necessitated a lead compensator which will effectively boost the phase margin of our plant at our desired bandwidth. It is also to be remembered that higher phase margin and greater bandwidth are not possible at the same time as the product of the B.W and time is a constant i.e. we have to make a compromise between the two.
Addition of an integral controller along with the lead controller will also stabilise the steady state error. Now-a-days ceramic capacitors are used in all output filters because of their low cost, abundance of supply, etc. This ESR of ceramic capacitor is also very low which keeps the output ripple voltage very low as well. However this ESR of the output filter capacitor introduces a zero in the $G_{vd}$ model of our plant and the transfer function is modified as:

$$G_{vd(\mathrm{modified})} = \frac{R(1+sC\,ESR)}{s^2LC(R+ESR)+s(L+RC\,ESR)+R}\left(\frac{V}{nd}\right)$$

$$G_{vd} = \frac{V}{nd}\left(\frac{1}{1+s\frac{L}{R}+s^2LC}\right)$$

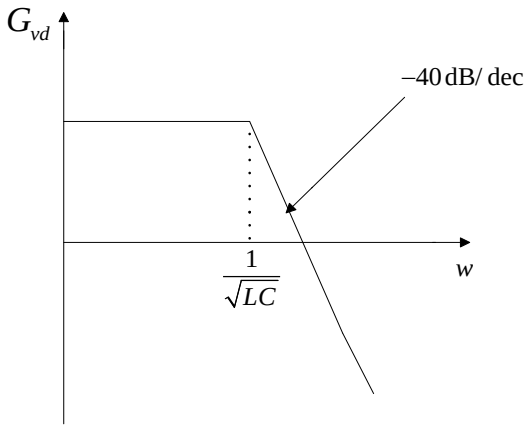



**Fig: Bode Plot of $G_{vd}$**

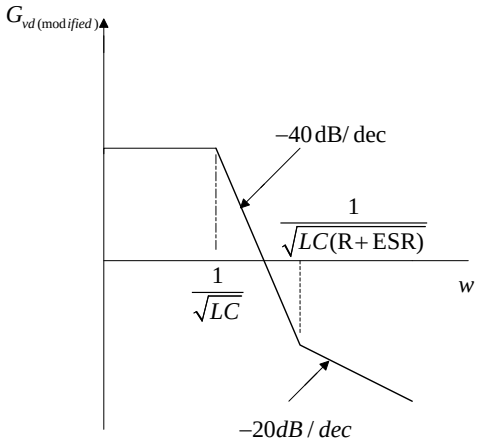



**Fig: Bode Plot of modified $G_{vd}$**

The slope of the loop gain should be -20dB/decade to ensure a stable system. This can be provided by a zero-pole pair. Thus the transfer function of the Type III compensator is as:

$$H(\mathrm{s}) = \frac{k(1+sC_2R_2)(1+sC_3(R_1+R_3))}{s(1+sC_1R_2)(1+sC_3R_3)}$$

and the structure is designed by using a combination of six passive elements:

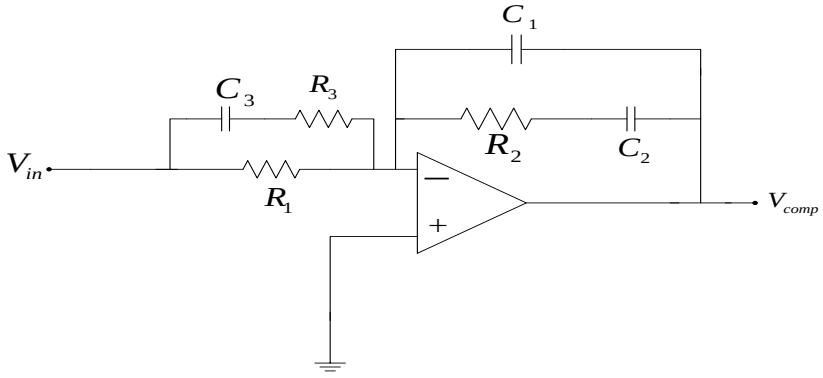



**Fig: Op-Amp implementation of Type III Compensator**

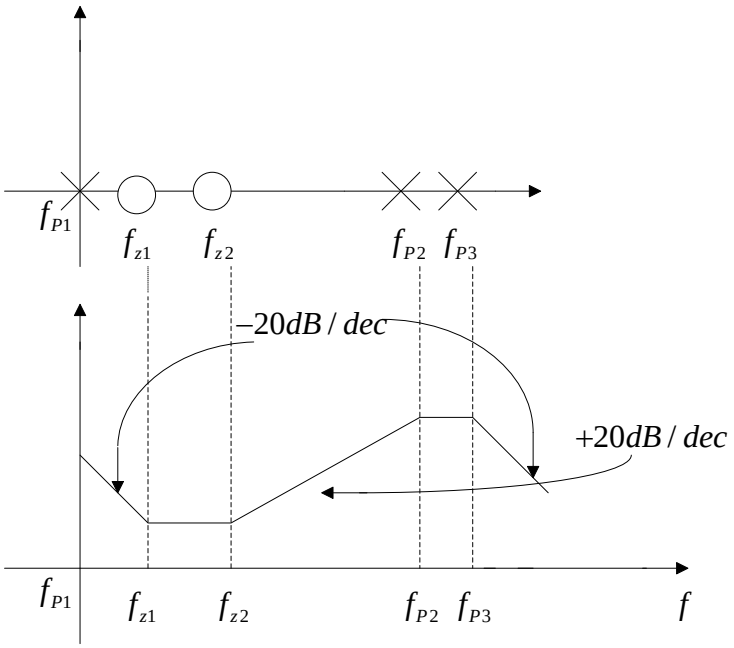



**Fig: Pole zero configuration and frequency response**

The first zero of the compensator $f_{Z1}$ compensates the phase lag of the pole which is present at the origin. The second zero of the compensator $f_{Z2}$ is to compensate for one of the double poles of the LC filter so that the slope of the resultant bode plot (plant+controller) is -20dB/decade . The second pole $f_{p2}$ of the compensator and zero of the ESR cancel each other and the third pole $f_{p3}$ provides more attenuation for frequency above $f_s/2$ i.e. 50 kHz.

The controller transfer function can be modified as:

$$H(\mathrm{s}) = \frac{k(1+\frac{s}{w_z})^2}{s(1+\frac{s}{w_p})^2}, where \ \mathrm{w}_z = \frac{1}{R_2C_2} = \frac{1}{R_2(\mathrm{C}_1+C_3)}; w_p = \frac{1}{R_3C_3} = \frac{1}{R_2C_{12}}$$

$$k = \frac{1}{R_1(\mathrm{C}_1+C_2)}; C_{12} = \frac{C_1C_2}{C_1+C_2}$$

Substituting s=jw for frequency domain analysis we have:

$$|H(jw)| = \frac{k\left|(1+j\frac{w}{w_z})^2\right|}{w\left|(1+j\frac{w}{w_p})^2\right|}$$

$$\underline{|H(jw)} = -90 + 2\tan^{-1}\frac{w}{w_z} - 2\tan^{-1}\frac{w}{w_p}$$

$$= -90 + 2(\tan^{-1}\frac{w}{w_z} - \tan^{-1}\frac{w}{w_p}) = -90 + 2(\tan^{-1}\frac{\frac{w}{w_z} - \frac{w}{w_p}}{1+(\frac{w}{w_z})(\frac{w}{w_p})})$$

$$= -90 + 2\tan^{-1}\frac{w(w_p - w_z)}{w^2 + w_p w_z}$$

*where,* $\phi_v(\mathrm{w}) = 2\tan^{-1}\frac{w(w_p - w_z)}{w^2 + w_p w_z}$

For maximum value of $\phi_v(\mathrm{w})$, differentiating w.r.t w gives us:

$$\frac{d\phi_v(\mathrm{w})}{dw} = 0 \Rightarrow at\ w = \sqrt{w_z w_p} = w_m$$

$$\therefore \phi_v(\mathrm{w})_{\max} = 2\tan^{-1}\frac{w_m(w_p - w_z)}{{w_m}^2 + w_p w_z} = 2\tan^{-1}\frac{(w_p - w_z)}{2\sqrt{w_p w_z}}$$

*Let* $k_1 = \frac{w_p}{w_z} \Rightarrow$ ratio of distance between the poles and zeros, called separation factor

Substituting we have, $\phi_v(\mathrm{w})_{\max} = 2\tan^{-1}\frac{k_1 - 1}{2\sqrt{k_1}}$

The main aim of using the controller is to boost the phase of the control loop. Thus we should know the value of $k_1$ for which the phase of $H(jw)$ is zero and accordingly we can next choose the value of k.

$$\underline{|H(jw)} = 0, when\ \tan^{-1}\frac{k_1 - 1}{2\sqrt{k_1}} = \frac{\pi}{4}$$

$$Solving: k_1 - 2\sqrt{k_1} - 1 = 0 \Rightarrow k_1 = 5.827$$

For value of $k_1 > 5.827$ we will get $|H(jw)|$ as positive, which is desired, since we want to boost the phase of the overall transfer function using type III compensator.

If k < 5.827 is selected phase lag will be introduced and this will be detrimental to our system as the Phase Margin will be further deteriorated.

Thus safely $k_1 > 6$

The required transfer function of the compensator becomes:

$$H(s) = \frac{k(1+sC_2R_2)(1+sC_3(R_1+R_3))}{s(1+sC_{12}R_2)(1+sR_3C_3)} = \frac{782(1+s(52.8u))(1+s(52.9u))}{s(1+s(4.51u)(1+s4.79u)}$$

$$H(jw) = \frac{782(1+\frac{w}{w_z})^2}{w(1+\frac{w}{w_p})^2} = \frac{782(1+\frac{w}{18.9k})^2}{w(1+\frac{w}{208.5k})^2}$$

## 4.1.1 MATLAB SIMULATION AND RESULTS

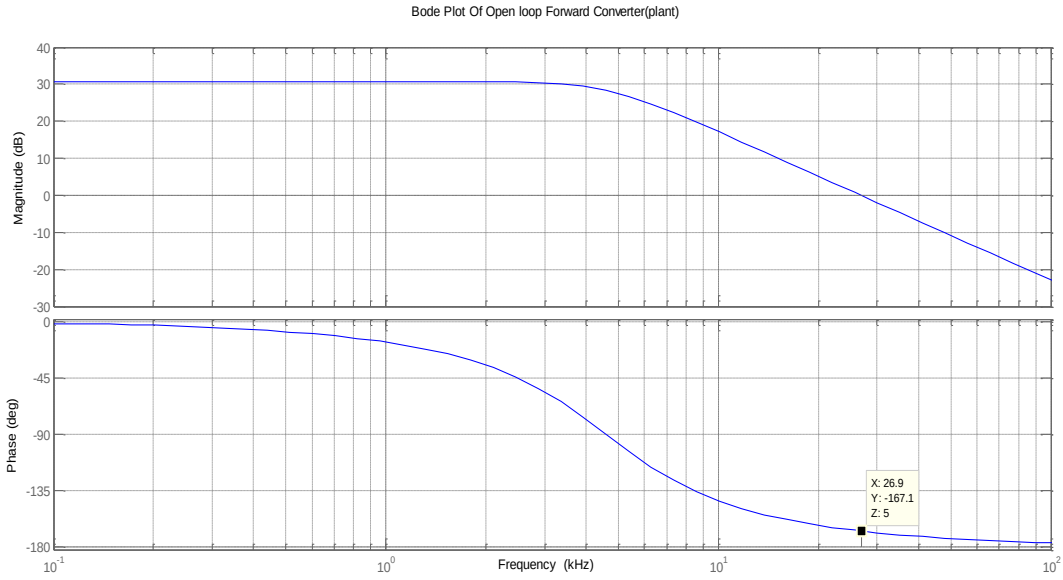



**Fig: Bode Plot of Open Loop Plant**

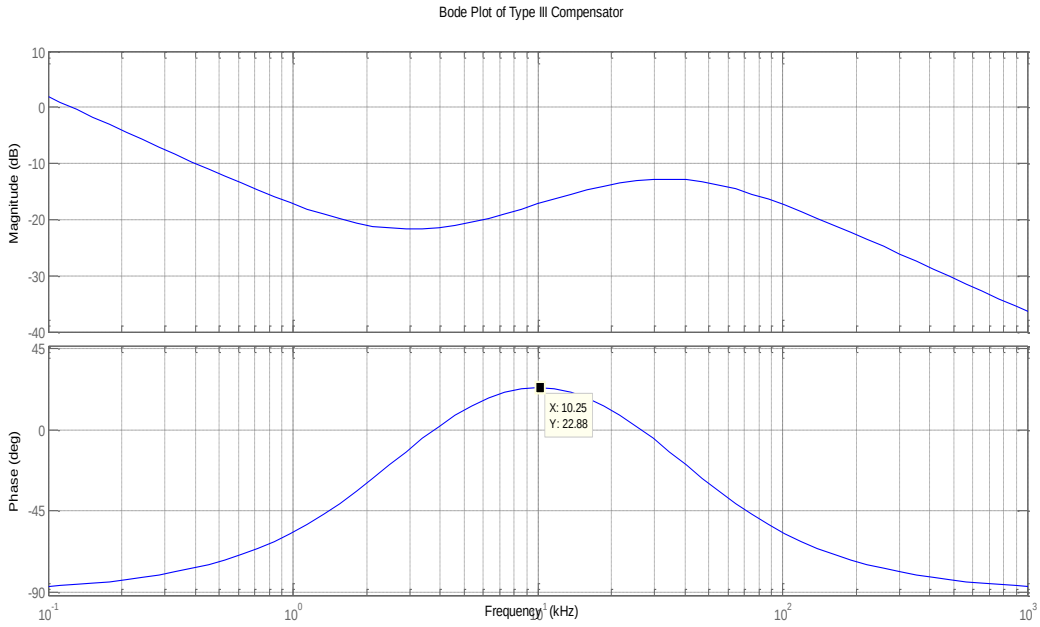



**Fig: Bode Plot of Type III compensator**

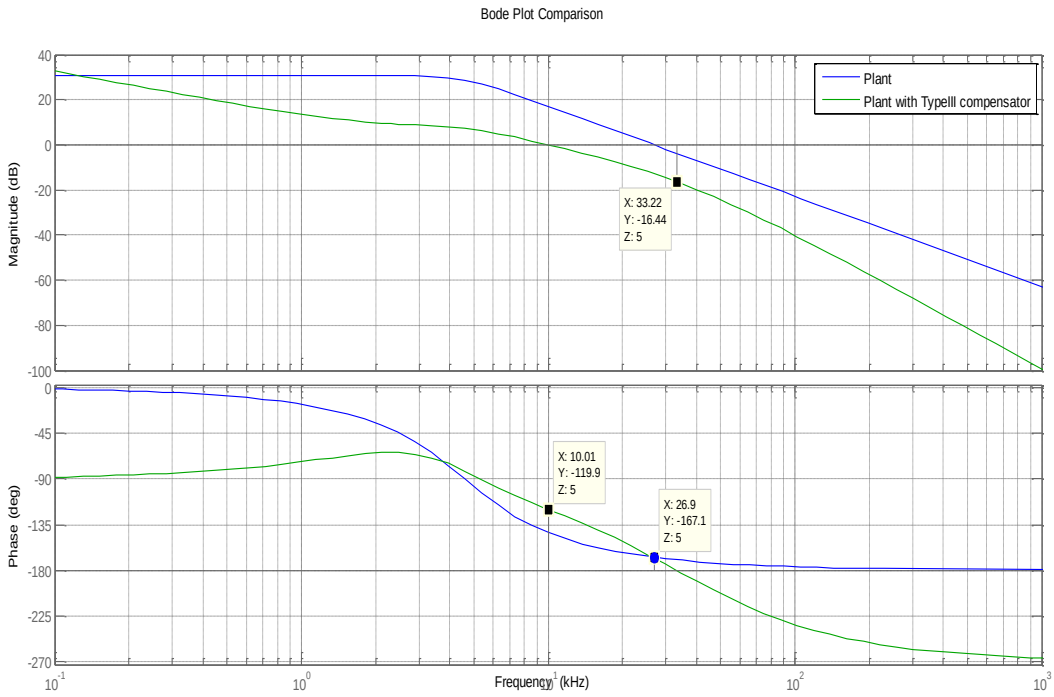



**Fig: Comparison of Bode Plot of Plant and Plant after compensation**

# 4.2 ISOLATION OF FEEDBACK

The most important aspect of the forward converter is the isolation provided by the transformer in the forward path which makes it a very useful one for use in space and military applications. But the galvanic isolation in the forward path by the transformer would be entirely lost if the feedback path is not isolated. This necessitated the use of an isolating device in the feedback also to serve the purpose of our isolation and restrict the propagation of any dangerous current flow in the other side while one side is shorted or faulted.

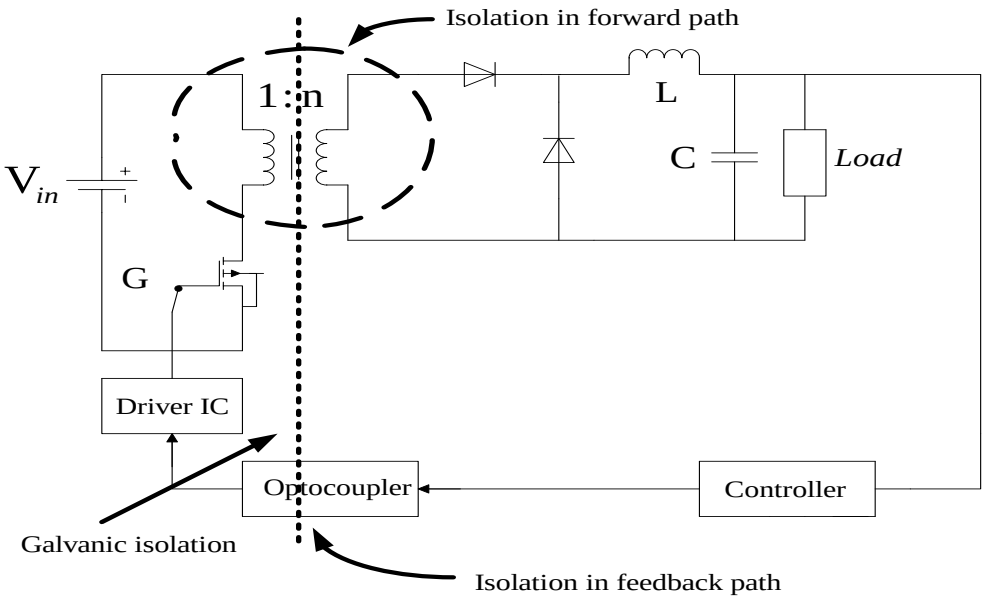



**Fig: Concept of Isolation in feedback path**

Now the isolation can be provided by various means. We can either use a transformer again to isolate the feedback or use an Optocoupler with a suitable current transfer ratio. The use of a transformer in the feedback will make the circuit bulkier as it is heavy and consumes a lot of space. On the other hand the Optocoupler, which now-a-days comes in a small IC package, is relatively small and light weight and very easy to use. We just have

to use a suitable Optocoupler package considering the current transfer ratio after designing the feedback path.

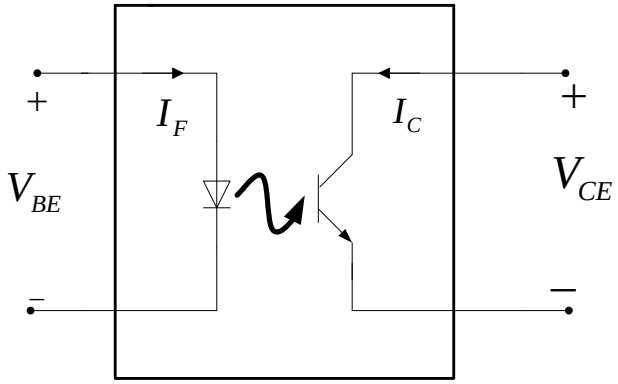



**Fig: A basic structure of an Optocoupler**

The Optocoupler is nothing but a combination of an LED and a transistor operating in the CE mode. When the diode is forward biased the LED glows and the light rays fall on the base of the transistor which gives rise to a base current and if the transistor is biased properly a collector current will flow out of the transistor.

The only problem with the CE configured transistor is the Miller's capacitance effect. The CB junction is the reverse biased junction which means that a capacitance is formed in that region which is basically the input-output port of the transistor. This capacitance between the base and the collector can be resolved according to Miller into two capacitances, one across the base (or the input) and the other across the collector i.e. the output. This capacitance across the input creates a pole in the transfer function of the converter which results in the degradation of the phase margin of the plant and also its stability. Thus effective counter measures should be taken so as to add a zero again in the transfer function of the plant. This can be done by adding a parallel combination of a resistor and a capacitor at the output of the Optocoupler and hence modifying the circuit.

## 4.2.1 PSPICE SIMULATION AND RESULTS

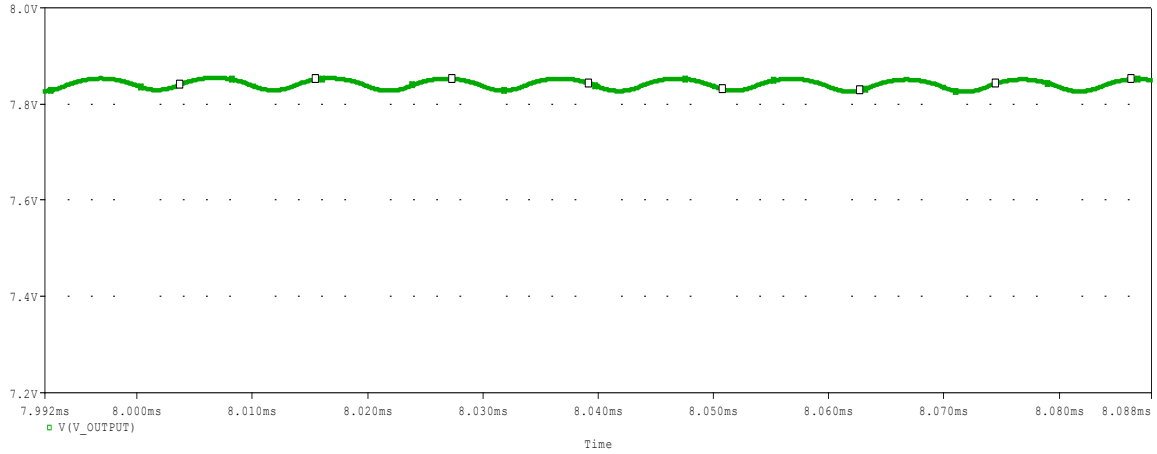



**Fig: Output Voltage Waveform**

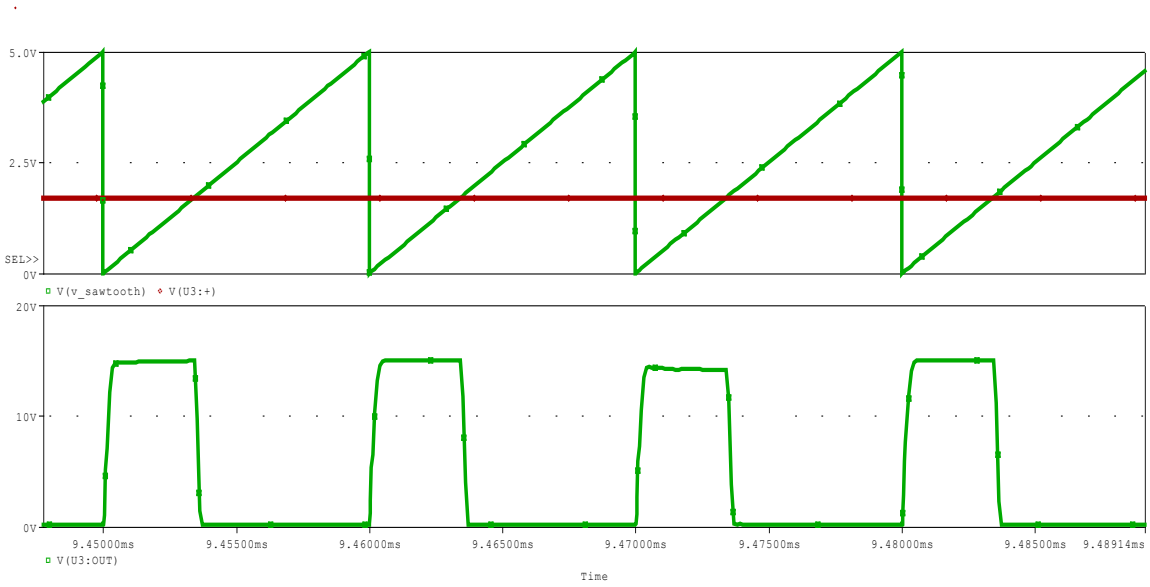



**Fig: Generation of Gate Pulse**

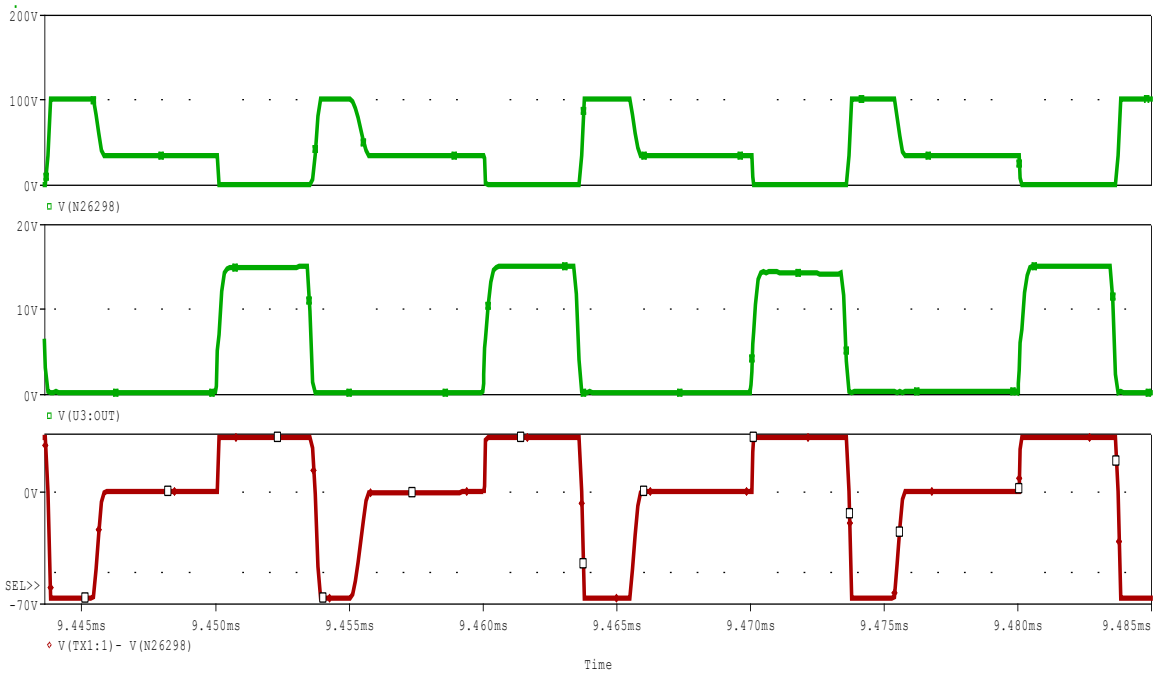



**Fig: a) Switch Voltage, b) Gate pulse, c) Transformer Primary Voltage**

# CHAPTER 5
# DESIGN OF COMPONENTS OF CONVERTER

## 5.1 DESIGN OF TRANSFORMER USING THE CORE GEOMETRY APROACH

### 5.1.1 SPECIFICATIONS

1. Input voltage, $V_{min}$ ..... 26 volts
   $V_{max}$ ..... 42 volts
   $V_{nominal}$ ..... 34 volts
2. Output voltage, $V_{out}$ ..... 8 volts
3. Output current, $I_0$ ..... 6 A
4. Switching frequency, f ..... 100kHZ
5. Efficiency, $\eta$ ..... 98%
6. Regulation, $\alpha$ ..... 0.5%
7. Diode voltage drop, $V_d$ ..... 1 volt
8. Operating flux density, $\Delta B$ ..... 0.1 T
9. Core material ..... Ferrite
10. Window utilisation, $k_u$ ..... 0.3
11. Temperature rise goal, $T_f$ ..... $30^0$C
12. Maximum duty ratio, $D_{max}$ ..... 0.5

## 5.1.2 DESIGN PROCEDURES

Skin Depth

$$\delta = \frac{6.62}{\sqrt{f}} = \frac{6.62}{\sqrt{100k}}$$

$$\therefore \delta = 0.0209 \text{ cms}$$

Wire diameter = $2(\delta) = 0.0418$ cms = D

Bare wire area = $A_w = \frac{\pi D^2}{4} = \frac{(3.14)(0.0418)^2}{4}$

$$A_w = 0.00137 \text{ cm}^2$$

From Standard available tables of AWG, Number 26 has bare wire area 0.00128 $cm^2$.

| WIRE AWG | BARE AREA($cm^2$) | AREA INSULATION | BARE/INSULATION | $\mu\ \Omega$/cm |
|---|---|---|---|---|
| # 26 | 0.00128 | 0.001603 | 0.798 | 1345 |

*Step 1: Transformer Output power*

$$P_o = I_o(V_o + V_d) = 6(8+1)$$

$$P_o = 54 \text{ Watts}$$

*Step 2: Input Power*

$$P_{in} = \frac{P_o}{\eta} = \frac{54}{0.98}$$

$$P_{in} = 55.102 \text{ Watts}$$

*Step 3: Electrical Co-efficient*

$$k_e = 0.145 * f^2 * (\Delta B)^2 * (10^{-4})$$

$$k_e = 0.145 * (100\,k)^2 * (0.1)^2 * (10^{-4})$$

$$k_e = 1450$$

*Step 4: Core Geometry, $k_g$*

$$k_g = \frac{P_{in} * D_{\max}}{\alpha * k_e}$$

$$k_g = \frac{55.102 * 0.5}{0.5 * 1450}$$

$$k_g = 0.0380 \ \ [\text{cm}]^5$$

Note: In this case transformer is being operated at 100 kHz with a wire #26. Now because of the skin effect at about 100 kHz the ratio of the bare wire area to the total area is about 0.78. Therefore the overall window utilisation $k_u$ is reduced. Thus to return back to the norm again $k_g$ is multiplied by 1.35 and the current density J is calculated using a window utilisation factor of 0.29.

$K_g$= (1.35)(0.0380)=0.0513 $cm^5$

*Step 5: Selection of ETD Core according to $k_g$*

| | |
|---|---|
| Core number | ETD-29 |
| Manufacturer | Ferroxcube |
| Magnetic material grade | 3C90 |
| Magnetic path length, MPL | 7.2 cm |
| Window height, G | 2.2 cm |
| Copper weight, $W_{tcu}$ | 32.1 gm |
| Core weight, $W_{tfe}$ | 28.0 gm |
| Mean Length Turn, MLT | 6.4 cm |
| Iron area, $A_c$ | 0.761 $cm^2$ |
| Window area, $W_a$ | 1.865 $cm^2$ |
| Area product, $A_p$ | 1.08 $cm^2$ |

| | |
|---|---|
| Core geometry, $k_g$ | 0.0517 |
| Surface area, $A_t$ | 42.5 $cm^2$ |
| Milihenrys per 1000 turns, AL (value approximated for a permeability of 1000) | 1000 |

| MATERIAL GRADE | AL | $\mu_e$ (PERMEABILITY) | AIR GAP ( $\mu m$ ) | TYPE NUMBER |
|---|---|---|---|---|
| 3C90 | 2350 ± 25% | 1770 | 0 | ETD 29/16/10 |

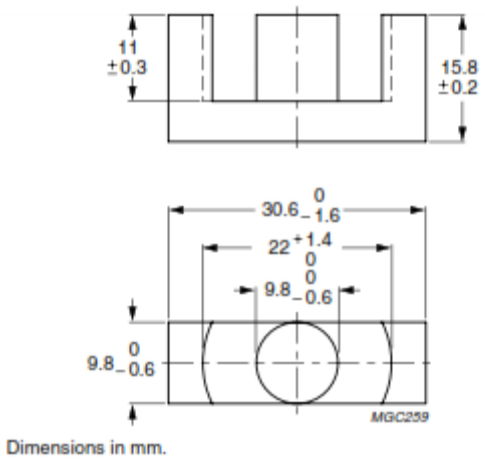



**Fig: Dimensions of ETD-29 core**

*Step 6: Number of Primary turns*

$$N_P = \frac{V_{in(\min)} * D_{\max} * 10^4}{f * A_c * (\Delta B)} = \frac{26 * 0.5 * 10^4}{100k * 0.761 * (0.1)}$$

$$N_P = 17.08 \approx 17$$

Step 7: Current density J, using window utilisation factor, $k_u$

$$J = \frac{2P_{in}\sqrt{D_{\max}} * 10^4}{f * A_c * (\Delta B) * W_a * k_u} = \frac{2(55.102)\sqrt{0.5} * 10^4}{(100\,\text{k}) * 0.761 * (0.1) * 1.865 * 0.29}$$

$$J = 189.33 \approx 190 \text{ A/cm}^2$$

*Step 8: Primary RMS current, $I_P$*

$$I_P = \frac{P_{in}}{V_{in(\min)}\sqrt{D_{\max}}} = \frac{55.102}{(26)(\sqrt{0.5})}$$

$$I_P = 2.997 \approx 3 \text{ Amps}$$

*Step 9: Primary bare wire area, $A_{wp\,(B)}$*

$$A_{wp(\text{B})} = \frac{I_P}{J} = \frac{3}{190}$$

$$A_{wp(\text{B})} = 0.01579 \text{ (cm)}^2$$

*Step 10: Number of primary strands, $NS_P$*

$$NS_P = \frac{A_{wp(\text{B})}}{\#26} = \frac{0.01579}{0.00128}$$

$$NS_P = 12.33 \approx 12$$

*Step 11: Calculation of new primary $\mu\Omega$/cm*

$$\text{new } \mu\Omega / cm = \frac{\mu\Omega / cm}{NS_P} = \frac{1345}{12}$$

$$\text{new } \mu\Omega / cm \approx 112$$

*Step 12: Calculation of Primary resistance, $R_P$*

$$R_P = (MLT)(N_P)(\mu\Omega / cm)_{new} * 10^{-6}$$

$$R_P = (6.4)(17)(112) * 10^{-6}$$

$$R_P = 0.0122\ \Omega$$

*Step 13: Calculation of Primary copper loss, $P_{cu}$*

$$P_P = I_P^2 R_P = (3)^2 (0.0122)$$
$$P_P = 0.1098 \text{ Watts}$$

*Step 14: Number of secondary turns, $N_s$*

$$N_s = \frac{N_P (V_o + V_d)}{(D_{\max})(V_{in(\min)})}[1 + \frac{\alpha}{100}] = \frac{17(8+1)}{(0.5)(26)}[1 + \frac{0.5}{100}]$$
$$N_s = 11.828 \approx 12 \text{ turns}$$

*Step 15: Secondary RMS current, $I_s$*

$$I_s = \frac{I_o}{\sqrt{2}} = \frac{6}{\sqrt{2}} = 4.2426$$
$$I_s = 4.24 \text{ Amps}$$

*Step 16: Secondary Bare Wire Area, $A_{wsB}$*

$$A_{wsB} = \frac{I_s}{J} = \frac{4.24}{190}$$
$$A_{wsB} = 0.0223 \text{ cm}^2$$

*Step 17: Calculation of number of secondary strands, $NS_s$*

$$NS_s = \frac{A_{wsB}}{\#26} = \frac{0.0223}{0.00128} = 17.43$$
$$NS_s \approx 17$$

*Step 18: New secondary $\mu\Omega/cm$*

$$\text{new } \mu\Omega/cm = \frac{\mu\Omega/cm}{NS_s} = \frac{1345}{17} = 79.11$$
$$\text{new } \mu\Omega/cm \approx 79$$

*Step 19: Calculation of secondary resistance, $R_s$*

$$R_s = (MLT)(N_s)(\mu\Omega/cm)_{new} * 10^{-6}$$
$$R_s = (6.4)(17)(79)(10^{-6}) = 0.0086 \text{ ohms}$$

*Step 20: Calculation of secondary copper loss, $P_s$*

$$P_s = I_s^2 R_s = (4.24)^2 (0.0086)$$
$$P_s = 0.1546 \text{ Watts}$$

*Step 21: Total Primary and Secondary copper loss, $P_{cu}$*

$$P_{cu} = P_P + P_S = (0.1098 + 0.1546)$$
$$P_{cu} = 0.2644 \text{ Watts}$$

*Step 22: Transformer Regulation, $\alpha$*

$$\alpha = \frac{P_{cu}}{P_o} = \frac{0.2644}{48} = 0.55\%$$

*Step 23: Calculation of Magnetizing inductance, $L_M$*

$$L_M = (L_{1000})(N_{mag})^2 (10^{-6}) \text{ [mH]}$$
$$L_M = (L_{1000})(N_P)^2 (10^{-6}) \text{ [mH]}$$
$$L_M = (2350)(12)^2 (10^{-6})$$
$$L_M = 338.4 \ \mu\text{H}$$

*Step 24: Calculation of OFF time, $T_{off}$*

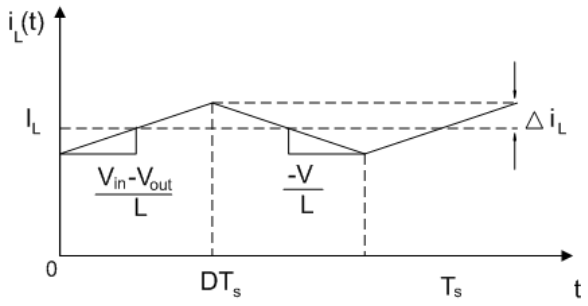



**Fig 2: Waveform of the inductor current**

$$T_{off} = T(1-D) = \frac{1-D}{f} = 5\mu \sec$$

*Step 25: Calculation of the ripple current,* $\Delta I$

$$\Delta I = \frac{V_{in}(T_{off})}{(L_M)} = \frac{26*5\mu}{338.4\mu} = 0.384 \text{ Amps}$$

*Step 26: Window utilisation factor,* $k_u$

$$k_u = \frac{N*(A_{wB}\#26)}{W_a}$$

Now, $N=(N_P NS_P) + (N_S NS_S)$

$$N = (17)(12) + (12)(17) = 408$$

$$k_u = \frac{408*0.00128}{1.865} = 0.28$$

*Step 27: Calculation of milliwatts per gram, mW/gm*

$$mW/gm = (0.000318)(f)^{1.51}(B_{ac})^{2.747}$$

$$mW/gm = 3.01$$

*Step 28: Calculation of core loss*

$$P_{fe} = (mW/gm)(W_{tfe})(10^{-3})$$

$$P_{fe} = (3.01)(28)(10^{-3}) = 0.084$$

*Step 29: Total Losses,* $P_\Sigma$

$$P_\Sigma = P_{cu} + P_{fe} = 0.2644 + 0.084$$

$$P_\Sigma = 0.3487 \text{ Watts}$$

*Step 30: Watts per unit area, Ψ*

$$\Psi = \frac{P_{\Sigma}}{A_t} = \frac{0.349}{42.5} = 8.21*10^{-3}$$

$$\Psi = 0.00821 \ [\text{watts/cm}^2]$$

*Step 31: Temperature rise, $T_f$*

$$T_f = 450*(\Psi)^{0.826}$$

$$T_f = 8.52^0 C$$

# 5.2 OUTPUT INDUCTOR DESIGN USING THE CORE GEOMETRY, kg APPROACH

## 5.2.1 SPECIFICATIONS

1. Input voltage, $V_{min}$ ..... 26 volts
   $V_{max}$ ..... 42 volts
   $V_{nominal}$ ..... 34 volts
2. Output voltage, $V_{out}$ ..... 8 volts
3. Output current, $I_{0max}$ ..... 6.6 A
4. Switching frequency, f ..... 100kHZ
5. Delta current, $\Delta I$ ..... 98%
6. Regulation, $\alpha$ ..... 1%
7. Output power, $(V_o+V_d)I_o$, $P_o$ ..... 54W
8. Operating flux density, $B_{pk}$ ..... 0.3 T
9. Core material ..... Ferrite
10. Window utilisation, $k_u$ ..... 0.4
11. Diode voltage drop ..... 1.0V

| WIRE AWG | BARE AREA | AREA INSULATION | BARE INSULATION | $\mu\Omega$/cm |
|---|---|---|---|---|
| #26 | 0.001280 | 0.001603 | 0.798 | 1345 |
| #27 | 0.001021 | 0.001313 | 0.778 | 1687 |
| #28 | 0.0008046 | 0.0010515 | 0.765 | 2142 |

**SELECTION OF CORE FROM $k_g$ (MPP TOROIDAL CORE)**

| | |
|---|---|
| Core Number | 55351 |
| Manufacturer | Magnetics |
| Magnetic path length, MPL | 5.88 cm |
| Core weight, $W_{tfe}$ | 18.706 gms |
| Copper weight, $W_{tcu}$ | 17.90 gms |
| Mean length turn, MLT | 3.5 cm |
| Iron area $A_c$ | 0.388 $cm^2$ |
| Window area, $W_a$ | 1.446 $cm^2$ |
| Area product, $A_p$ | 0.561153 |
| Core geometry, $k_g$ | 0.0249 |
| Surface area, $A_t$ | 31.40 $cm^2$ |
| Milihenrys per 1000 turns, AL | 51mH/1k |

| PART NO. | OD | ID | HT |
|---|---|---|---|
| 55351 | 2.430cm | 1.377 cm | 0.965 cm |

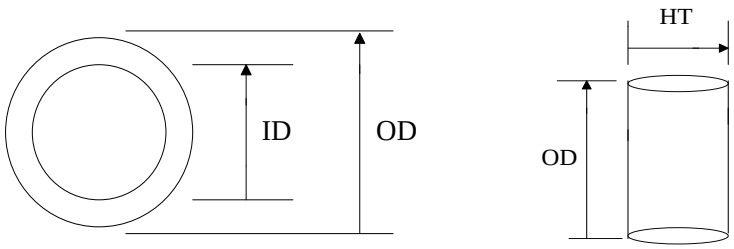



**Fig: Dimensions of Core 55351 (Top view and Front view)**

# CHAPTER 6

# HARDWARE DEVELOPMENTS AND RESULTS

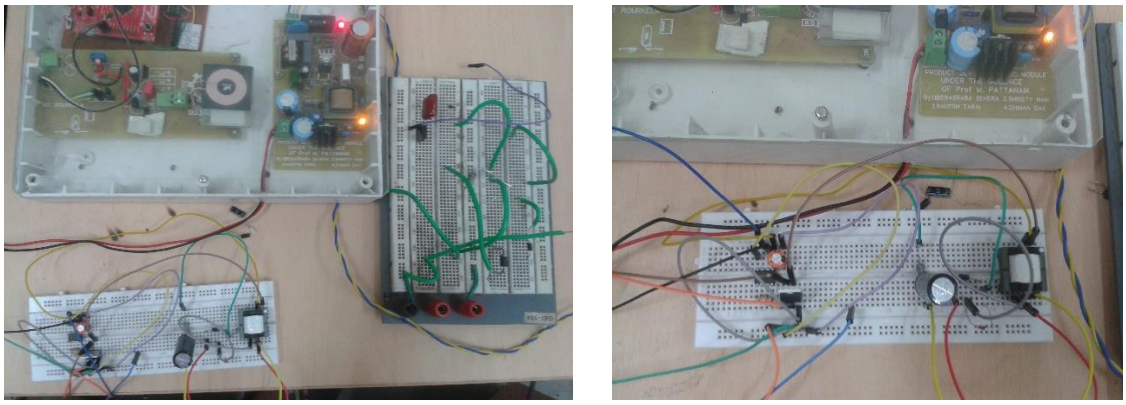


**Fig: Hardware Setup in Laboratory**

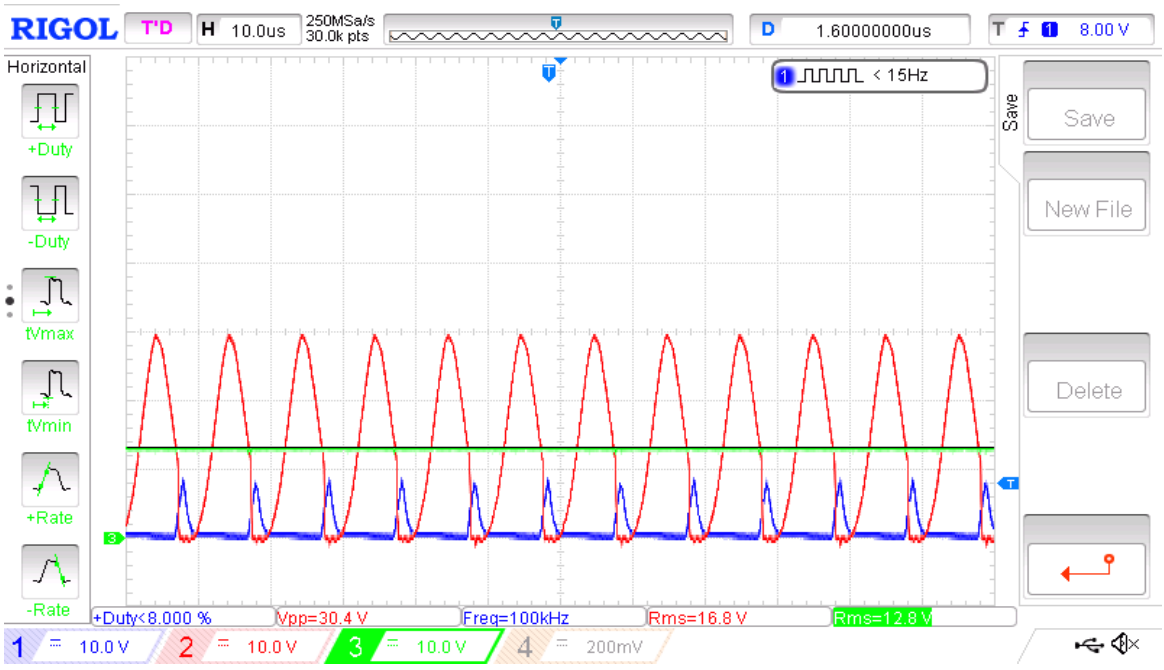


**Fig: Comparison of Switch voltage and input bus voltage at a switching frequency of 100 kHz and a duty cycle of 8%**

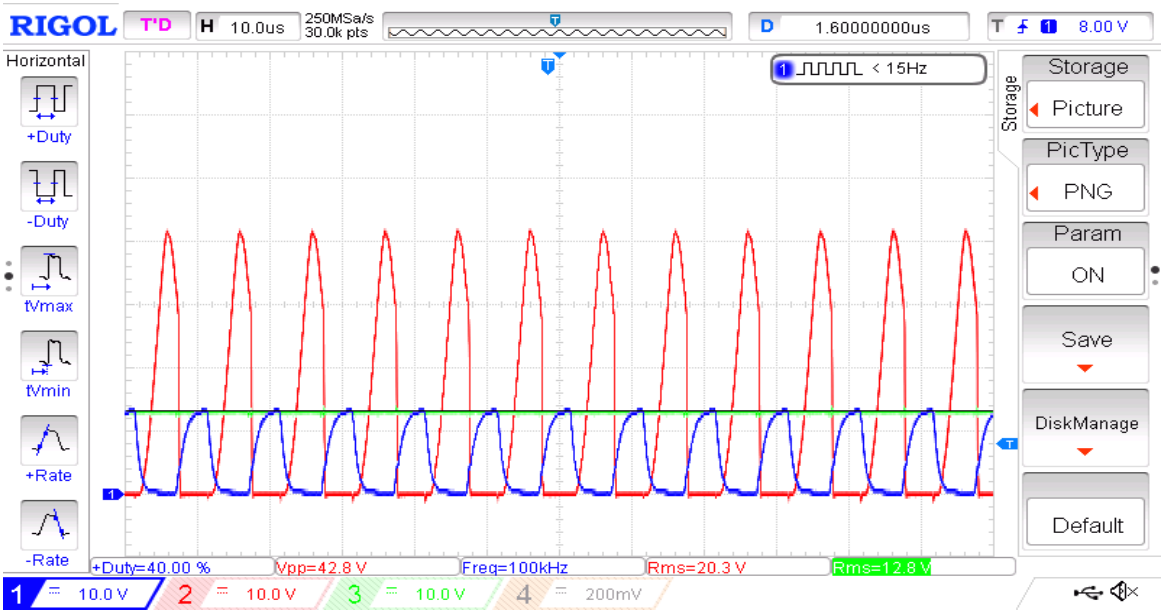



**Fig: Comparison of Switch voltage and input bus voltage at a switching frequency of 100 kHz and a duty cycle of 40%**

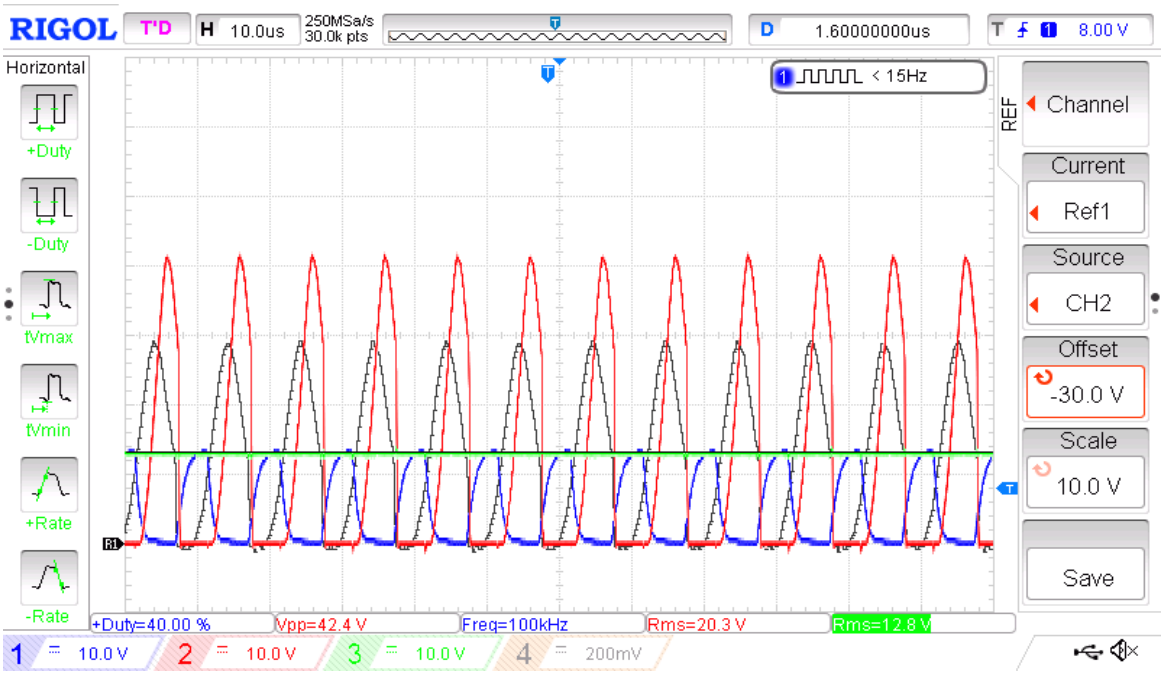



**Fig: Comparison of the switch voltages at an input bus voltage of 12V for two different duty cycle inputs of 8% and 40%**

# CHAPTER 7

# CONCLUSION

In this project we analysed in detail the working modes of a Resonant Reset Forward converter considering all the parasitic capacitances, both in distributed and lumped form. The lumped capacitance method gave somewhat better results as it resulted in the reduction in the number of modes and allowed us to formulate a reset criterion which was a function of the converter parameters. Next the small signal analysis was carried out by two approaches so as to develop a model which would eliminate all the higher order switching harmonics and give us high quality DC waveform at the output. In the feedback stage the addition of a type IIIB compensator generated the necessary phase margin and improved stability. But the incorporation of the Optocoupler to maintain the galvanic isolation led to the introduction of a pole in the transfer function which again degraded the system phase margin. This was manually compensated by using a parallel combination of a resistor and a capacitor at the terminals of the collector output of the transistor in the Optocoupler IC. Finally the simulations were carried out on various platforms as MATLAB and PSPICE to validate the theoretical models developed and hardware developments were done to establish the proposed model.

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