ATLAS BASED SIMULATION OF DOUBLE GATE TUNNEL FIELD EFFECT TRANSISTOR

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF
THE REQUIREMENTS FOR THE DEGREE OF
BACHELOR OF TECHNOLOGY

By
JYOTSNA KATIYAR
Roll no: - 112EI0276

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
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UNDER THE GUIDANCE OF
Prof. SANTANU SARKAR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
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CERTIFICATE

This is to certify that the thesis entitled, "Atlas based simulation of Double Gate Tunnel Field Effect Transistor" submitted by Jyotsna katiyar in partial fulfilment of the requirements for the award of Bachelor of Technology Degree in Electronics and Instrumentation Engineering at National Institute of Technology, Rourkela is an authentic work carried out by her under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university / institute for the award of any Degree or Diploma.

Date:

Prof. Santanu Sarkar
Dept. of Electronics and communication Engineering
National Institute of Technology
Rourkela-769008

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JYOTSNA KATIYAR

Date: Roll No: -112EI0276

B.Tech, Dept. of Electronics and Communication Engineering

NIT Rourkela

ABSTRACT

With the advancement in technology various devices are designed with the complex structure of processors. In this simulation through the study of Double Gate Tunnel FET, device parameters are studied to meet the requirements of the technological developments. The scaling of large devices is done to fabricate more no. of devices on a single structure. The integration of large devices into small chip provides efficient advantages with a smaller area. But as the number of devices increases the amount of supply voltage required is high as well as the decreases in the area increases the device OFF- state current.

To reduce all these problems TFET structure was designed to provide lower subthreshold swing. Several other structures like double gate tunnel FET is used to increase the ON-state current. The high- k and low-k dielectric were used with double gate. The high-k dielectric increases the channel capacitance and decreases the amount of subthreshold swing. Hence, the amount of supply voltage decreases and the power consumption is also reduced.

Dual material gate structure was designed over hetro dielectric to provide better current since the gate material like silicon and poly silicon is used. It has been observed that the amount of current increases in the presence of light because the flow of carriers increases so, the effect was applied on double gate structure to get the desirable amount of current.

Keywords : scaling, Double Gate Tunnel FET, TFET, channel capacitance

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CHAPTER 1

INTRODUCTION

With the advancement in technology several processors were designed with efficient usage. Since past few decades, the MOSFETs are scaled down to design a compact structure with the integration of more transistors on a single device as shown in Fig 1.1 Certain conditions were provided by ITRS, Firstly the advancement of scaling includes less power consumption with more no. of transistors on a single device and simulation of three-dimensional structure. The area of accomplishing the device should be decreased. The second one includes the integration of heterogeneous technology and designing the new devices with the efficient way.

With the introduction of new technology, the power consumption has increased. The device best suited for low power consumption are CMOS with a large amount of scaling in the device. But the amount of increase in transistor is greater than the increase in area due to scaling. As a result of which the temperature increases. This causes to increase in power dissipation of model.

The static power consumption is given by leakage OFF state current multiplied by supply voltage and dynamic power consumption is given by:

$$P_{dynamic} = f\, C_L (V_s)^2 \qquad \text{- - - (1.1)}$$

where f is the frequency, V_s is supply voltage and C_L is load capacitance.

So it is required to scale the value of supply voltage for proper functioning else the power consumption is high, which increases the heating effects in the device and causes the damage in the instrument.

So to solve these problems faced by the conventional MOSFET research has been done to find other devices with less power consumption and reduced subthreshold swing.

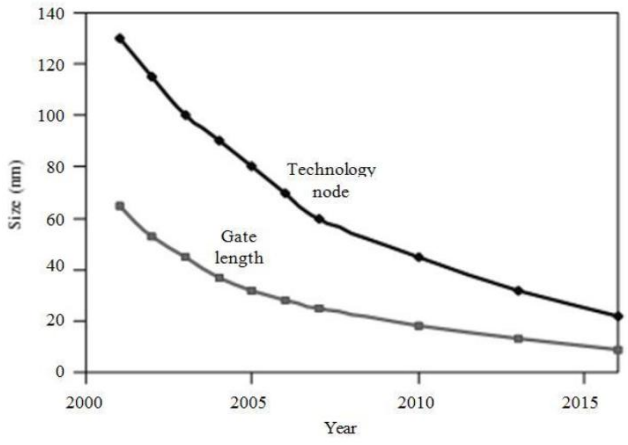

Figure 1.1 Size reduction over the decades

1.1 MOSFET

MOSFET is evolved from the MOS integrated circuit technology. MOSFET is a device which can be used in analog and digital circuits. It works on the basis of change in channel length. An Insulated layer of SiO_2 is deposited over silicon substrate its structure is same as planar capacitance. There are four terminals gate, source, drain, and body in which body is connected to source hence making it three terminal device.

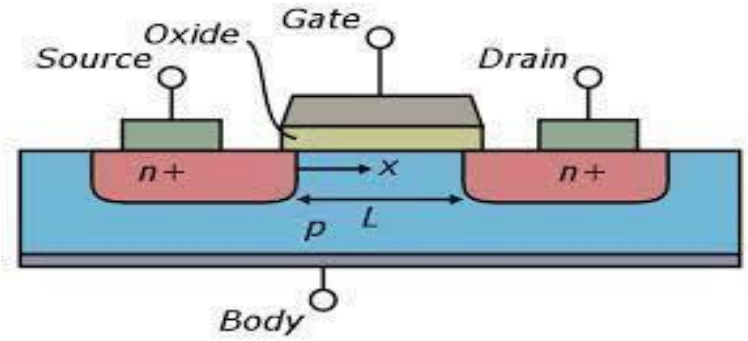

Figure 1.2 MOSFET structure

Mosfet structure: current flow is carried by the electrons. Source and Drain regions are formed by using n+ regions. In enhancement mode of MOSFET, channel starts forming between source and drain. When the positive voltage is applied between gate and source in this structure the holes are repelled at the channel forming a depletion layer with negative charges. As gate voltage is increased, electron density at the inversion layer increases and current flow from drain to source increases.

1.2 MODES OF OPERATION

There are three modes of operation of MOSFET:

1) cut off region:

The Transistor is considered to be in off state and Drain current is zero. Applied gate voltage is less than the threshold voltage, the gate to drain voltage(Vd) is less than the threshold voltage(Vt) and drain to source voltage (Vds) is greater than zero.

2) linear or triode region:

When the gate voltage is increased such that it is greater than the threshold voltage, the current starts flowing between source and drain and gate to drain voltage is greater than threshold voltage. Transistor is in ON state and works as a resistor.

3) Saturation region:

For saturation region gate to source voltage is greater than the threshold voltage, the gate to drain voltage is less than the threshold voltage and drain to source voltage is greater than zero. In the saturated region, the MOSFET behaves as an ideal current source.

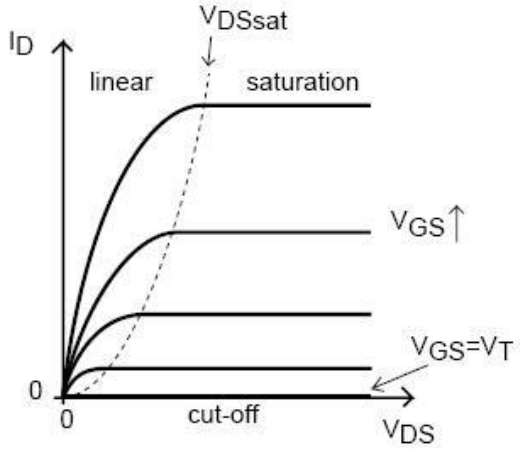

Figure 1.3 I_D vs V_{DS} characteristics of MOSFET

1.3 LIMITATIONS OF MOSFET

1) leakage current- when Vgs<Vt it is assumed that drain current is zero but the current decreases exponentially zero. The subthreshold swing is given by the amount of gate voltage applied to produce 10 times the change in current. Subthreshold swing is given by-

$$SS = \ln(10)\frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right) \quad \text{- - - (2)}$$

Its value is constant to 60 mv/dec for MOSFETs at room temperature. When scaling is done on the device to reduce power dissipation the subthreshold swing should be reduced.

2) Short channel effects-

a) Velocity saturation effect – Due to the scaling of MOSFETs to lower dimensions very high electric field is experienced by the charge carriers. In velocity saturation effect with the increase in electric field velocity increases but at very high electric field velocity saturates.

b) Drain Induced Barrier Lowering – In long channel devices, the threshold voltage is independent of drain voltage but due to short channel effects as the drain voltage is increased threshold voltage starts decreasing.

c) Impact Ionization- Due to high electric field the velocity of electrons is very high. They impact on silicon atoms and pair of electron and holes are created. This is called impact ionization.

d) hot carrier effect- Due to this, the electrons and holes enter into dielectric after gaining high kinetic energy. This changes the capacitance of the system and makes it less reliable.

1.4 SUBTHRESHOLD SWING

This is defined as the amount of gate voltage applied to provide a one decade change in current. Subthreshold swing for a Tunnel FETs changes with the change in gate voltage, it varies not constant. At low gate voltages, for Tunnel FETs, it is possible to have this value less than 60 mV/decade compared to MOSFET at room temperature. Tunneling current from a p-n Junction with reverse biased:

$I = aV_{eff} F \exp(-\frac{b}{F})$ - - - (3)

where

$a = Aq^3 \sqrt{2m^* E_g} / 4 \pi^2 \hbar^2$ and

$b = 4\sqrt{m^*} E_g^{3/2} / 3q \hbar$

V_{eff} is the bias voltage applied at tunnel junction. Subthreshold swing is given by :

$S = \ln 10 [\frac{1}{V_{eff}} \frac{dV_{eff}}{dV_{GS}} + \frac{F+b}{F} \frac{dF}{dV_{GS}}]$ - - - (4)

It is cleared from the above subthreshold swing value that it is dependent on V_{GS}. As gate voltage decreases the swing value decreases and it increases with the increase in gate voltage. Therefore, the value of subthreshold swing is not linear with the I_D and V_{GS} curve and may have different values. The swing can be defined as of two types on the basis of the I_D and V_{GS} curve –

1) Point Swing : This is the least value of swing on I_D and V_{GS} curve when the transistor is in OFF - state. This the starting value when tunneling current begins its flow.
2) Average Swing : When the device is in the on state ,the Average swing is calculated from the ON-state of the device.

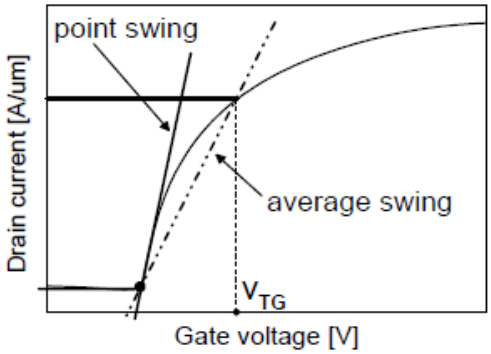

Figure 1.4

1.5 TUNNEL FIELD EFFECT TRANSISTOR

The Tunnel FET has the same structure as MOSFET but differs in the switching techniques and switching can be done at low voltage than MOSFETs. This device is more useful in low power electronics due to its low subthreshold swing and low OFF-state current. Unlike conventional MOSFETs the shorts channel effects are removed in Tunnel

FETs because the current is controlled by a tunneling phenomenon. It works on the principle of the band to band tunneling which makes it operate at the low subthreshold swing. Tunnel FET is a gated p-i-n diode which works on the basis of reverse bias. Source and drain region are heavily doped with p+ and n+ regions.

1.5.1 TFET STRUCTURE AND ITS OPERATION

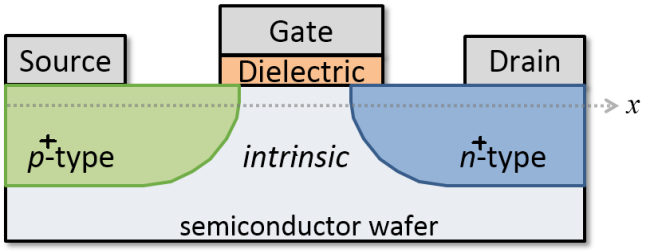

Figure 1.5 Tunnel FET structure

Tunnel FET is a gated p-i-n diode. Due to its heavily doped p+ and n+ region, depletion region forms at the junction of intrinsic region and the n+ doped drain region. When a reverse bias has applied the width of the depletion region increases producing the swept charge carriers. These charge carriers tunnel from intrinsic region to source valence band through the band to band tunneling phenomenon.

It is of two types n- type in which source is p+ doped and drain is n+ doped and a positive voltage is applied to the gate terminal. And other is p -type in which source n+ doped and drain is p+ doped.

1.5.2 BAND TO BAND TUNNELING

It is a phenomenon of conduction of current used in Tunnel Field Effect Transistor. The phenomenon of tunneling is same as a Tunnel diode. The Fermi level exists in the conduction band of n-type drain and valence band of the p-type source region. The electrons are present in n- type drain and holes are present in p- type source. At zero bias condition due to heavily doped p+ and n+ region, the conduction band of n side and the valence band of p side becomes align to each other as shown in figure 1.6.1. When reverse biased is applied the height of potential barrier decreases and electric field increases. This causes the electrons from the conduction band of n- type drain to transfer from the valence band of p- type source side, due to which the current increases and max current flows as shown in figure 1.6.2.

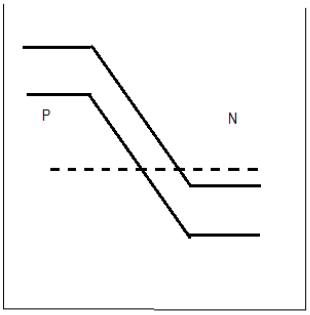

Figure.1.6.1 at zero biased condition

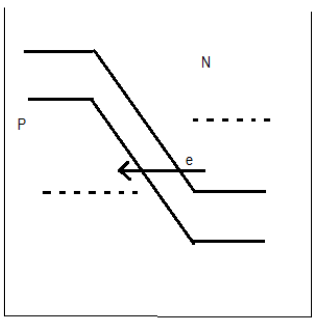

Figure.1.6.2. when a reverse bias is applied

Tunneling is of two types direct and indirect. In direct tunneling, the electrons pass from the valence band to conduction band without any absorption or emission of photons. The examples of this tunneling are GaAs etc. In indirect tunneling, there is a change of momentum due to absorption or emission phenomenon when the electrons are transferred from valence band to conduction band. The examples of the indirect band to band tunneling are germanium, silicon etc.

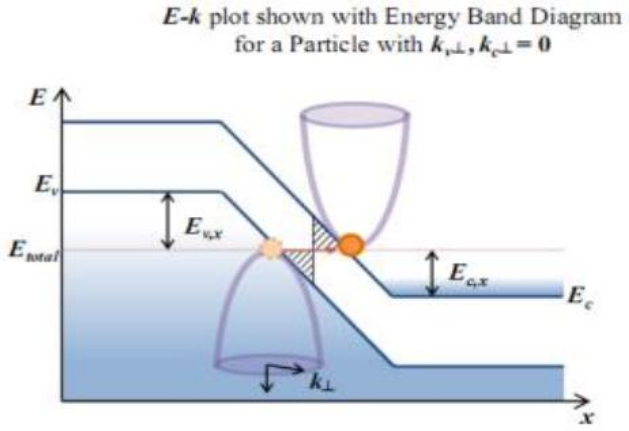

Figure 1.7.1 showing the direct tunneling process

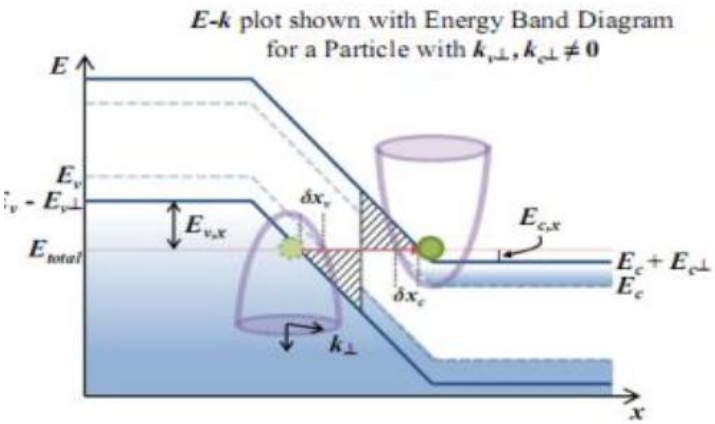

Figure 1.7.2 showing the Indirect tunneling process

The band to band tunneling expression for current can be described by WKB method of approximation. The potential barrier is taken as triangular. The value of transmission is

$T_t \approx \exp\left[-2 \int_{-x_1}^{x_2} |k(x)| dx \right]$ - - - (5)

Where k(x) is given by quantum wave vector and its value is given by

$K(x) = \sqrt{\frac{2m^*}{\hbar^2}} \sqrt{E_p - E}$ - - - (6)

Where E_p is given as potential energy and E is given by incoming electrons energy. The energy will be maximum when E=0 and potential energy can be replaced by :

Eg/2-qFx , Eg it is given by the energy band gap at the tunneling junction and F is given by the electric field.

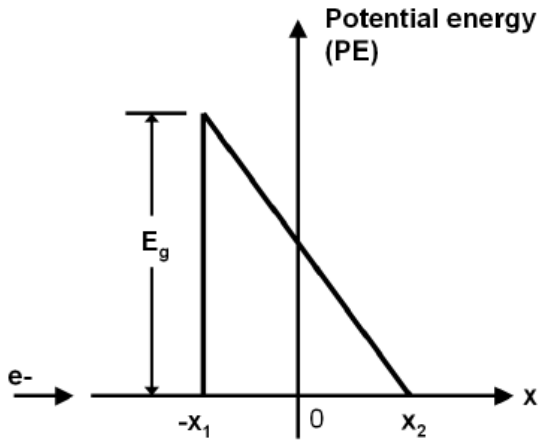

Figure 1.8 Potential barrier in triangular form in which the tunneling distance is large at the base portion of triangle

$K(x) = \sqrt{\frac{2m^*}{\hbar^2}} \sqrt{\frac{E_g - 2qFx}{2}}$ - - - (7)

Placing equation 7 in 5 :-

$T_t \approx \exp\left[-2 \int_{-x_1}^{x_2} \sqrt{\frac{2m^*}{\hbar^2}} \sqrt{\frac{E_g - 2qFx}{2}}\, dx \right.$ - - - (8)

$T_t \approx \exp[\frac{4}{3} \frac{\sqrt{2m^*}}{q\epsilon\hbar} (\frac{E_g}{2} - qFx)^{3/2}]$ - - - (9)

Integrated from x1 to x2 , we know that x = x2, (Eg/2 – qFx) = 0, and that at x = -x1,

(Eg/2 – qFx) = Eg, hence

$T_t \approx \exp[(\frac{-4\sqrt{2m^*}}{2} (E_g)^{3/2}) /3qF\hbar)$ - - - (10)

1.5.3 ADVANTAGES AND LIMITATIONS OF TUNNEL FET

ADVANTAGES :

There are many features in TFET that makes them efficient transistor in the upcoming future. The current carrying transport mechanism in both the devices is different as MOSFET uses drift and diffusion method for transport of carriers and TFET uses the band to band tunneling in the current flow process. So the dependency of MOSFET on temperature is high as compared to tunnel FETs which are less dependent on temperature. Therefore, in TFETs the subthreshold potential is less than 60 mv/decade.here in TFETs the tunneling width is controlled by the gate voltage and OFF state leakage current is less.

The value of subthreshold swing is reduced which reduces the amount of supply voltage required to operate and hence static and dynamic power dissipation is less. This decreased value of subthreshold swing helps them to behave as an ideal switch with the change in gate voltage in a small amount.

LIMITATIONS OF TFET:

1) In silicon Tunnel FET the ON current is less since band to band tunneling is not much effective which is needed to be overcome.
2) The excessive scaling of the device leads to very high OFF current and can vary the transistor performance.
3) The current flows in both directions due to ambipolar nature of TFET. It shows p -type behavior with excess holes and n -type with excess electrons. TFETs show the dominant phenomenon of ambipolar nature, in which symmetric structures are maintained and the level of doping of drain and source is done same with single material of gate dielectric.

CHAPTER 2

DOUBLE GATE TUNNEL FET

2.1 DOUBLE GATE TUNNEL FET

Double gate Tunnel FET consist of conducting channel surrounded by the gate electrodes on both sides and the channel is formed in between. Double gate tunnel FET plays a very important role in increasing the current by providing better control over the channel. In this work, the study of TFET with single and double gate, using different gate dielectrics and using dual material gate is done to improve the current and to achieve efficient characteristics. The simple model of the double gate is studied to get the desired amount of current with suitable subthreshold voltage. There is always the benefit of the extra gate like extra current can add to the original one. Hence, ON current is increased. The presence of two gate forms two tunneling junctions hence there is an increase in current and the OFF current is same in the range of pA. Subthreshold swing is decreased and Ion/Ioff ratio is increased making it the suitable device for operation.

2.1.1 STRUCTURE AND OPERATION

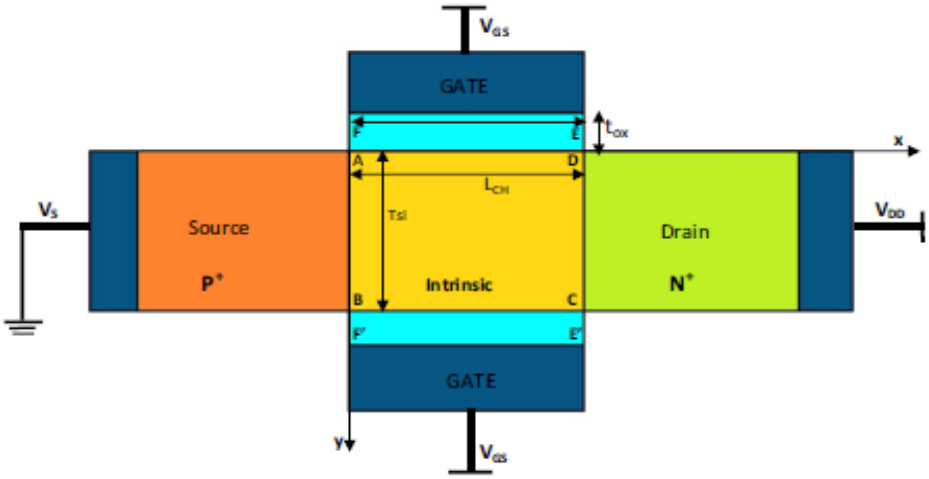

Figure 2.1 structure of double gate tunnel FET

The working principle is same as tunnel FET and follows the band to band tunneling for the conduction of current. Voltage is applied to the gate terminal which controls the electric field and it provides the better control over channel current. The presence of double gate improves the control over tunnel junction with the gate voltage and this causes the current to double the previous amount coming from the thin device body. The current is increased by two decades and hence, the subthreshold swing is decreased.

The doping level plays an important role in the optimization of the device characteristics like an increase in ON current and decrease in OFF current. The doping in source region should be high for the optimized on current and desirable characteristics because of the tunneling between the source and intrinsic region. The OFF state current depends on the doping level in the drain region. The ambipolar behavior of the transistor is shown when the doping levels are equal in both source and drain region. The undesirable characteristics can be reduced by decreasing the doping level in drain side. This also decreases the OFF current level. The gate threshold voltage differentiates or checks the changes in the tunnel

junction width through the energy barrier. The change from single to the double gate has highly increased the current.

2.1.2. OBJECTIVES OF DOUBLE GATE TUNNEL FET

1) Reduced short channel effects- The dependency of the threshold voltage on drain voltage decreases. its value remains constant and makes the device more reliable. the value of OFF state leakage current decreases.

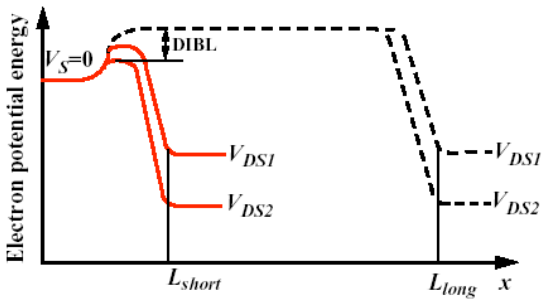

Figure 2.2.1 For short channels as drain voltage is increased potential barrier decreases, due to which large no of electrons flow to the drain.

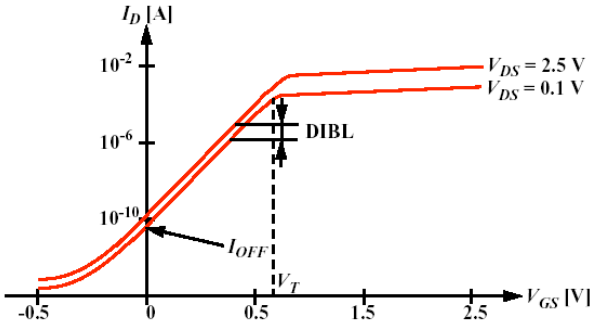

Figure 2.2.2 Due to this with the increase in drain voltage the threshold voltage decreases , hence these effects can be reduced using the double gate.

2) The ration of I_{ON}/I_{OFF} has increased making it suitable for lower power electronics applications. The I –V curve values are accurate and sharp.
3) It is easily fabricated through simple processes.

2.1.3 ADVANTAGES AND PROBLEMS

ADVANTAGES

1) decreasing the OFF state leakage current. I_{off} , it is the current flowing when V_{GS}=0 and device is considered to be in off state. this arises due to mainly due to Thermionic emission phenomenon, Quantum Mechanical Tunneling, and Band-to-Band Tunneling.

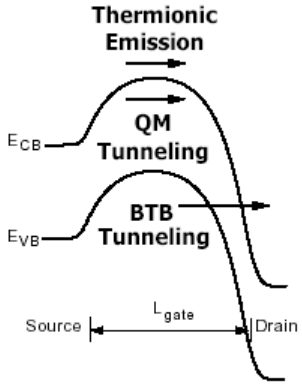

Figure 2.3

With the help of double gate, the potential of the channel is efficiently controlled by gate and channel capacitance increases.

2) it decreases the variation of internal parameters since threshold voltage fluctuations are decreased and minimizes the scattering of impurity.

3) double gate adds up to the double value of current.

4) It provides better electrostatic control over the channel.

PROBLEMS IN FABRICATION:

1) there are several problems in the fabrication process.

2) for efficient device alignment of both the gates is necessary which is difficult to achieve. the misalignment in the gates can cause extra capacitance to arise which may cause the leakage current to increase.

2.2 HETRO DIELECTRIC DOUBLE GATE TUNNEL FET

TFETs can be used as alternatives for MOSFETs since it is not affected by the degradation of subthreshold swing due to short channel effects. It has been seen that TFET does not provide the desirable amount of ON- state current and shows the ambipolar behavior.

It provides the better performance over using a single layer of silicon dioxide only. The value of subthreshold swing provided by the TFET is also not desirable. Therefore, a high-k dielectric and a low- k dielectric materials are used at the gate. The hetro dielectric double gate TFET is featured with high-k and low-k dielectric values at the gate in drain and source side.

In double gate TFET only silicon dioxide is used as gate dielectric material. The length of the low-k silicon dioxide is equal to the length of high-k dielectric values below the gate. The value of subthreshold swing is decreased and the amount of ON -state current is expected to be of higher value after using the dielectrics.

The hetero gate dielectric is a lower band gap material which is used in the Double Gate Tunnel FET and simulated over here. The device simulated has reduced value of short channel effects and channel length modulation. There are three capacitances in tunnel FET, the capacitance between gate and source(Cgs), between gate and drain (Cgd) and channel

capacitance. In ON state, the value of gate to source capacitance is less for double gate TFET and due less potential between drain and channel Cgd is having high value. Hetro gate oxides are used to fulfill ITRS requirements.

2.2.1 CASE: I STRUCTURE AND OPERATION

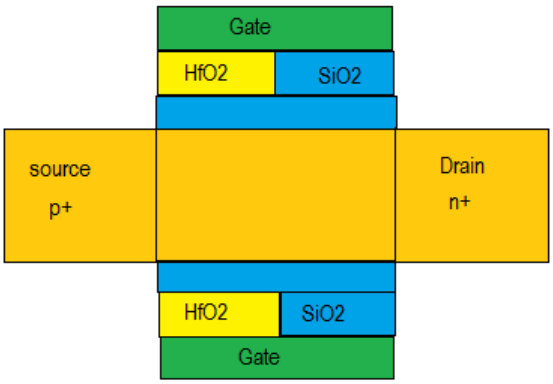

Figure 2.4. Hetro Dielectric Double Gate Tunnel FET with HfO_2 at the source side and SiO_2 at the drain side.

In the first case, the HfO_2 (high –k material) is placed at the source side and SiO_2 (low-k material) is placed at the drain side. The current flowing in ON-state is called as drain current which flows when the amount of gate voltage and the drain voltage supplied is 1 V and it can be expressed by the overlapping of the source to channel dopped region. The current flowing in the OFF state due to ambipolar effects is called as the ambipolar current which flows when the amount of gate voltage supplied is -0.2 V and drain voltage is 1 V and it can be expressed by the drain to channel doping by a low-k dielectric.

The width of the tunnel junction becomes less and the conduction band level in the drain gets aligned with the valence band level in source side by using these two types of dielectrics in the same structure. The structure with high -k dielectric is independent of temperature. The use of insulators reduces the band-to-band tunneling (BTBT) effects due to which OFF state current increases. The current obtained in this structure can be further improved so, another structure of double gate was simulated. In ON state of the device, the tunnel width decreases with the increase in gate voltage due to which tunneling occurs and in the OFF state of the device the tunnel width decreases, even though a small amount of leakage current flows through the device.

2.2.1.1 HETRO DILELCTRIC DUAL MATERIAL DOUBLE GATE TUNNEL FET:

In this study, the structure of hetro dielectric with the dual material gate is studied. The two types of the gate are defined, the gate length covering the high-k dielectric HfO_2 at source side is called as tunneling gate and gate length over low –k dielectric SiO_2 at the drain side is called as auxiliary gate. The source region is heavily doped with the p+ region, the drain is heavily doped with the n+ region and the intrinsic region is p-type doped region. There exist two different values of work function for different gates φ_{tunn} and φ_{aux} . the tunnel gate

over HfO2 has work function φ_{tunn} and the auxiliary gate over SiO2 has the work function $\varphi_{aux.}$

STRUCTURE AND OPERATION

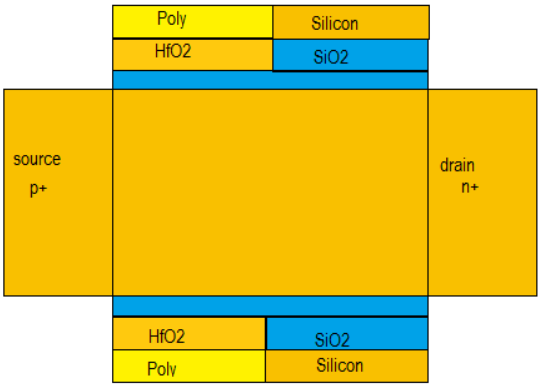

Figure 2.5 Hetro Dielectric Dual Material Double Gate Tunnel FET structure

HD-DMG DGTFET has a p-i-n structure which works on the basis of the reverse biased voltage applied. When the gate voltage is increased the tunnel width decreases and energy barrier. This phenomenon causes the transfer of electrons from the conduction band of drain side to the valence band of the source side and hence tunneling occurs. The insulator with high-k dielectric is used to increase the ON - state current because due to this the coupling of bands increases at the junction.

The electrical characteristics can further optimize with the variation in the work function of the device. Initially, when tunnel gate work function is fixed to 4 eV and auxiliary gate work function is increased from 4 eV to 4.8 eV , the leakage OFF state current increases because the tunneling at the drain and intrinsic region increases due to less tunnel width and potential barrier. This change in auxiliary work function does have much effect on ON-state current of the device because the tunnel width increases and overlapping of band decreases at the source and channel junction. When φ_{aux} is very high greater than 4.4 eV the value of OFF state current increases.

Now tunnel gate work function is increased by keeping auxiliary gate work function constant. This increases the tunnel width and very less amount of current flows. Hence, for less value of tunnel gate work function, the current is high because the amount of threshold voltage and tunnel width is less. The amount of current is not up to the desirable amount so another structure is simulated with the single material gate but Hetro dielectric.

2.2.2 CASE: II STRUCTURE AND OPERATION

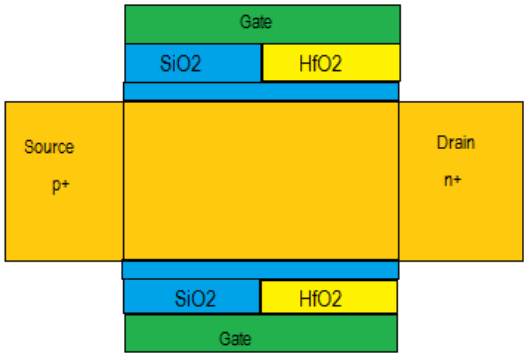

Figure 2.6 Structure of Hetro dielectric double gate with HfO_2 at drain side and SiO_2 at source side

To get the desirable amount of current another structure was simulated with reversing the insulators. In this structure, the high-k dielectric is placed at the drain side and low-k dielectric is placed at the source side with germanium gate. The germanium gate has several advantages over silicon gate as the band gap of germanium is less so the tunneling process becomes fast and the transfer of electrons from the drain to source region increases.

Double gate – In double TFET there is added the advantage of the presence of extra gate and two tunnel junctions are created.the value of subthreshold swing is deceased and the current ratio of ON -state current and OFF state current increases. It provides immunity to short channel effects, by reducing the dependency of the threshold voltage on drain voltage. It provides better electrostatic control over the channel.

High –k dielectric :– there are several high –k dielectric insulators like SiO2 and Si3N4 which can be used as high- k dielectric for the decreased value of subthreshold swing and increased drain current.

The oxide capacitance is given by

$C_{ox} = kA\varepsilon / t$ - - - (11)

So if high-k dielectric is used the value of oxide capacitance is increased. The sub threshold swing is given by-

$SS = \ln(10) \frac{kT}{q}(1 + \frac{C_d}{C_{ox}})$ - - - (12)

So as the capacitance increases the value of subthreshold swing decreases. The current for the system is given by –

$I_D = \frac{W}{L}\mu C_{ox}(V_G - V_{th})^2 / 2$ - - -(13)

Low –k dielectric :– SiO2 as low dielectric value is used in the device. It helps in suppressing the ambipolar effects produced in TFET.

Ambipolar effects – These effects arises when the level of doping is same in both the drain and source region. Therefore, it can be reduced or removed using asymmetric structures with different doping in source and drain region or by introducing different dielectrics. The low –k type dielectric helps in reducing the effect of ambipolar behavior.

2.3 HETRO DIELECTRIC DOUBLE GATE TUNNEL FET WITH INFRARED RAYS

To find the level at which the energy bands align each other in source and drain side was difficult earlier. Different methods and experiments were done finally. The infrared radiations are falling on the device. With the help of optical photoemission of particles the potential barrier in source and drain side can be reduced. Several device models like impact ionization were introduced to decrease the less subthreshold swing value. The flow of ON current takes place with the help of band to band tunneling. The gate material used over here is germanium which consists of maximum no of mobile electrons and holes. When the light rays fall on the device these mobile charges start flowing and participate in the flow of current. This current is added to the band to band tunneling current value and helps in increasing the current of the device to the desirable amount.

CHAPTER 3

SIMULATION PROCEDURE

3.1 SIMULATION USING ATLAS

Atlas is a software which provides with the capability to perform the simulation of semiconductor devices in two dimensions and in three dimensional. It helps in performing different analysis and gives us the idea of the device parameters which helps in designing of devices for future generation. It helps in optimizing the characteristics of semiconductor devices for the wider application. The different selected models simulation results and meshing structure helps in getting the idea of device parameters and its behavior.

Atlas consist of several VWF tools(Virtual WaferFabrication). These tools include

1) DeckBuild - The command language of Atlas run in a particular environment which is provided by DeckBuild.
2) TonyPlot - The output characteristics such as log files and structure files with device parameters are referred using TonyPlot.
3) DevEdit - The meshing specification and device structure is created in an environment given by DevEdit.
4) MaskViews- they are used for editing the IC layout .
5) Optimizer – it is used for providing Optimization in different simulators.

Athena is used as a simulator for the process, after different steps of processing are completed the structures are produced by it. The VWF tools help in analyzing the characteristics of the devices and suitable for the development of semiconductor devices. The meshing is done in designing of the structure which includes dividing the space into small portions and defining the value of electrodes at that point.

There are two input files in Atlas which contains the structure which we need to simulate, they are structure file and command file (includes the necessary command for the simulation process). They combine together to form text file.

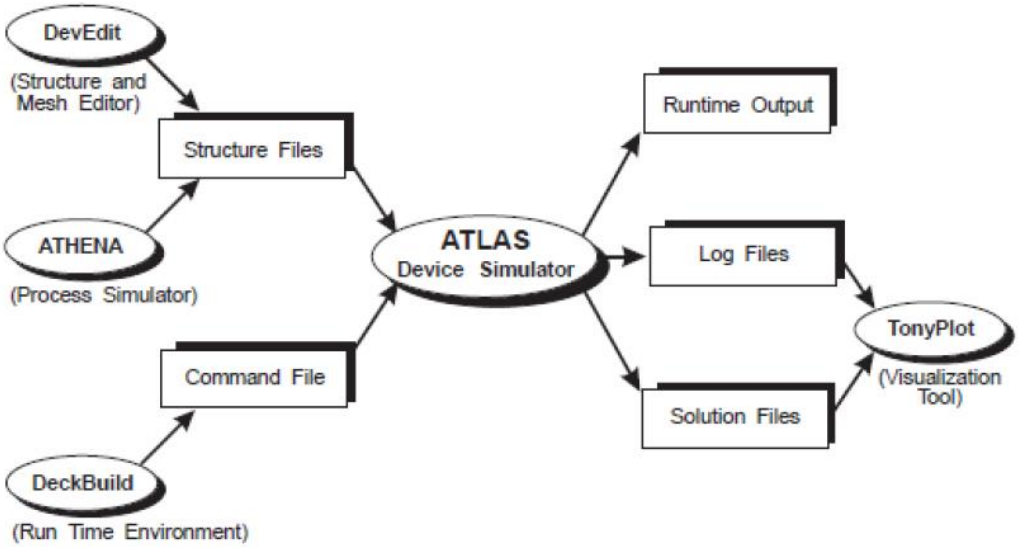

Figure 3.1 Flow of the simulation process in Atlas .

There are three output files :

1) Runtime output - This is the output obtained at every instant of execution of the program when the processing starts and shows errors in the device.

2) log files - These give the information about different electrical parameters. These involve the basic simulation results with the help of which different characteristics can be the plot for different electrical parameters.

3) Solution files - This includes the information about data for electrical parameters of the device by the simulation results.

3.2 MODELS IN SIMULATION:

There are several models defined in the Atlas, according to the structure to be simulated they are chosen. The commonly used models are:

1) Concentration dependent and low field model :- This is activated using CONMOB command and the information for mobility of electron and holes is provided.

2) Fermi- Dirac model :- FERMI is used to represent this model. This model is used in the situations when the doping is high and concentration of carriers is low.

3) Tunneling Models - There are different tunneling models-

a) Normal Band to Band Tunneling -

When the electric field present is very high and the width of tunnel junction decreases and the electrons tunnel due to overlapping of bands. This phenomenon includes standard tunneling process. The rate of tunneling can be expressed by the given equation:

$$G_{BBT} = \text{D BB.A } E^{BB.GAMMA} \exp\left(\frac{-BB.B}{E}\right)$$

Where , E is the Electric field, other are parameters defined by the user.

BB.A = $9.6615e^{18} cm^{-1}V^{-2}s^{-1}$

BB.GAMMA =2.0

BB.B = $3.0e^{7}$V/cm

b) Kane model of band to band tunneling-

It is same as the standard method of the band to band tunneling and proposed by kane. The rate of tunneling is given by

$$G_{BBT} = \frac{D\ BBT.A_{KANE}}{\sqrt{E_g}} F^{BBT.GAMMA} \exp\left(-BBT.B\_KANE\ \frac{{E_g}^{3/2}}{F}\right)$$

E is an electric field and F is bandgap.

c) Non- Local Band to band tunneling –

when band to band tunneling is non- local. This type of band to band tunneling is used for tunnel FETs. According to this, the tunneling depends on each local point not just on the electric field and it happens at every one -dimensional part. Their parts divided in one dimension slices are parallel with each other. It can be defined by BBT.NONLOCAL. They can be specified as

- QTX.MESH and QTY.MESH, these are used for specifying the region in a rectangular shape around the device.
- QTREGION, this specifies the area near Tunnel junction.

The tunneling can be given by the equation:

$$T(E) = \exp(-2\int_{x_{start}}^{x_{end}} k(x)dx)$$

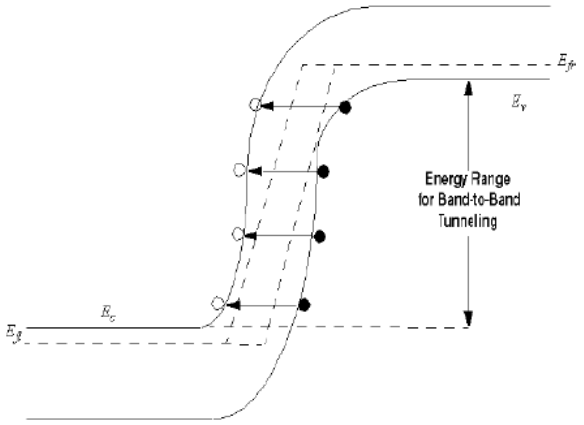

Figure 3.2 Diagram of non -local band to band tunneling

3.3 METHODS OF SOLUTION

NUMERICAL METHOD

There are three different methods :

1) Gummel- By keeping the value of all the variables constant, only the value of one variable is calculated and simulated.
2) Newton- This involves repetition of the same process again and again to find the value of unknown parameters. All the variables are simulated simultaneously.
3) Block- It is having the properties of both the variables , as it finds the solution to some of the variables and keeps some of the variables as constant.

OTHER METHODS:

There are many other methods in Atlas to find the solution of the device parameters : DC method is used for finding the DC solution of the device and AC method is used for finding the AC solution. AC method is the extension of DC solution .

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 TUNNEL FET STRUCTURE AND ITS CHARACTERISTICS

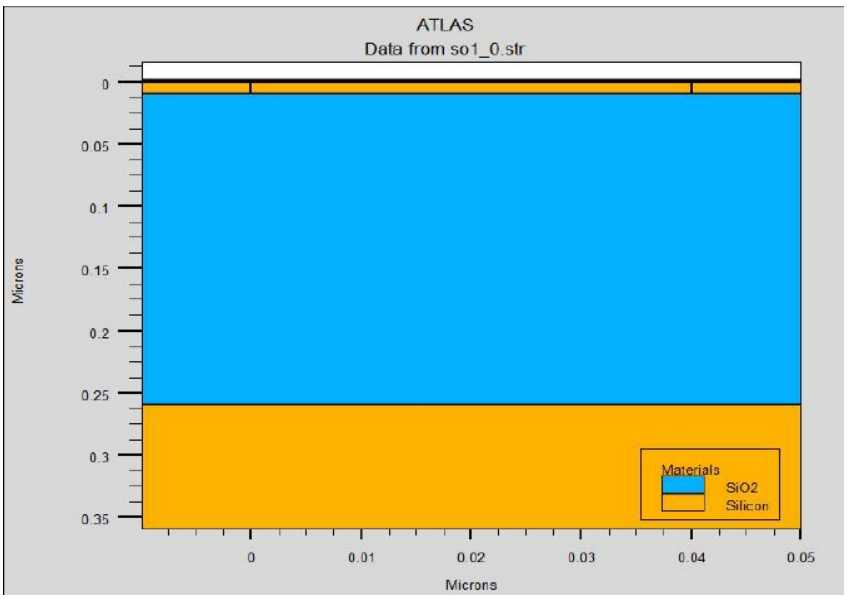

Figure 4.1.1 Tonyplot simulated result of Tunnel FET

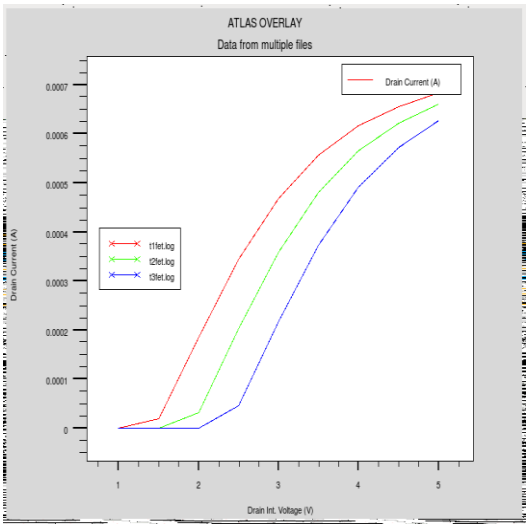

Figure 4.1.2 I_D vs V_D characteristics at Different V_G

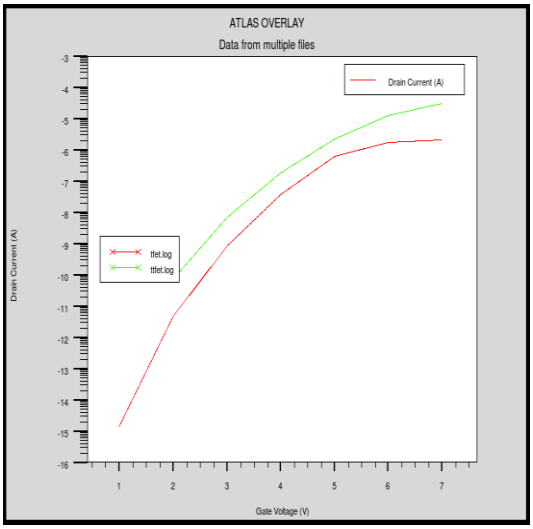

Figure 4.1.3 I_D vs V_G characteristics for different V_D

The Tunnel FET simulation was performed using Atlas software which is shown in Fig 4.1.1. It is clear from the Fig. 4.1.2 as the gate voltage increase the value of drain current increases and drain current vs gate voltage characteristics were simulated at different values of drain voltage.

4.2 DOUBLE GATE TUNNEL FET CHARECTARISTICS

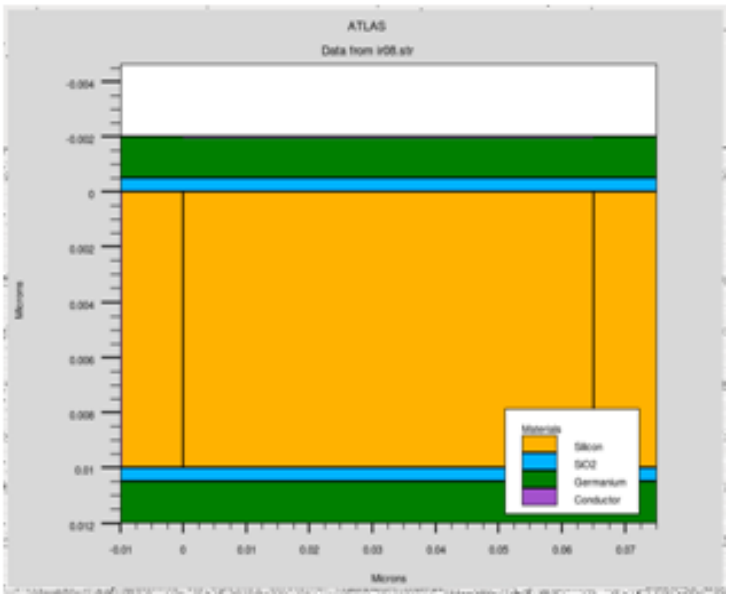

Figure 4.2.1 Tonyplot structure of Double Gate Tunnel FET

The double gate structure is simulated in Atlas to get the efficient characteristics and decreased the value of subthreshold swing.

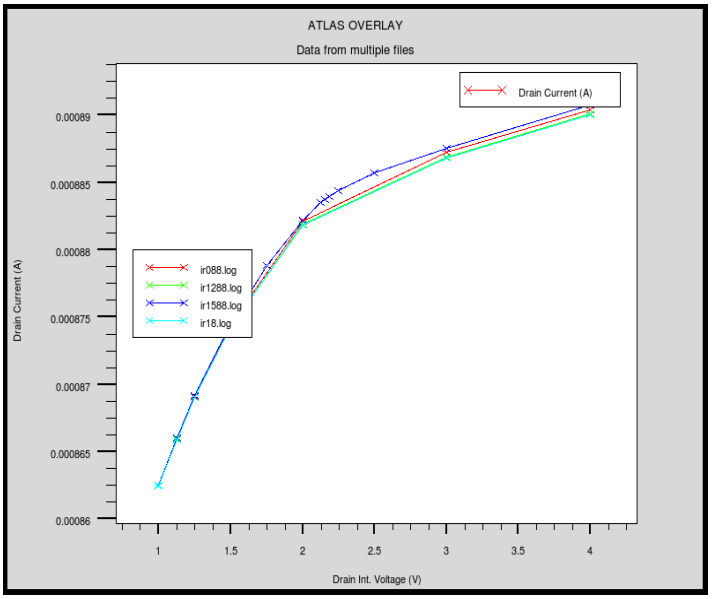

Figure 4.2.2 I_D vs V_D characteristics at different V_G

The simulated structure of Double Gate Tunnel FET gives the better performance of the device. The drain current vs drain voltage characteristics is obtained with the efficient advantage of decreased value of subthreshold swing.

4.3 HETRO DIELECTRIC DOUBLE GATE TUNNEL FET

Case : I HfO_2 at source side and SiO_2 at drain side

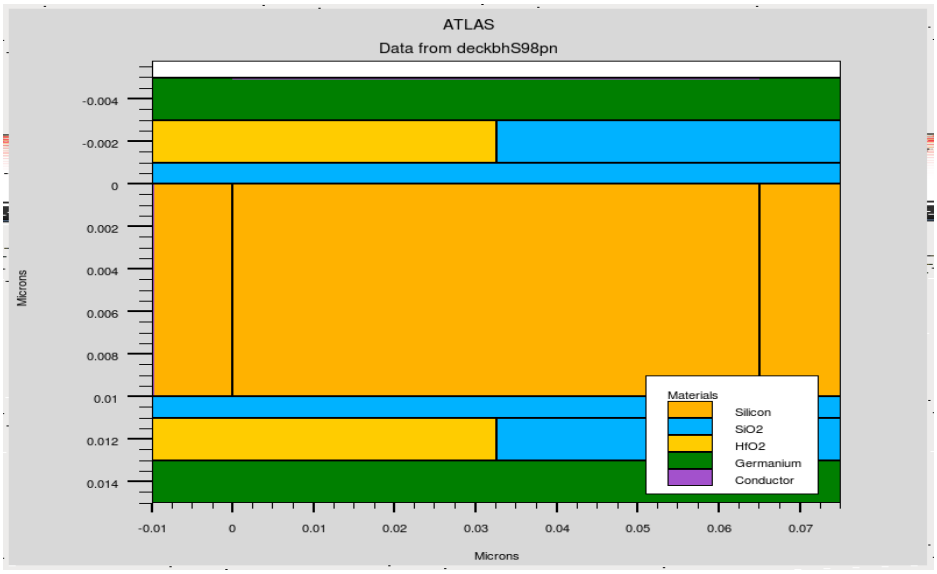

Figure 4.3.1 TonyPlot structure of Hetro Dielectric Double Gate Tunnel FET

The structure of hetro dielectric with HfO_2 at the source side and SiO_2 at the drain side are simulated using Atlas.

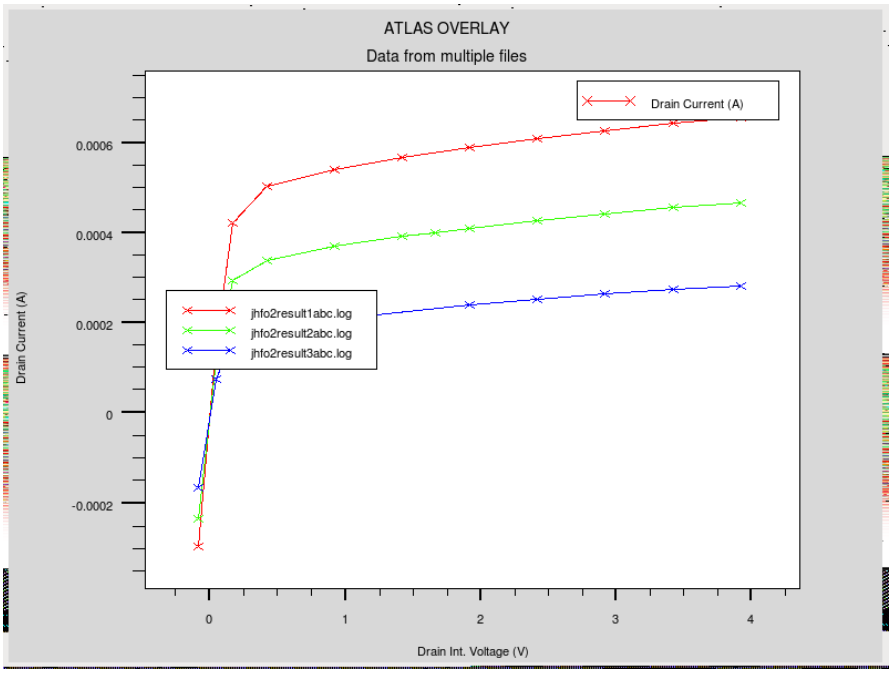

Figure 4.3.2 I_D vs V_D characteristics for different value of V_G

The drain current vs drain voltage characteristics for different values of gate voltage was simulated and the amount ON -state is improved.

4.3.1. HETRO DILELCTRIC DUAL MATERIAL DOUBLE GATE TUNNEL FET

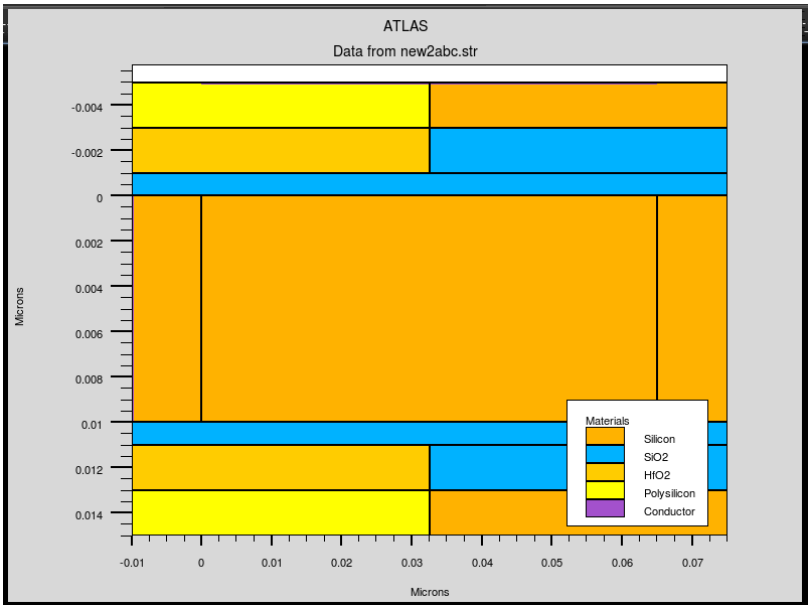

Figure 4.3.3 TonyPlot structure of Hetro Dieleclctric dual material double gate tunnel fet

The structure of hetro dielectric was simulated using different material at the gate using TonyPlot.

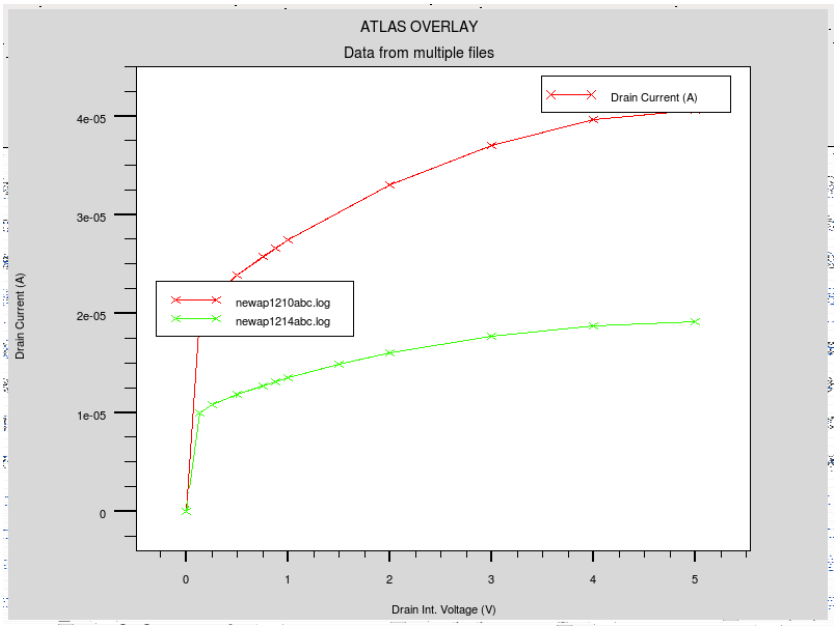

Figure 4.3.4 Id vs Vd for different values of Work function 4 and 4.4

The value of current decreases in ON state when work function of tunnel gate is increased and its is shown from the Figure .4.3.4

Case :II HfO_2 at drain side and SiO_2 at source side

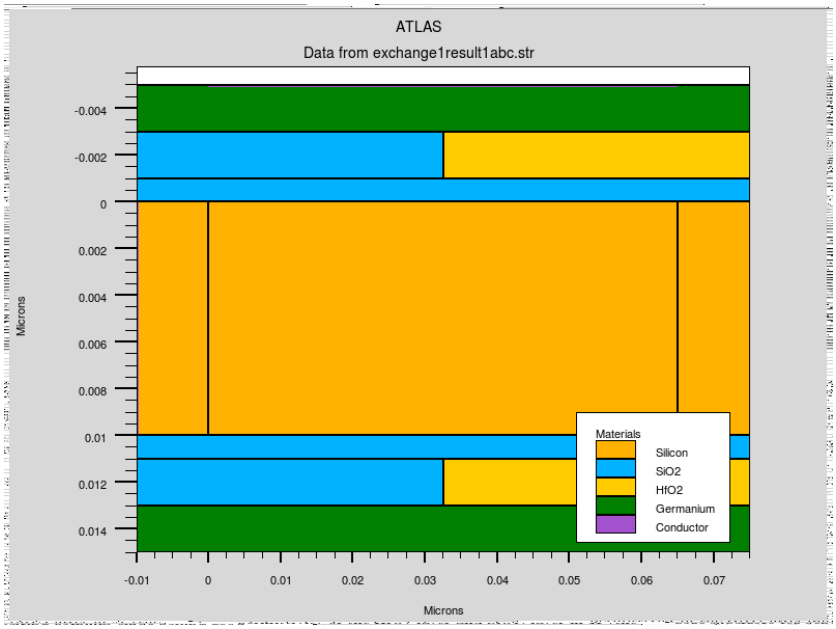

Figure 4.3.5 TonyPlot structure of Hetro Dielectric Double Gate Tunnel FET

To get the improved and desired value of current the above structure was simulated.

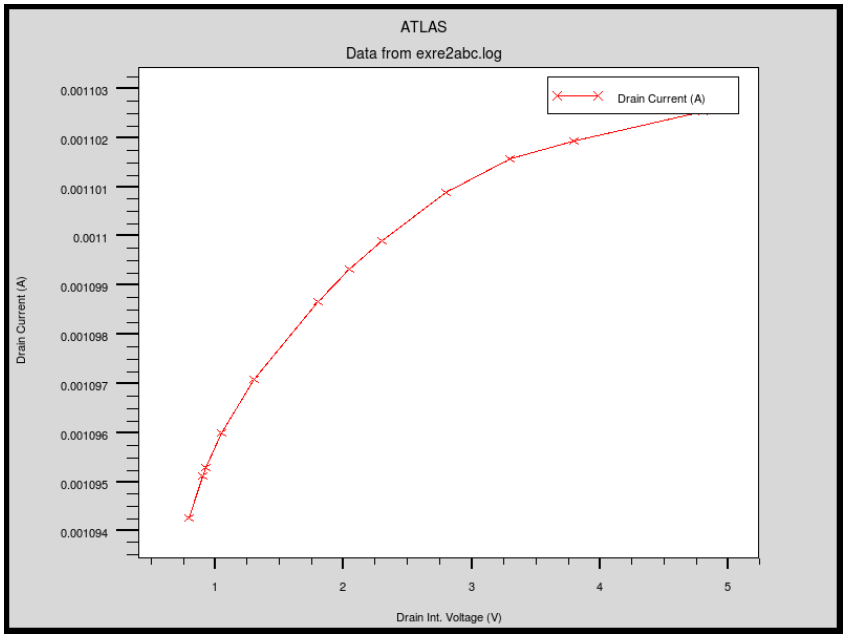

Figure 4.3.6 I_D vs V_D characteristics

The drain current vs drain voltage characteristics was simulated using different structures of the double gate to get the improved current value.

4.4 HETRO DIELECTRIC DOUBLE GATE TUNNEL FET WITH INFRARED RAYS

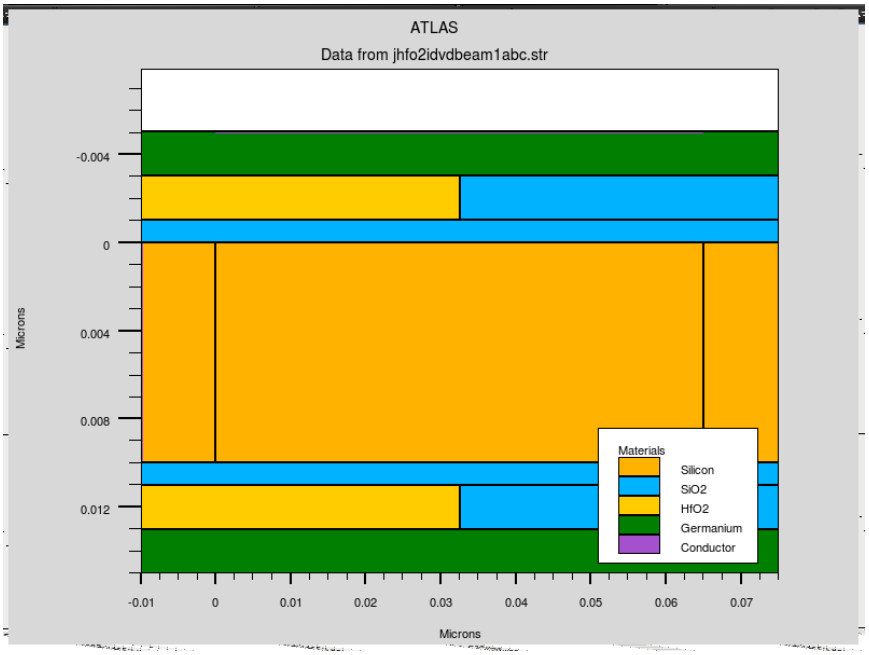

Figure 4.4.1 Tonyplot structure of hetro dielectric double gate tunnel fet with infrared rays

The introduction of infrared radiations increases the amount of current due movement of mobile charge carriers.

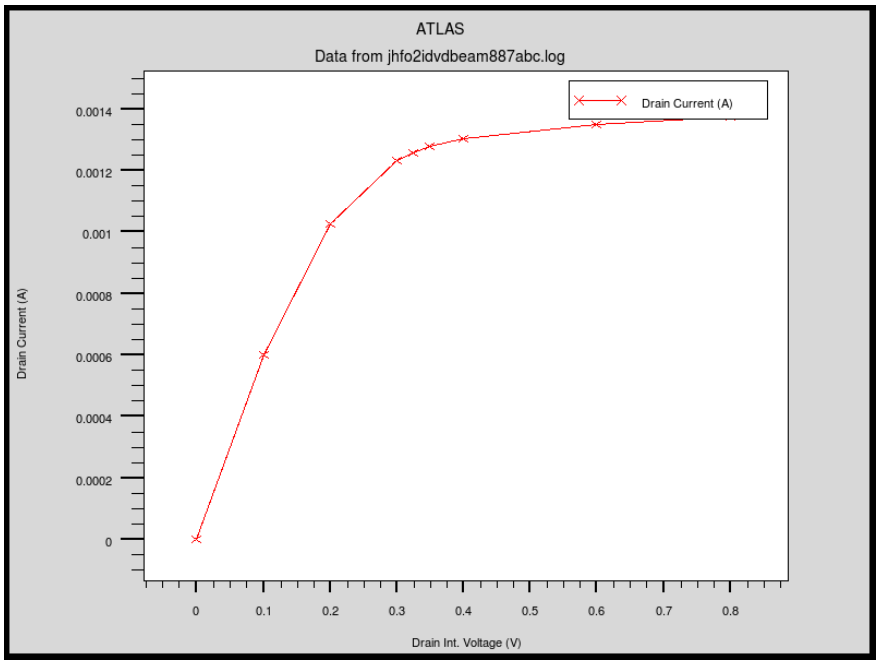

Figure 4.4.2 I_D vs V_D characteristics

Hence , the desirable amount of current is obtained.

CHAPTER 5

CONCLUSION

Conclusion

The structure of TFET was simulated and it was found that the subthreshold voltage suppression was achieved. Further to get the high amount of current Double Gate Tunnel FET several structures were simulated. The presence of double gate helped in increasing the ON-state current of the device and provided immunity to the short channel effects. With the scaling of device parameters, the performance of the device also needs to be efficient. So several other structures were simulated.

Hetro dielectric Double gate tunnel fet includes both types of a dielectric provided larger ON - state current and decreasing the ambipolar effects. The dual material gate was also designed over it to gets perfect device parameters but it was observed that the amount of current can still be improved. So the dielectric positions were reversed, uses of high –k and low – k dielectric were defined. To get the desirable amount of current the device was exposed to infrared radiations. And finally, the simulation results were obtained.

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